32 Mbit Burst Mode Concurrent SuperFlash ComboMemory

SST34WA32A3 / SST34WA32A4 / SST34WA3283 / SST34WA3284

Advance Information

FEATURES:

- **Flash Organization:**
  - 2M x 16
- **PSRAM Organization:**
  - 8 Mbit: 512k X 16
  - 16 Mbit: 1M x 16
- **Single Voltage Read and Write Operations**
  - V_{DD} = 1.7V - 1.95V for Program, Erase and Read
- **Top or Bottom Boot Block Protection**
  - Bottom Boot Protection - SST34WA32x3
  - Top Boot Protection - SST34WA32x4
- **Multiplexed Data/Address for reduced I/O count**
  - A_{15}–A_0 multiplexed as DQ_{15}–DQ_0
  - Addresses are latched by AVD# control input when BEF# is low
- **Low Power Consumption (Typical)**
  - Standby Current: 50 µA
- **Flexible Flash Memory Organization**
  - 4 Banks (512 KW)
  - 63 Uniform 32 KWord blocks
  - Uniform Sectors (2KWord) for entire memory array
- **Concurrent Flash Memory Operation**
  - Read While Program (RWP)
  - Read While Erase (RWE)
- **Erase-Suspend/Erase-Resume Capability**
  - Read while Erase-Suspend
  - Program while Erase-Suspend
  - Read while Program during Erase-Suspend
- **Industry Standard CFI interface compatible**
- **Flash Synchronous Burst Mode Read (54 MHz/66 MHz)**
  - Continuous, Sequential Linear Burst
  - 8/16/32-words with Wrap-Around Burst
  - 8/16/32-words without Wrap-Around Burst
  - Burst Access Time: 13.5 ns/11.5 ns
  - Asynchronous Random Address Access: 70 ns
- **PSRAM Burst Mode Read/Write Access (54 MHz/66 MHz)**
  - Continuous, Sequential Linear Burst
  - 4/8/16-words with Wrap-Around Burst
  - 4/8/16-words without Wrap-Around Burst
  - Burst Access Time: 13.5 ns/11.5 ns
  - Asynchronous Random Address Access: 70 ns
- **Fast Program and Erase (Typical)**
  - Word Program Time: 10 µs
  - Sector/Block Erase Time: 15 ms
  - Chip Erase Time: 30 ms
- **Expanded Block Locking**
  - All blocks locked at Power-up
  - Any block can be locked/unlocked by software
- **Flash Security ID**
  - 128-bit unique ID – factory preset
  - 128-word non-erasable, lockable User-programmed ID bits (“OTP-like”)
- **End-of-Write Detection**
  - Data# Polling
  - Toggle bit
- **Packages Available**
  - 56-ball VFBGA (6 x 8mm)
- **Superior Reliability**
  - Endurance per sector: 1,000,000 cycles (typical)
  - Greater than 100 years Data Retention
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST34WA32A3 / SST34WA32A4 / SST34WA3283 / SST34WA3284 are 32 Mbit (2 Mbit x16) ComboMemory devices which integrate a 32 Mbit flash with either a 16 Mbit PSRAM or 8 Mbit PSRAM in a multi-chip package (MCP). These devices utilize a single 1.8V supply and support burst mode access and address / data multiplex architecture.

The Combo Memory devices feature a 512 KWord uniform multi-bank flash memory architecture that consists of four banks that contain individually-erasable blocks and sectors for increased flexibility. Either the top or bottom bank, consists of 15 standard 32 KWord blocks and four parameter 8 KWord blocks for added granularity. The remaining three banks each contain uniform 32 KWord blocks. Each 32 KWord block is further divided into sixteen uniform 2 KWord sectors. Any bank can be read while another bank is being erased or programmed, with zero latency. In addition, these devices provide Erase-Suspend mode during which data can be programmed to, or read from, any sector or block that is not being erased.

SST34WA32A3/32A4/3283/3284 support synchronous Burst mode Read from any address location of the flash memory array; and Burst mode Read and Write from any address location of the PSRAM. The Burst modes allow the devices to Read or Write sequential data with significantly shorter latency delays than during a random read or write.

To protect against inadvertent write, the flash memory bank offers an expanded Block Locking scheme. Each block can be individually locked, and the top or bottom 8 KWord parameter blocks of each boot block can be individually locked for finer granularity. In addition, a 136-words Security ID, included on the flash memory, increases system design security.

Designed, manufactured, and tested for applications requiring low power and small form factor the SST34WA32A3/32A4/3283/3284 are offered in an extended temperature with a small footprint package to meet board space constraints requirement. See Figure 8 for pin assignments.

Advance Information

DEVICE OPERATION

The SST34WA32A3/32A4/3283/3284 control operation of either the flash or the PSRAM memory bank using BEF# and BES#.

When BEF# is low, the flash bank is activated for Read, Program, or Erase operation. When BES# is low, the PSRAM is activated for Read and Write operation.

Do not assert BEF# and BES# low at the same time. If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.

Flash Memory

Various commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. See Table 20 on page 30 for the command sequence for each function.

The flash memory of SST34WA32A3/32A4/3283/3284 has an Auto Low Power mode which puts the device in a “near stand-by” mode after data has been accessed with a valid Read operation. This reduces the flash active read current. The Auto Low Power mode reduces the current consumption of the flash memory to stand-by level. The flash memory exits the Auto Low Power mode with any address or flash control signal transition; therefore, there is no access time penalty for Read cycles.

TABLE 1: Critical Parameters

Critical Parameters	Values	Units
Max Random Address Access Time	70	ns
Max Synchronous Access Time (54 MHz)	13.5	ns
Max Synchronous Access Time (66 MHz)	11.5	ns

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Concurrent Read/Write Operation

The multi-bank architecture of the flash memory of this device allows zero latency Concurrent Read/Write operation whereby the user can read from one bank of the flash while programming or erasing in another bank. With this operation a user can read system code in one bank while updating data in another bank. A unique feature of the SST34WA32A3/32A4/3283/3284 is ability to Read during an Erase-Suspend even while Programming in another bank. This feature is designed to respond to interrupt requests during concurrent operation. See Table 2, Current Read/Write State.

TABLE 2: Concurrent Read/Write State

Current Operation in One Bank	Possible Operation in Any Other Bank
Read	No Operation
Read	Write
Write	Read
Write	No Operation
No Operation	Read
No Operation	Write

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Note: For the purposes of this table, “Write” means to perform Sector/Block or Word-Program operations as applicable to the appropriate bank.

Asynchronous Read

The default configuration of the flash memory on power-up, or after a hardware reset via the RST# pin, is Asynchronous Read. To read data from the flash memory array, the system must assert a valid address on A/DQ_{15}–A/DQ_0 and A_{20}–A_{16}, while AVD# and BEF# are at V_{IL}. During the read, WE# remains at V_{IH} and CLK is X for Asynchronous Read, the rising edge of AVD# latches the address, and OE# is driven to V_{IL}. The data appears on A/DQ_{15}–A/DQ_0. For details, see Figure 9. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (T_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (T_{CE}) is the delay from the stable addresses and stable BEF# to valid data at the outputs. The output enable access time (T_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set to read array data upon device power-up or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Burst Mode Read (Synchronous)

The SST34WA32A3/32A4/3283/3284 flash memory default configuration on power-up or after reset is Asynchronous Read. However, it can be configured to operate in a Synchronous Read mode with a continuous, sequential linear burst operation or a linear burst operation of 8-, 16-, or 32-words length with wrap-around.

Before setting the flash memory configuration to Burst Mode, determine the number of wait states for the initial word access time (T_{IACC}) and the desired Burst mode—continuous with, or without, wrap-around.

WAIT States

On power up, the flash memory of SST34WA32A3/32A4/3283/3284 defaults to asynchronous read operation. The device is automatically enabled for burst mode on the first rising edge on the CLK input, while the AVD# is held low and the addresses are latched on the first rising edge of the CLK. Prior to activating the clock signal, the system determines how many wait states are desired for the initial word (T_{IACC}) of each burst session. The system then writes the Set Configuration Register command sequence.

The device automatically delays RY/BY# by the needed number of clock cycles if data is not ready. Refer to the details in “Handshaking Feature” section.

The initial word is output on the Data Bus T_{IACC} after the active edge of the first CLK cycle. Each successive clock cycle automatically increments the addresses counter. Subsequent words are output on the Data Bus T_{BACC} after the active edge of each successive clock cycle.

To return the device to Asynchronous Read mode, either drive BEF# to V_{IH} or drive RST# to V_{IL}.

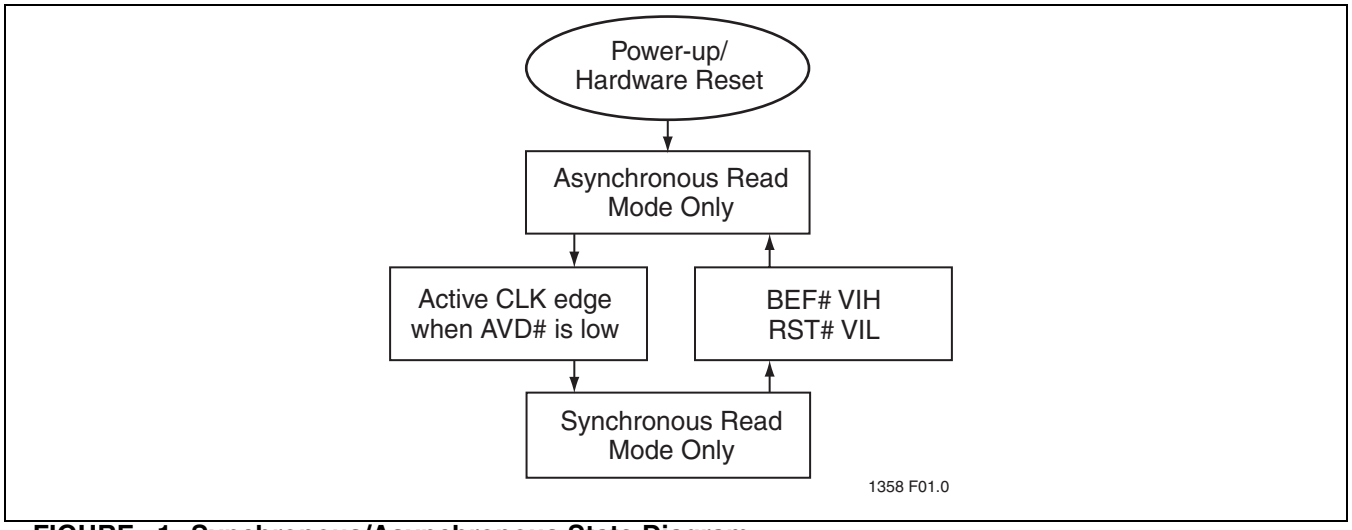

FIGURE 1: Synchronous/Asynchronous State Diagram

8-, 16-, 32-Words Linear Burst Mode with Wrap-Around

The flash memory of the SST34WA32A3/32A4/3283/3284 device supports a synchronous read operation with a Linear Burst mode of a pre-determined word length with wrap-around. Groups of 8, 16, and 32 words can be read in this way as defined in Table 3.

In 8, 16, and 32-words Linear Burst mode operation, the starting address of the linear burst sequence is the address written to the device. Each successive clock cycle automatically increments the address counter until the top address of the group is reached. Once the top address is reached, the address wraps back to the first address of the selected group and continues incrementing from there.

An example of an 8-word linear Burst mode with Wrap-Around is as follows: if the starting address in the 8-word mode is 11H (8 words group start = 10H, group end = 17H), the address range to be read would be 10H-17H, and the burst sequence would be 11H -12H -13H - 14H - 15H - 16H - 17H - 10H - and so on.

The RY/BY# pin will indicate when valid data is present on the data bus.

TABLE 3: 8-, 16-, 32-Words Linear Burst Mode Wrap-Around Groups

Group Size	Address Ranges				
8 words	00000H - 00007H	00008H - 0000FH	00010H - 00017H	…	(A)[1] - (A + 7H)
16 words	00000H - 0000FH	00010H - 0001FH	00020H - 0002FH	…	(B)[1] - (B + FH)
32 words	00000H - 0001FH	00020H - 0003FH	00040H - 0005FH	…	(C)[1] - (C + 1FH)

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1. A is a multiple of 00008H, B is a multiple of 00010H, and C is a multiple of 00020H.

8-16-32-Words Linear Burst Mode without Wrap-Around

The SST34WA32A3/32A4/3283/3284 flash memory supports a synchronous read operation with a Linear Burst mode that does not wrap around. A fixed number of words predefined as 8-, 16-, or 32-words are read from consecutive addresses starting with the initial word, which is written to the device. Once the fixed number of words are read completely, the Burst Read operation stops and the RY/BY# output goes low. There is no group limitation as there is with Linear Burst with Wrap-Around. See Table 3 for group definitions.

An example of an 8-word linear Burst mode without Wrap-Around is as follows: for an 8-word length Burst Read, if the starting address written to the device is 39h, the burst sequence would be 39-3A-3B-3C-3D-3E-3F-40h, and the read operation will be terminated at 40h. In a similar fashion, the 16-word and 32-word modes begin their burst sequence on the starting address written to the device, and Continuously Read to the predefined word length, of 16 or 32 words.

The operation is similar to the Continuous Burst, but will stop the operation at fixed word length. If the device crosses the first 32-word address boundary during burst read, a latency may occur before data appears for the next address and RY/BY# is pulsing low. If the burst read start address is 8-word boundary aligned (A0 = A1 = A2 = 0), the latency does not occur. If the host system crosses the bank boundary, the device will react in the same manner as in the Continuous Burst.

Continuous Linear Burst Mode

The flash memory of SST34WA32A3/32A4/3283/3284 supports a synchronous read operation with a continuous, sequential linear Burst mode read. When in this mode, the Addresses are automatically incremented linearly with every successive clock active edge. If the device reaches the Highest Memory Location Address (FFFFFH), it will continue the continuous, sequential linear Burst read operation by wrapping around to Address 00000H. The Burst operation will continue sequentially until another address is latched via the AVD# pin, until BEF# is driven to V_{IH}, or until RST# is driven to V_{IL}.

When an address is latched via AVD# pin with active edge of CLK, a new burst read will start with a new initial address.

If the continuous, sequential linear burst read sequence crosses a bank boundary into a bank that is performing a Programming or Erasing operation, the device will provide status information. Once the system has completed the status read operation, or the device has completed the Program/Erase Operation, the system is allowed to start a new burst read operation. In this case a new address needs to be latched via the AVD# pin.

In synchronous, continuous, sequential, linear read array, a latency in output data may occur when a burst sequence crosses the first 32-word address boundary. If the burst read start address is 8-word boundary aligned ($A_0 = A_1 = A_2 = 0$), the delay does not occur. If the burst read start address is mis-aligned to an 8-word boundary, the delay occurs once per burst-mode read sequence. The RY/BY# signal will indicate this delay to the system.

Burst Register

The flash memory of SST34WA32A3/32A4/3283/3284 defaults to Asynchronous Read on power-up. However, it can be configured to operate in a Synchronous Read Mode with continuous, sequential linear burst operation and linear burst operation of 8-, 16-, 32- words length with wrap-around.

The Burst Register is used to configure the type of read bus access the flash memory will perform by setting the desired Mode of Burst (continuous or wrap-around) and the number of wait states for the initial word access time (T_{IACC}).

The user can set the Burst Register with the Set Burst Register Command. The Burst Register will retain its information until it is reset via the RST# pin or after Power-Up.

The Set Burst Register Command is initiated by executing a three-cycle command sequence. On the last bus cycle, Data is C0H, address bits A_{11}–A_0 are 555H, and address bits A_{17}–A_{12} set the code to be latched, as shown in Table 4.

Upon power-up or hardware reset using the RST# pin, the device will be in the default state. The Burst Register cannot be changed if the device is Programming, Erasing, or if it is in Sector Lock/Unlock mode.

TABLE 4: Burst Mode Configuration Command

Function	Address	Value
Programmable Initial WAIT State	A_{12}	A_{14} - A_{13} - A_{12} values
	A_{13}	0 - 0 - 1 = 3 wait states for initial word
	A_{14}	0 - 1 - 0 = 4 wait states for initial word
		0 - 1 - 1 = 5 wait states for initial word
		1 - 0 - 0 = 6 wait states for initial word
		1 - 0 - 1 = 7 wait states for initial word (default)
		1 - 1 - 0 = Reserved
		1 - 1 - 1 = Reserved
Burst Mode Type	A_{15}	A_{16} - A_{15} values
	A_{16}	0 - 0 = Continuous burst (default)
		0 - 1 = 8-word linear burst
		1 - 0 = 16-word linear burst
		1 - 1 = 32-word linear burst
	A_{17}	0 = linear burst with wrap-around (default)
		1 = linear burst without wrap-around

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Note: The Device will be in the default state after Hardware Reset (via RST# pin) or after Power-Up.

Burst Suspend/Resume

The Burst Suspend / Resume feature allows the system to temporarily suspend a synchronous burst operation on the flash memory during the initial access, before data is available, or after the device is reading data. When the burst operation is suspended, previously latched internal data and the current state are retained.

Burst Suspend occurs when BEF# is asserted, WE# is de-asserted, and OE# is de-asserted. CLK must be halted at V_{IH} or V_{IL}. To resume the burst access, OE# is reasserted, and afterwards CLK can be restarted. Subsequent CLK edges resume the burst sequence where it was suspended.

When the Burst Suspend is enabled the flash will enter a low power mode, in which the current consumption is reduced to typically 1mA. The RY/BY# pin, which is controlled by BEF#, will remain active and is not placed into a high-impedance state when OE# is de-asserted.

Writing Commands

The SST34WA32A3/32A4/3283/3284 accept address and data information in the form of program commands. To write a command, the system needs to drive BEF#, and WE# to V_{IL}. The addresses are latched on the rising edge of AVD# while keeping OE# at V_{IH}, and data is latched on the rising edge of WE# while keeping OE# at V_{IH}.

Word-Program Operation

The SST34WA32A3/32A4/3283/3284 are programmed on a word-by-word basis. Before programming, erase the sector to be programmed.

A Program operation is accomplished in three phases. First, the Software Data Protection is initiated using the three-word load sequence. Next, the word address and word data are loaded. Finally, the internal Program operation initiates after the rising edge of the fourth WE#. The Program operation completes within 12 µs.

The SST34WA32A3/32A4/3283/3284 features an programming acceleration mode for faster programming. Once the device enters the programming acceleration mode, only two write cycles are required to program a word, instead of the four cycles required in the standard program command sequence.

During the Program operation, the only valid reads within the bank being programmed are status reads (DQ_7 Data# Polling and DQ_2/DQ_6 Toggle Bits). Any commands issued during an internal Program operation are ignored.

When the Program Operation is complete, the bank will return to Read Array Mode. For Program operation timing diagram and flowchart, see Figure 13 and Figure 47.

Programming Acceleration Operation

The programming acceleration makes programing faster than using a standard program command sequence because it reduces the standard four-cycle process to two cycles. Two unlock cycles initiates the programming acceleration command sequence which is followed by a third write cycle containing 20H as the programming acceleration command. The chip enters the programming acceleration mode. To program in this mode, a two-cycle programming acceleration program command sequence is all that is required. The first cycle contains the programming acceleration command, A0h; the second cycle contains the program address and data. Likewise, additional data is programmed. The initial two unlock cycles required in the standard program command sequence is eliminated. This reduces the total programming time. See Table 20 for programming acceleration command sequence requirements.

The system issues a two-cycle programming acceleration reset command sequence to exit the programming acceleration mode and return to the read mode. The first cycle contains the data 90h, and the second cycle contains the data 00h.

Eight-Word Program

An Eight Word Program command is provided for fast data programming. At room temperature and normal V_{DD}, the command is only enabled when the ACC pin is at Supervoltage VH (11.4V to 12V). The Eight Word Program Operation is initiated with the A0H command and then the host provides eight consecutive data words. The Eight Word program is an Asynchronous operation and the CLK signal is ignored. The system drives BEF# low to V_{IL} and the Initial address is latched on the rising edge of the first AVD# pulse while keeping OE# high. Data is latched on the rising edge of each WE# pulse while keeping OE# high. See Figure 15 for AC timings. The Initial address A_{INI} must be 8-words boundary aligned ($A_0 = A_1 = A_2 = 0$), otherwise the part will force the boundary alignment. Each subsequent WE# pulse will automatically increment the address of one word from A_{INI} to $A_{INI + 7}$. The user must issue 8 data words to be programmed when in Eight Word Program Mode.

Standby Mode

The SST34WA32A3/32A4/3283/3284 flash memory enter the Standby mode when both the BEF# and RST# inputs are held at V_{DD} ± 0.2 V. The device requires standard access time (T_{CE}) for read access before it is ready to read data.

Auto Low Power Mode

The flash memory of these devices have the Auto Lower Power mode which puts it in a near standby mode. In Asynchronous read mode, this happens when addresses remain stable within T_{ACC} + 60 ns after data is accessed with a valid Read operation. This reduces the flash active Read current to 3 µA, typically.

While BEF# is low, the device exits Auto Low Power mode with any address transition or control signal transition used to initiate another flash Read cycle, with no access time penalty. While in Auto Low Power mode, output data is latched and always available to the system.

In synchronous read mode, after the AVD# falling edge, the flash memory automatically enters the Auto Low Power mode when there is no active CLK edge within T_{ACC}+ 60ns. The flash memory exits Auto Low Power mode with an active CLK edge.

Memory Architecture

The flash memory of SST34WA32A3/32A4/3283/3284 features a 4-bank, 512 KWord uniform multi-bank architecture. Either the top or bottom bank consists of 15 standard 32 KWord blocks and four parameter 8 KWord blocks for added granularity. The remaining three banks each contain uniform 32 KWord blocks. All 8 and 32 KWord blocks are further divided into 4 or 16 uniform 2 KWord sectors, respectively.

Each block and sector can be individually erased for greater flexibility. The device's unique bank architecture, allows reads from any bank while another bank is being erased (RWE) or programmed (RWP). The device also supports an Erase-Suspend mode that allows programming data in any other sector or block other than the one being erase-suspended. It can also read data at any memory sector or block other than the one being erased during the Erase-Suspend operation. Suspend operations cannot be nested because the system needs to complete or resume any previously suspended operation before a new operation can be suspended.

Sector/Block-Erase Operation

The Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector or block-by-block basis. The SST34WA32A3/32A4/3283/3284 offers Sector-Erase and Block-Erase modes. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode erases either the regular 32 KWord blocks or the smaller 8 KWord Parameter Blocks. The Sector-Erase operation is initiated by executing a six-word command sequence with Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-word command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The Sector or Block address is latched during the sixth cycle, either on the rising edge of AVD# or on the falling edge of WE# cycle, whichever occurs last, while the command (30H/50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figure 14 for timing waveforms and Figure 51 for the flowchart.

Erase-Suspend, Erase-Resume Operations

The Erase-Suspend command temporarily suspends a Sector/Block-Erase operation which allows data to be read from any memory location, or to be programmed into any sector or block that is not suspended for an Erase operation. The operation is executed by issuing the Erase-Suspend one-word command, B0H. The device automatically enters the Erase-Suspend Read Mode within TES, 15 µs, after the Erase-Suspend command is issued. Valid data is read from any sector or block that is not suspended from an Erase operation. Reading at an address location within erase-suspended sectors or blocks will output DQ2 toggling and DQ6 at '1'. See Table 6, Write Operation Status, for details. While in Erase-Suspend mode, a Word-Program operations are allowed for all sectors and blocks, with the exception of the sector or block selected for Erase-Suspend. If a Word Program operation is attempted in the suspended sector or block, the command is rejected and the Program operation is not performed.

The system can also issue the Software ID Entry command during the Erase-Suspend. After the system has issued the Software ID Exit command, the device automatically reverts to Read Mode.

To resume the Sector/Block-Erase operation that is suspended, the system must issue the Erase-Resume command. The operation is executed by issuing the Erase-Resume one-word command, 30H, at any address in the last word sequence.

For an erase operation being suspended or re-suspended after resume, the cumulative erase time needed is greater than the erase time of a non-suspended erase operation. The accumulative erase time needed may become very long if the hold time from Erase-Resume to the next Erase-Suspend operation, T_{ERH}, is less than 330µs.

The Erase-Resume command will be ignored until any program operations initiated during Erase-Suspend are complete. The Erase-Suspend and Program Resume operations have no influence on the program operation. See Table 5 for details of Suspend-Resume and Concurrent operations

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TABLE 5: Erase-Suspend and Concurrent Banks State

Current Operation in One Bank	Possible Operation in The Same Bank	Possible Operation in Any Other Concurrent Bank
Sector/Block-Erase-Suspend	Read any other Sector/Block within the same Bank	No Operation
Sector/Block-Erase-Suspend	Read any other Sector/Block within the same Bank	Program any Sector/Block
Sector/Block-Erase-Suspend	Program any other Sector/Block within the same Bank	No Operation
Sector/Block-Erase-Suspend	Program any other Sector/Block within the same Bank	Read any Sector/Block
Sector/Block-Erase-Suspend	No Operation	Read any Sector/Block
Sector/Block-Erase-Suspend	No Operation	Program any Sector/Block

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Chip-Erase Operation

The SST34WA32A3/32A4/3283/3284 provides a Chip-Erase operation which allows the user to erase the entire flash memory array to the '1' state. This is a quick way to erase the entire flash memory. To initiate the Chip-Erase execute a six-word command sequence with the Chip-Erase command, 10H, at address 555H in the last word sequence. The Erase operation begins with the rising edge of the sixth WE#. During the Erase operation, the only valid reads are Toggle Bit or Data# Polling. See Table 20 for the command sequence, Figure 14 for timing diagram, and Figure 51 for the flowchart. Any commands issued during the Chip-Erase operation are ignored, including the Erase-Suspend Command. If WP# pin is held to V_{IL}, or one or more blocks are locked, the Chip Erase Operation is disabled.

Write Operation Status Detection

The SST34WA32A3/32A4/3283/3284 optimizes the system flash Write cycle time by providing two software means to detect the completion of a Program Write cycle or an Erase Write cycle. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of- Write detection mode, which is enabled after the rising edge of WE#, initiates the internal Program or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling (DQ7), or Toggle Bit (DQ6) Read may be simultaneous with the completion of the Write cycle. If this occurs, the system will get an erroneous result. For example, valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection when an erroneous result occurs, the software routine must include a loop to read the accessed location an additional time. If both Reads indicate the completion, then the Write cycle has completed.

Ready (RY/BY#)

The RY/BY# pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during synchronous burst reads. When RY/BY# is asserted (RY/BY# = V_{OH}), the output data is valid and can be read. When RY/BY# is de-asserted (RY/BY# = V_{OL}), the system will wait until RY/BY# is re-asserted before expecting the next word of data.

Two conditions cause the RY/BY# output to be low: during the initial access while in burst mode, and when the device is set to Continuous Burst Mode and the address crosses the first 32 word boundary.

In asynchronous, non-burst mode, the RY/BY# pin does not indicate valid or invalid output data. Instead, RY/BY# = V_{OH} when BEF# = V_{IL}, and RY/BY# is Hi-Z when BEF# = V_{IH}.

Data# Polling (DQ7)

When the SST34WA32A3/32A4/3283/3284 is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector/ Block or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 16 for Data# Polling timing diagram and Figure 48 for a flowchart.

Toggle Bits (DQ6 and DQ2)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating '1's and '0's. For example, toggling between '1' and '0'. When the internal Program or Erase operation is complete, the DQ6 bit will stop toggling. The device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle Bit (DQ6) is valid after the rising edge of sixth WE# pulse. DQ6 will be set to '1' if a Read operation is attempted on an Erase-Suspended Sector/Block. If the Program operation is initiated in a sector/block not selected for Erase-Suspend mode, DQ6 will toggle. An additional Toggle Bit is available on DQ2, which can be used in conjunction with DQ6 to check whether a particular sector is being actively erased or erase-suspended. Table 6 shows detailed status bit information. The Toggle Bit (DQ2) is valid after the rising edge of the last WE# pulse of the Write operation. See Figure 17 for Toggle Bit the timing diagram and Figure 48 for a flowchart.

TABLE 6: Write Operation Status

Status		DQ7	DQ6	DQ5	DQ2
Normal Operation	Standard Program	DQ7#	Toggle	0	No Toggle
	Standard Erase	0	Toggle	0	Toggle
Erase-Suspend Mode	Read from Erase-Suspended Sector/Block	1	1	0	Toggle
	Read from Non- Erase-Suspended Sector/Block	Data	Data	Data	Data
	Program	DQ7#	Toggle	0	N/A

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Note: Note: DQ7, DQ6 and DQ2 require a valid address when reading status information. When in Erase-Suspend Mode the system can read either synchronously (Burst) or asynchronously.

Data Protection

The SST34WA32A3/32A4/3283/3284 provides both hardware and software features to protect flash memory data from inadvertent writes.

Hardware Data Protection

The device provides the following protection features to prevent inadvertent writes to the flash memory:

- Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a write cycle.
- V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than V_{LKO}.
- Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

A_{CC} Pin

When the A_{CC} pin is brought to the Supervoltage VH the Eight Word Program command is enabled. In this case all blocks are temporarily unprotected regardless of the Block Locking Register. The only device operation available when A_{CC} pin is at V_H is Eight Word Programming, the A_{CC} pin must not be held above V_{IH} during other operations. Eight Word Programming is provided for fast data programming in the manufacturing environment. The device will return to normal operations when voltage is set to V_{IH} on A_{CC} pin and each block locking status will depend on the Block Locking Register value (this is the value that each block had before the application of V_H on A_{CC}). The A_{CC} pin must not be left floating or unconnected.

When the A_{CC} pin is brought to V_{IL} all sectors are locked. The A_{CC} pin should be at V_{IH} for all other conditions and chip operations.

WP# Pin

The SST34WA32A3/32A4/3283/3284 provides a hardware block protection which protects the 8 KWords for Blocks BA0 and BA1 (SST34WA32x3), and/or BA65 and BA66 (SST34WA32x4) of the flash memory. BAx stands for Block Address.

The 8 KWord blocks, located in the top or bottom blocks, are protected when WP# is held to V_{IL}. The Program and Erase operation in these blocks is disabled independently using the Block Locking Register Status. The user can disable the hardware protection for the outermost blocks by driving WP# to V_{IH}. In this case, the Protection Status of the two outermost Blocks will revert to what is indicated by the corresponding Block Locking Registers. WP# will be latched at a specific time in the program or erase sequence. To prevent a write to the outermost blocks, WP# must be held to V_{IL} on the last write cycle of the sequence. For example, the 4th write cycle in the program sequence and the 6th write cycle in the erase sequence. If using the

programming acceleration feature, on the 2nd program cycle after the programming acceleration command is written, WP# must be held to V_{IL} on the 2nd cycle. If the WP# pin is held to V_{IL} the Chip Erase Operation is disabled. WP# should be in pull-up state if it is not used.

Software Block Locking

To prevent accidental data programming or erasing, the Block Lock command is used. All 32 KWord main blocks and 8KW parameter blocks can be independently locked. A locked block can not be able to be programmed or erased. After Power-Up, all blocks are locked.

Changing the state-of-lock for a block is done by using the Block Lock/Unlock Command (60H). See Table 20.

In the third cycle the address must point to the Block to be locked/unlocked. The status of the A_6 Address bit will specify if the block must be locked (A_6=V_{IL}) or unlocked (A_6=V_{IH}). After the third cycle, the state-of-lock of additional Blocks in the same Bank can be modified.

Reading the state-of-lock for each block is achieved using the Read Block Locking Register command with the address parameter that is within the block address space For details, see Table 20. This command will read the Block Locking Register. If the Block Locking Register is 0000H the Block is Unlocked, if it is 0001H the Block is Locked.

The Read Block Locking Register command can be written to a bank which is either in Read Mode or in Erase-Suspend-Read mode. Only one bank at a time can be switched to Read Block Locking Register mode. To return the selected bank to Read Mode, or Erase-Suspend Read Mode, the Software ID Exit/Block Locking Exit Command must be issued by the system. see Table 20.

WP# is internally ORed with the Block Locking register. When WP# is low, the blocks are hardware write protected regardless of the state of the Write-Lock bit for the corresponding Block Locking registers. Clearing the Write-Protect bit in any register when WP# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

After the third cycle, the state-of-lock for additional Blocks in the same Bank can be modified.

TABLE 7: Block Locking Register Data

Reserved Bits BLR[15:1]	Write-Lock bit: BLR[0]	Hex Code	Lock Status
000000000000000	0	0000H	Full Access
000000000000000	1	0001H	Write Locked (Default State at Power-Up)

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Note: The default read status of all blocks upon power-up is write-locked (“01H”). After power-up, when the power supply (V_{DD}) is valid, the register is alterable.

Hardware Reset (RST#)

The RST# pin provides a hardware method to reset the flash memory of devices to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and the flash memory will return to Read Array mode. When no internal Program/Erase operation is in progress, a minimum period of T_{RH} is required after RST# is driven high before a valid Read can take place.

The interrupted Erase operation must to be reinitiated after the flash memory resumes normal operation mode to ensure data integrity.

The RST# pin is an asynchronous input signal which aborts an on-going Erase or Program operation and resets the flash memory to Read Array mode within a time T_{Readyw}. If RST# pin is asserted during a flash Read Operation, the required time to reset the device is T_{Ready}. At this point all outputs are tri-stated, and the device ignores any Read/Write operations for the duration of the RST# low pulse. The RST# reset operation will also reset the Flash Burst Configuration register to Asynchronous Read Mode and set the flash memory in Read Array mode.

Software Data Protection (SDP)

The SST34WA32A3/32A4/3283/3284 provides the JEDEC approved Software Data Protection scheme for all data alteration operations of the flash memory, such as Program and Erase. Any single word Program operation requires the inclusion of the three-word sequence. The three-word load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations; for instance, during the system power-up or power-down. Any Erase operation requires the inclusion of six-word sequence. These devices are shipped with the Software Data Protection permanently enabled. See Table 20 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode within T_{RC}. The contents of DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Common Flash Memory Interface (CFI)

The SST34WA32A3/32A4/3283/3284 contains the CFI information to describe the characteristics of the flash memory. In order to enter the CFI Query mode, the system must write a one word command or a three-word sequence, with 98H— the CFI Query command—to address 555H in the last word sequence. Once the device enters the CFI Query mode, the system can read the CFI data at the addresses given in Tables 23 through 27. The System can write the CFI entry command when the device is in Read Array mode and also when the device is in Product Identification Mode. The system must write the CFI Exit command to return to Read mode or Erase-Suspend Read mode from the CFI Query mode.

Security ID

The SST34WA32A3/32A4/3283/3284 device offers a 136-word Security ID space. The Secure ID space is divided into two segments—one 8-word, 128-bit factory programmed segment and one 128-word user programmed segment. The first segment is programmed and locked at SST with a unique 128-bit number. The user segment is left un-programmed for the customer to program as desired.

To program the user segment of the Security ID, the Security ID Word-Program command is required. Check the end-of-write status of the Security ID by reading the toggle bits. Do not use Data# Polling to detect the end-of-write. Once the programming is complete, the Sec ID must be locked using the User Sec ID Program Lock-Out, which disables any future corruption of this space. Neither SEC ID segment—user nor factory programmed—can be erased, regardless of whether or not the Sec ID is locked. The Secure ID space can be queried by executing a three-word command sequence with Enter Sec ID command (88H) at address 555H in the last byte sequence. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 8 for more details.

The Security ID space is located at addresses 000000H to 0000FFH. The Factory programmed segment is located at addresses 000000H to 000007H. The User segment is located at address 000080H to 0000FFH. The Security ID Locked/Unlocked status can be read at Address 000007FH. See Table 20. If DQ_3 = '1' the User Segment of the Security ID is Unlocked. When DQ_3 = '0', the User Segment of the Security ID is Locked. Once the Query Security ID Command is executed, the system can read the Security ID space with normal Read cycles using the valid address range 0000000H to 00000FFH. See Table 8 for more details.

TABLE 8: Security ID Valid Range

Security ID Segment	Start Address	End Address
Factory Programmed	000000H	000007H
User Programmed	000080H	0000FFH
Sec ID Locked/ Unlocked Status	00007FH	

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Product Identification

The Product Identification mode identifies the devices and the manufacturer. For software operation details see Table 20, for Software ID Entry command sequence flowchart see Figure 49. The Product Identification Mode (PIM) is entered by issuing two unlock cycles. This must be followed by a third cycle that contains the Bank Address (BA using A_{20} to A_{19}) and the Product Identification Mode command. After this third cycle, the addressed Bank enters the Product Identification Mode. The system can read the manufacturer ID or the Device ID any number of times without re-issuing the PIM command sequence. The Product Identification command may be written to a bank that is either in Read Mode or in Erase-Suspend Read Mode. The Product Identification Command cannot be written while the device is Programming or Erasing another bank. If the system addresses a different Bank, memory array data is read from the device following normal Asynchronous Read operation. No subsequent data will be made available if the device is in Synchronous Mode. The system must issue the Software ID Exit command in order to return the Bank previously set in Product Identification Mode into Read mode or Erase-Suspend Read mode.

TABLE 9: Product Identification

	Address	Data
Manufacturer's ID	BK_X0000H	00BFH
Device ID		
SST34WA32A3/3283	BK_X0001H	975BH
SST34WA32A4/3284	BK_X0001H	975AH

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Note: BK_X = Bank Address, using A_{20} to A_{19}.

Product Identification Mode / CFI Mode / Security ID / Block Locking Exit

In order to return the device to the standard Read Array Mode, the Software Product Identification / CFI / Security ID / Block Locking Modes must be exited. Exit is accomplished by issuing the Software Product Identification / CFI / Security ID / Block Locking Modes Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read Array Mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. The Software Product Identification / CFI / Security ID / Block Locking Query/Exit command cannot be executed concurrent to Program/ Erase operations. See Table 20 for the software command code, Figure 50 for a flowchart.

Handshaking Feature

The device is equipped with a handshaking feature that brings out the fastest initial latency of this burst mode flash memory by simply monitoring the RY/BY# signal from the device to determine when the initial word of burst data is ready to be read. In this handshaking mode, the microprocessor does not need to set its register the number of initial wait clocks. The device will indicate when the initial word of burst data is valid by the rising edge of RY/BY# after OE goes low. If the handshaking feature is not used for burst mode performance optimization, then the host system must set the appropriate number of wait states in the flash device depending on clock frequency. See "Configuration Register Set Command" section for more information.

V_{DD} Power-up/Power-down Sequencing

There are no restrictions on V_{DD} sequencing during power-up or power-down. Setting RST# to V_{IL} level is required during the entire V_{DD} power sequence until the respective supplies reach their operating voltages. Once V_{DD} reach their respective operating voltages, setting RST# to V_{IH} level is allowed.

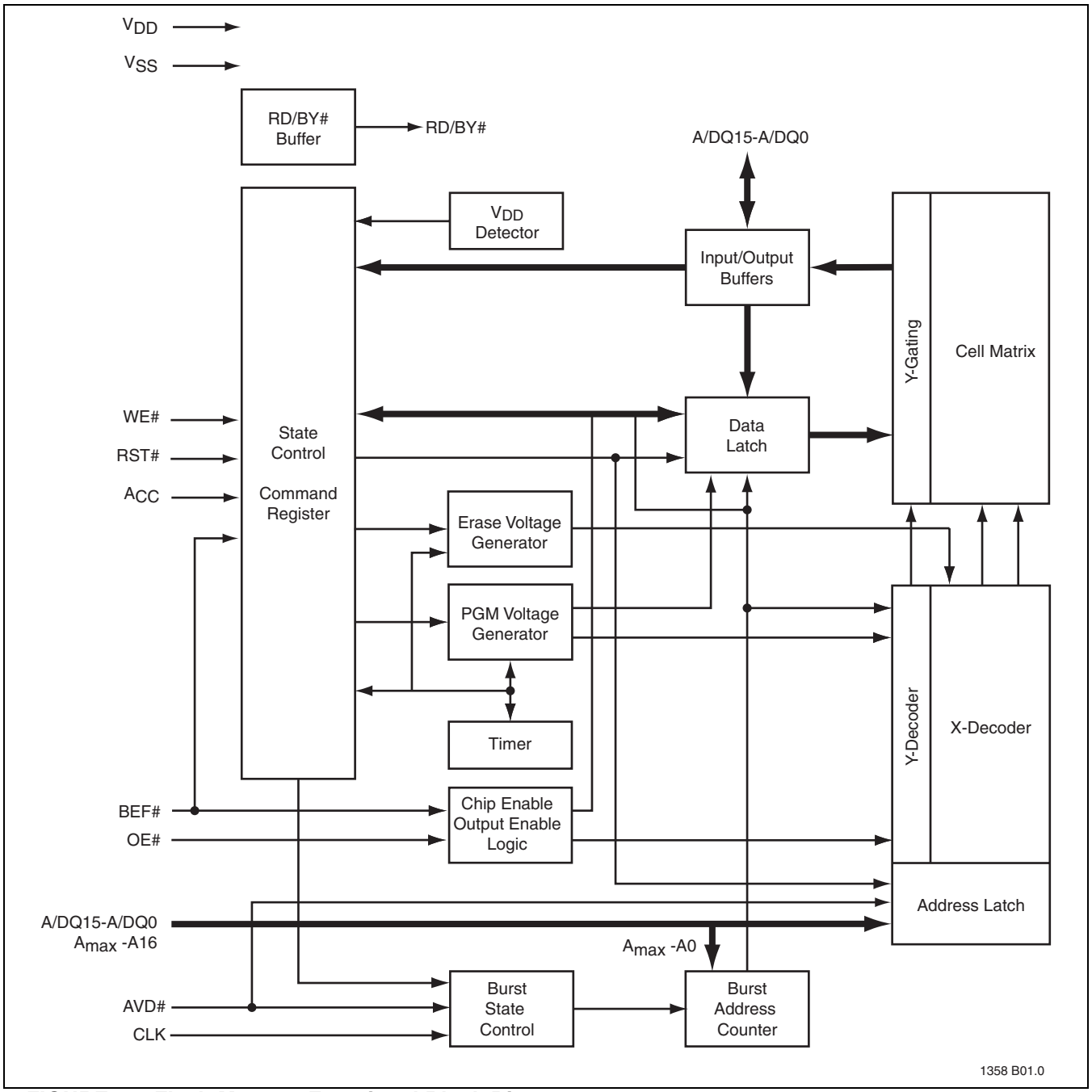

FIGURE 2: Flash Memory Functional Block Diagram

TABLE 10: SST34WA32A3/3283, 8 Mbit x4 Concurrent SuperFlash Multi-Bank Memory Organization (1 of 2)

Bank	Block	Block Size	Address Range
A	BA0	8 Kwords	000000h–001FFFh
	BA1	8 Kwords	002000h–003FFFh
	BA2	8 Kwords	004000h–005FFFh
	BA3	8 Kwords	006000h–007FFFh
	BA4	32 Kwords	008000h–00FFFFh
	BA5	32 Kwords	010000h–017FFFh
	BA6	32 Kwords	018000h–01FFFFh
	BA7	32 Kwords	020000h–027FFFh
	BA8	32 Kwords	028000h–02FFFFh
	BA9	32 Kwords	030000h–037FFFh
	BA10	32 Kwords	038000h–03FFFFh
	BA11	32 Kwords	040000h–047FFFh
	BA12	32 Kwords	048000h–04FFFFh
	BA13	32 Kwords	050000h–057FFFh
	BA14	32 Kwords	058000h–05FFFFh
	BA15	32 Kwords	060000h–067FFFh
	BA16	32 Kwords	068000h–06FFFFh
	BA17	32 Kwords	070000h–077FFFh
	BA18	32 Kwords	078000h–07FFFFh
B	BA19	32 Kwords	080000h–087FFFh
	BA20	32 Kwords	088000h–08FFFFh
	BA21	32 Kwords	090000h–097FFFh
	BA22	32 Kwords	098000h–09FFFFh
	BA23	32 Kwords	0A0000h–0A7FFFh
	BA24	32 Kwords	0A8000h–0AFFFFh
	BA25	32 Kwords	0B0000h–0B7FFFh
	BA26	32 Kwords	0B8000h–0BFFFFh
	BA27	32 Kwords	0C0000h–0C7FFFh
	BA28	32 Kwords	0C8000h–0CFFFFh
	BA29	32 Kwords	0D0000h–0D7FFFh
	BA30	32 Kwords	0D8000h–0DFFFFh
	BA31	32 Kwords	0E0000h–0E7FFFh
	BA32	32 Kwords	0E8000h–0EFFFFh
	BA33	32 Kwords	0F0000h–0F7FFFh
	BA34	32 Kwords	0F8000h–0FFFFFh
C	BA35	32 Kwords	100000h–107FFFh
	BA36	32 Kwords	108000h–10FFFFh
	BA37	32 Kwords	110000h–117FFFh
	BA38	32 Kwords	118000h–11FFFFh
	BA39	32 Kwords	120000h–127FFFh
	BA40	32 Kwords	128000h–12FFFFh
	BA41	32 Kwords	130000h–137FFFh
	BA42	32 Kwords	138000h–13FFFFh

Advance Information

TABLE 10: SST34WA32A3/3283, 8 Mbit x4 Concurrent SuperFlash Multi-Bank Memory Organization (2 of 2)

Bank	Block	Block Size	Address Range
	BA43	32 Kwords	140000h–147FFFh
	BA44	32 Kwords	148000h–14FFFFh
	BA45	32 Kwords	150000h–157FFFh
	BA46	32 Kwords	158000h–15FFFFh
	BA47	32 Kwords	160000h–167FFFh
	BA48	32 Kwords	168000h–16FFFFh
	BA49	32 Kwords	170000h–177FFFh
	BA50	32 Kwords	178000h–17FFFFh
D	BA51	32 Kwords	180000h–187FFFh
	BA52	32 Kwords	188000h–18FFFFh
	BA53	32 Kwords	190000h–197FFFh
	BA54	32 Kwords	198000h–19FFFFh
	BA55	32 Kwords	1A0000h–1A7FFFh
	BA56	32 Kwords	1A8000h–1AFFFFh
	BA57	32 Kwords	1B0000h–1B7FFFh
	BA58	32 Kwords	1B8000h–1BFFFFh
	BA59	32 Kwords	1C0000h–1C7FFFh
	BA60	32 Kwords	1C8000h–1CFFFFh
	BA61	32 Kwords	1D0000h–1D7FFFh
	BA62	32 Kwords	1D8000h–1DFFFFh
	BA63	32 Kwords	1E0000h–1E7FFFh
	BA64	32 Kwords	1E8000h–1EFFFFh
	BA65	32 Kwords	1F0000h–1F7FFFh
	BA66	32 Kwords	1F8000h–1FFFFFh

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TABLE 11: SST34WA32A4/3284, 8 Mbit x4 Concurrent SuperFlash Multi-Bank Memory Organization (1 of 2)

Bank	Block	Block Size	Address Range
A	BA0	32 Kwords	000000h–007FFFh
	BA1	32 Kwords	008000h–00FFFFh
	BA2	32 Kwords	010000h–017FFFh
	BA3	32 Kwords	018000h–01FFFFh
	BA4	32 Kwords	020000h–027FFFh
	BA5	32 Kwords	028000h–02FFFFh
	BA6	32 Kwords	030000h–037FFFh
	BA7	32 Kwords	038000h–03FFFFh
	BA8	32 Kwords	040000h–047FFFh
	BA9	32 Kwords	048000h–04FFFFh
	BA10	32 Kwords	050000h–057FFFh
	BA11	32 Kwords	058000h–05FFFFh
	BA12	32 Kwords	060000h–067FFFh
	BA13	32 Kwords	068000h–06FFFFh
	BA14	32 Kwords	070000h–077FFFh
	BA15	32 Kwords	078000h–07FFFFh
B	BA16	32 Kwords	080000h–087FFFh
	BA17	32 Kwords	088000h–08FFFFh
	BA18	32 Kwords	090000h–097FFFh
	BA19	32 Kwords	098000h–09FFFFh
	BA20	32 Kwords	0A0000h–0A7FFFh
	BA21	32 Kwords	0A8000h–0AFFFFh
	BA22	32 Kwords	0B0000h–0B7FFFh
	BA23	32 Kwords	0B8000h–0BFFFFh
	BA24	32 Kwords	0C0000h–0C7FFFh
	BA25	32 Kwords	0C8000h–0CFFFFh
	BA26	32 Kwords	0D0000h–0D7FFFh
	BA27	32 Kwords	0D8000h–0DFFFFh
	BA28	32 Kwords	0E0000h–0E7FFFh
	BA29	32 Kwords	0E8000h–0EFFFFh
	BA30	32 Kwords	0F0000h–0F7FFFh
	BA31	32 Kwords	0F8000h–0FFFFFh
C	BA32	32 Kwords	100000h–107FFFh
	BA33	32 Kwords	108000h–10FFFFh
	BA34	32 Kwords	110000h–117FFFh
	BA35	32 Kwords	118000h–11FFFFh
	BA36	32 Kwords	120000h–127FFFh
	BA37	32 Kwords	128000h–12FFFFh
	BA38	32 Kwords	130000h–137FFFh
	BA39	32 Kwords	138000h–13FFFFh
	BA40	32 Kwords	140000h–147FFFh
	BA41	32 Kwords	148000h–14FFFFh
	BA42	32 Kwords	150000h–157FFFh

Advance Information

TABLE 11: SST34WA32A4/3284, 8 Mbit x4 Concurrent SuperFlash Multi-Bank Memory Organization (2 of 2)

Bank	Block	Block Size	Address Range
	BA43	32 Kwords	158000h–15FFFFh
	BA44	32 Kwords	160000h–167FFFh
	BA45	32 Kwords	168000h–16FFFFh
	BA46	32 Kwords	170000h–177FFFh
	BA47	32 Kwords	178000h–17FFFFh
D	BA48	32 Kwords	180000h–187FFFh
	BA49	32 Kwords	188000h–18FFFFh
	BA50	32 Kwords	190000h–197FFFh
	BA51	32 Kwords	198000h–19FFFFh
	BA52	32 Kwords	1A0000h–1A7FFFh
	BA53	32 Kwords	1A8000h–1AFFFFh
	BA54	32 Kwords	1B0000h–1B7FFFh
	BA55	32 Kwords	1B8000h–1BFFFFh
	BA56	32 Kwords	1C0000h–1C7FFFh
	BA57	32 Kwords	1C8000h–1CFFFFh
	BA58	32 Kwords	1D0000h–1D7FFFh
	BA59	32 Kwords	1D8000h–1DFFFFh
	BA60	32 Kwords	1E0000h–1E7FFFh
	BA61	32 Kwords	1E8000h–1EFFFFh
	BA62	32 Kwords	1F0000h–1F7FFFh
	BA63	8 Kwords	1F8000h–1F9FFFh
	BA64	8 Kwords	1FA000h–1FBFFFh
	BA65	8 Kwords	1FC000h–1FDFFFh
	BA66	8 Kwords	1FE000h–1FFFFFh

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PSRAM

Self-Initialization

On the power-up of the PSRAM, a self-initialization process begins. During the initialization V_{DD} and V_{DDQ} must be simultaneously applied and BES# must remain High. Self-initialization requires 150µs after V_{DD} and V_{DDQ} are stable at or above 1.7V. After completion of the self-initialization, the default settings for the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) are configured and the device is ready for normal operation.

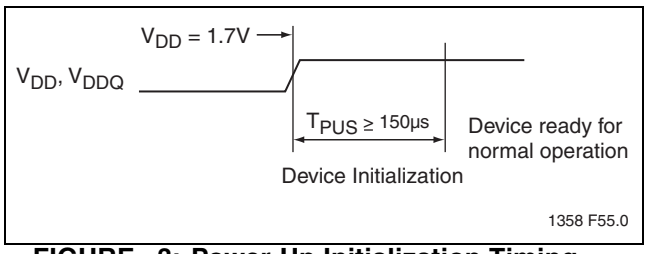


FIGURE 3: Power-Up Initialization Timing

Asynchronous Mode

The device configuration on power-up is Asynchronous Random Read. To read data from the PSRAM memory array, the system must assert a valid address on the multiplexed address/data bus while BES# and AVD# are at V_{IL}. During the read, WE# remains at V_{IH}, the rising edge of AVD# latches the address, and OE# is driven to V_{IL}. The data appears on A/DQ_{15} - A/DQ_0 after T_{BES}.

To write data, drive BES#, WE#, and LBS#/UBS# to V_{IL} while a valid address is asserted on the multiplexed address/data bus. Driving AVD# to V_{IH} latches the address and drives the data onto the bus. OE# is in a “don’t care” state during Asynchronous Random Write mode, and WE# can override OE#. To terminate the Write operation, de-assert BES#, WE#, and LBS#/UBS#. See Table 18 for details of the PSRAM bus operation during Asynchronous mode.

Burst Mode

High-speed, synchronous PSRAM Read and Write are enabled by burst mode operation. The access address latches on the next clock after AVD# and BES# are driven low. Read or Write is indicated by WE# during the first clock rising edge. Fixed-length bursts of 4-, 8-, or 16-words or continuous, bursts are selected in the BCR.

Latency is the number of clock cycles before the initial data is transferred between the processor and the PSRAM, and is set in the BCR. Initial Read latency is configured as either fixed or variable; however, Write latency is always fixed. To achieve minimum latency at high clock frequencies, configure the Burst PSRAM to variable latency. This requires the controller to monitor WAIT for refresh cycle conflicts.

Fixed latency improves performance at lower clock frequencies by sending the first data word after the worst case access delay. Use this feature when the controller cannot monitor the WAIT.

When a burst initiates, WAIT is asserted; and is then de-asserted when data is to be transferred into, or out of, the memory.

Stopping the CLK at High or Low suspends Bursts. While burst is suspended, if another device uses the data bus then OE# must be driven High to disable the outputs. Otherwise, OE# can remain Low. During the burst suspend, WAIT remains active and no other devices can share the WAIT connection to the controller. To resume the burst, drive OE# Low. After valid data is available on the bus, CLK is restarted.

The refresh cycle limits the time that BES# can stay low. If BES# remains Low due to a burst suspend longer than T_{BEPS}, then BES# must be driven High and the burst restarted with BES# Low / AVD# Low cycle. See Table 19 for details of the PSRAM bus operation at Burst mode.

Mixed Mode

Mixed mode combines synchronous Read and Asynchronous Write to seamlessly interface with legacy burst mode flash memory controllers; and is supported when the BCR is configured for synchronous operation. Hold the CLK low for the entire sequence for asynchronous Write. Latch the target address using AVD#. When transitioning between mixed more and fixed latency enabled, BES# can be driven High. BES# Low must not exceed T_{BEPS}.

WAIT

WAIT output connects to the RY/BY# of the SST34WA32A3/32A4/3283/3284 internally. This signal coordinates transactions on the synchronous bus in multiple memory systems.

After Read or Write is initiated, WAIT activates because in burst mode, PSRAM requires additional time before transferring data. For Reads, WAIT is active until valid data is output; for Writes, WAIT indicated when data can be accepted. Data burst progresses on successive rising clock edges when WAIT is inactive. Until the first data is valid, BES# must remain asserted. To prevent data corruption, do not bring BES# High during the initial latency.

If Read launches during an on-chip refresh and when using variable initial access latency (BCR[14] = 0), WAIT

prevents a collision. When a collision occurs, WAIT asserts until the refresh is complete. The Read continues normally once the refresh is complete. During asynchronous Read and Write, ignore asserted WAIT.

Using the PSRAM in burst mode with fixed latency (BCR[14] = 1), does not require WAIT monitoring. WAIT will indicate when valid data is available at the start of the burst and the end of the row. However, when WAIT is not monitored, the controller must stop burst access at the row boundaries.

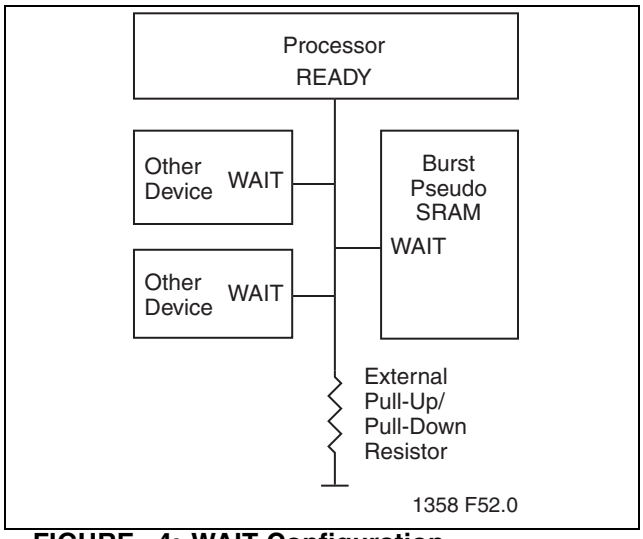


FIGURE 4: WAIT Configuration

LBS#/UBS#

Byte-wide data transfers are accomplished by the LBS# and UBS# enable signals. During Read, enabled bytes are driven to the A/DQs and disabled bytes A/DQs are put into High-Z state. Disabled bytes are not transferred to the RAM during a Write, and their values are unchanged. During asynchronous Write, data is latched on the rising edge of the first occurrence of either BES#, WE#, or LBS#/UBS#. The data bus will not receive or transmit data when both LBS# and UBS# are disabled (High) during an operation; however, as long as BES# remains Low, the device remains in active mode.

Standby Mode

After the completion of a Read or Write, or when the address and control inputs are static for an extended period, the PSRAM enters Standby mode when BES# is driven High. In Standby, power consumption are reduced to a level necessary to perform DRAM refresh. Standby continues until a change in address or PSRAM control input occurs.

Temperature Compensated Refresh

An on-chip temperature sensor automatically regulates the refresh rate according to the operating temperature. The Temperature compensated refresh (TCR) continually adjusts the refresh rate and ensures that sufficient refreshes occur at various temperatures.

Deep Power-Down

If the system does not require the storage provided by the PSRAM, Deep Power-down (DPD) disables all refresh related activities; however, DPD will corrupt any stored data. After re-enabling the refresh activity, the device requires 150 µs to initialize before normal operations resume. During this time, the current consumption is higher than during specified standby levels, but considerably lower than the active current specification. To enable DPD, Write to the RCR using CRES or the software access sequence. DPD starts when BES# is driven High; and is disabled the next time BES# is driven Low and remains for at least 10ns.

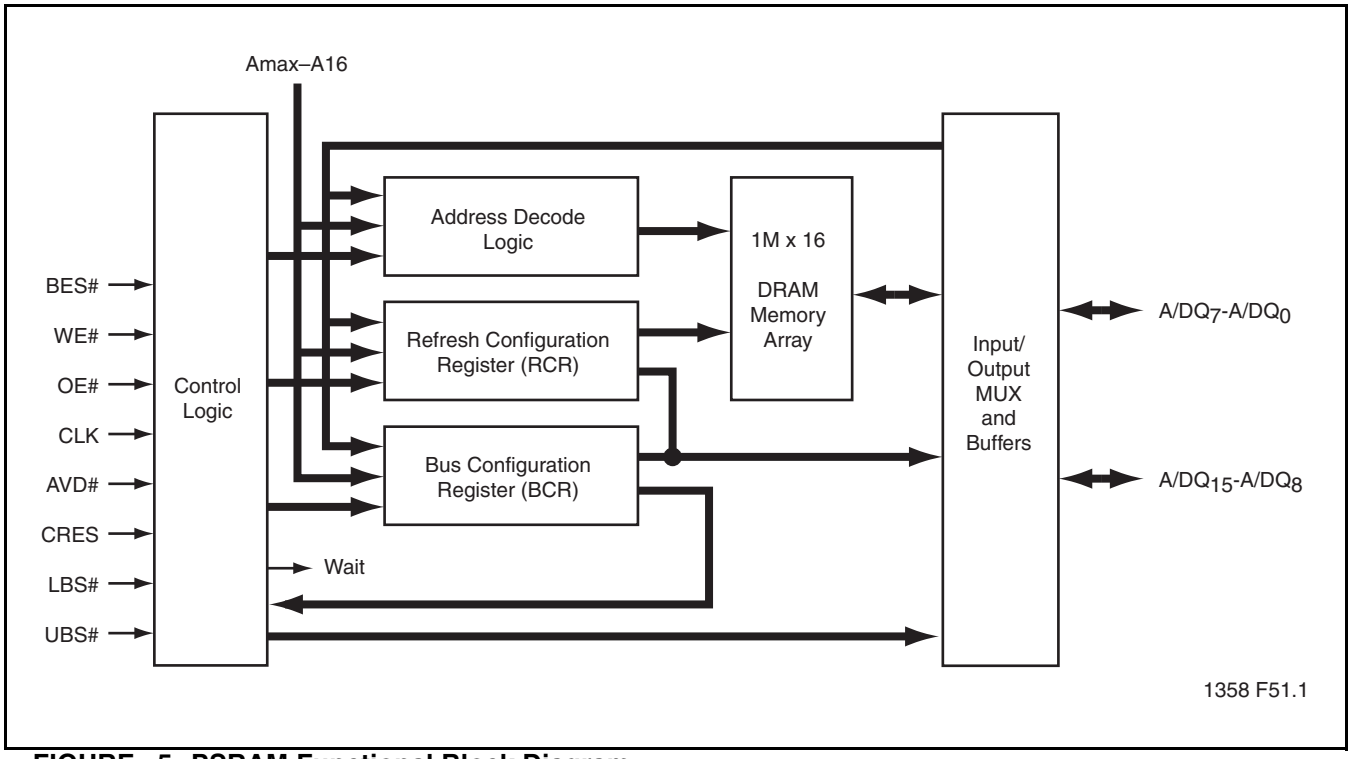


FIGURE 5: PSRAM Functional Block Diagram

PSRAM Configuration Registers

The SST34WA32A3/32A4/3283/3284 features two PSRAM configuration registers: Bus Configuration Register (BCR) and Refresh Configuration Register (RCR).

Register Read/Program using CRES

When the control register enable (CRES) input is High, access the registers in either asynchronous or synchronous mode. When CRES is Low, access the PSRAM array with either a Read or Write operation.

Values are written to the configuration registers using addresses A_{max} - A_0. During synchronous Write, LBS# and UBS# are Don't Care and values are latched on the rising edge of either AVD#, BES#, or WE#, depending on which occurs first. In SST34WA32A3/32A4, when A_{19} - A_{18} are 10b, BCR is accessed; when A_{19} - A_{18} are 00b, RCR is accessed and A_{17}-A_{16} must be set to 0. In SST34WA3283/3284, when A_{18}-A_{17} are 00b, RCR is accessed; when A18-A17 are 01b, BCR is accessed and A_{16} must be set to 0.

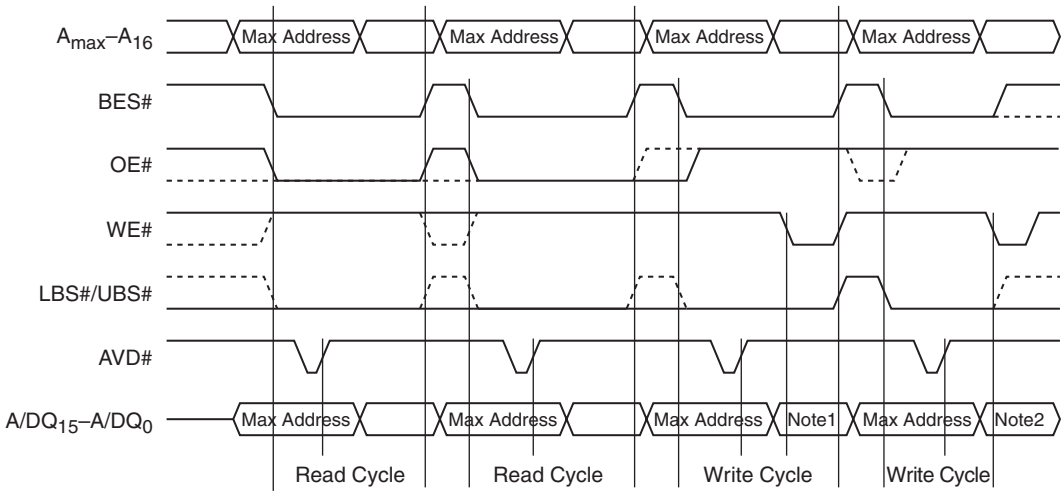
During reads, register bits 15 to 0 are output on A/DQ_{15-0} and address inputs other than A_{19} - A_{18} for SST34WA32A3/32A4, and A_{18} - A_{17} for SST34WA3283/3284, are Don't Care. On completion of a Read or Write operation on a register, immediately execute Read on the memory array. A_{17} - A_{16} must be Low during a register Read or Program using CRES.

Register Read/Program using Software Method

Do not use the software method to disable or enable the Deep Power-down mode (bit 4 of the RCR). To Read and Program the BCR and RCR, first issue a Read Configuration Register sequence and then issue a Set Configuration Register sequence, while CRES is Don't Care. Both the Read Configuration Register sequence and the Set Configuration sequence require four read and write cycles which are performed in asynchronous mode.

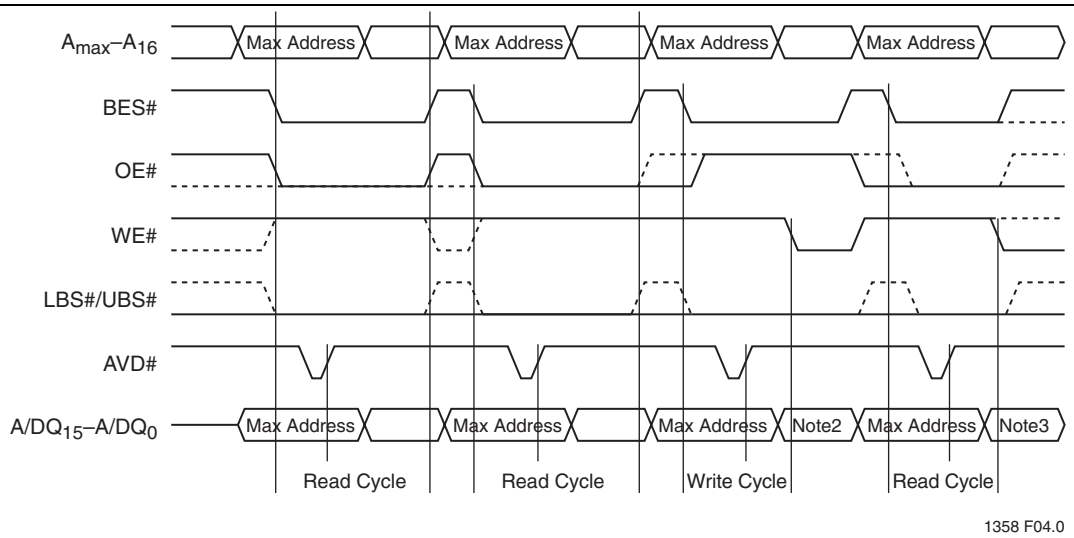
Two bus read cycles followed by one write cycle to the Max address—a unique address location—indicates whether the next operation is a read or write. During the third cycle, write 000h to access RCR and 001h to access BCR, in the next cycle. The configuration register is written to, or read from, during the fourth cycle.

Software Read/Program timings are identical to asynchronous write and read timings.



1. To program the BCR or the RCR on last bus write cycle, A/DQ_{15}–A/DQ_0 must be set to '0001h' and '0000' respectively.
2. Configuration Data In: Only the Bus Configuration Register(BCR) and the Refresh Configuration Register (RCR) can be modified.
3. The control signals BES#, OE#, WE#, LBS# and UBS#, must be toggled as shown in the above figure.

FIGURE 6: Set Configuration Register - Software Method



1. The highest order address location is not modified during this operation.
2. To read the BCR, the RCR, on last bus read cycle, A/DQ_{15}–A/DQ_0 must be set to '0001h' and '0000h' respectively.
3. Configuration Data Out.
4. The control signals BES#, OE#, WE#, LBS# and UBS#, must be toggled as shown in the above figure.

FIGURE 7: Read Configuration Register - Software Method

TABLE 12: Bus Configuration Register

A/DQ15	A/DQ14	A/DQ[13:11]	A/DQ10	A/DQ9	A/DQ8	A/DQ[7:6]	A/DQ[5:4]	A/DQ[3]	A/DQ[2:0]
Operating Mode	Initial Latency	Latency Counter	WAIT Polarity	Reserved	WC	Reserved	Drive Strength	BW[1]	BL[1]

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1. Burst wrap and length apply to both READ and WRITE operations.

Symbol	Function
Operating Mode	Operating Mode 0: Synchronous Burst Access Mode 1: Asynchronous Access Mode (default)
Initial Latency	Initial Access Latency 0: Variable (default) 1: Fixed
Latency Counter	Latency Counter 000b: Reserved 001b: Reserved 010b: Code 2 011b: Code 3 (default) 100b: Reserved 101b: Reserved 110b: Reserved 111b: Reserved
WAIT Polarity	WAIT Polarity 0: Active LOW 1: Active HIGH (default)
WC	WAIT Configuration 0: Asserted during delay 1: Asserted one data cycle before delay (default)
Drive Strength	Output Impedance 00b: Full Drive (default) 01b: Reserved 10b: 1/4 11b: Reserved
BW	Burst Wrap 0: Burst wraps within the burst length 1: Burst no wrap (default)
BL	Burst Length 001b: 4 words 010b: 8 words 011b: 16 words 111b: Continuous burst (default) Others: Reserved
Reserved	Must be set to “0”

TABLE 13: Refresh Configuration Register Mapping

A/DQ[15:5]	A/DQ4	A/DQ[3:0]
Reserved	DPD	Reserved

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Symbol	Function
DPD	Deep Power Down 0: DPD Enable 1: DPD Disable (default)
Reserved	Must be set to '0'

TABLE 14: Sequence and Burst Length

Burst Wrap		Starting Address	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	Continuous Burst
BCR[3]	Wrap	Decimal	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-...
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-...
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-...
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-...
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-...
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-...
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-...
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-...
		...			...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21-...
		...				...
		30				30-31-32-33-34-...
		31				31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-...
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-...
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-...
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-...
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-...
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20	5-6-7-8-9-10-11-...
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-21	6-7-8-9-10-11-12-...
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7-8-9-10-11-12-13-...
		...			...	...
		14			14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29	14-15-16-17-18-19-20-...
		15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-18-19-20-21-...
		...				...
		30				30-31-32-33-34-35-36-...
		31				31-32-33-34-35-36-37-...

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PIN DESCRIPTION

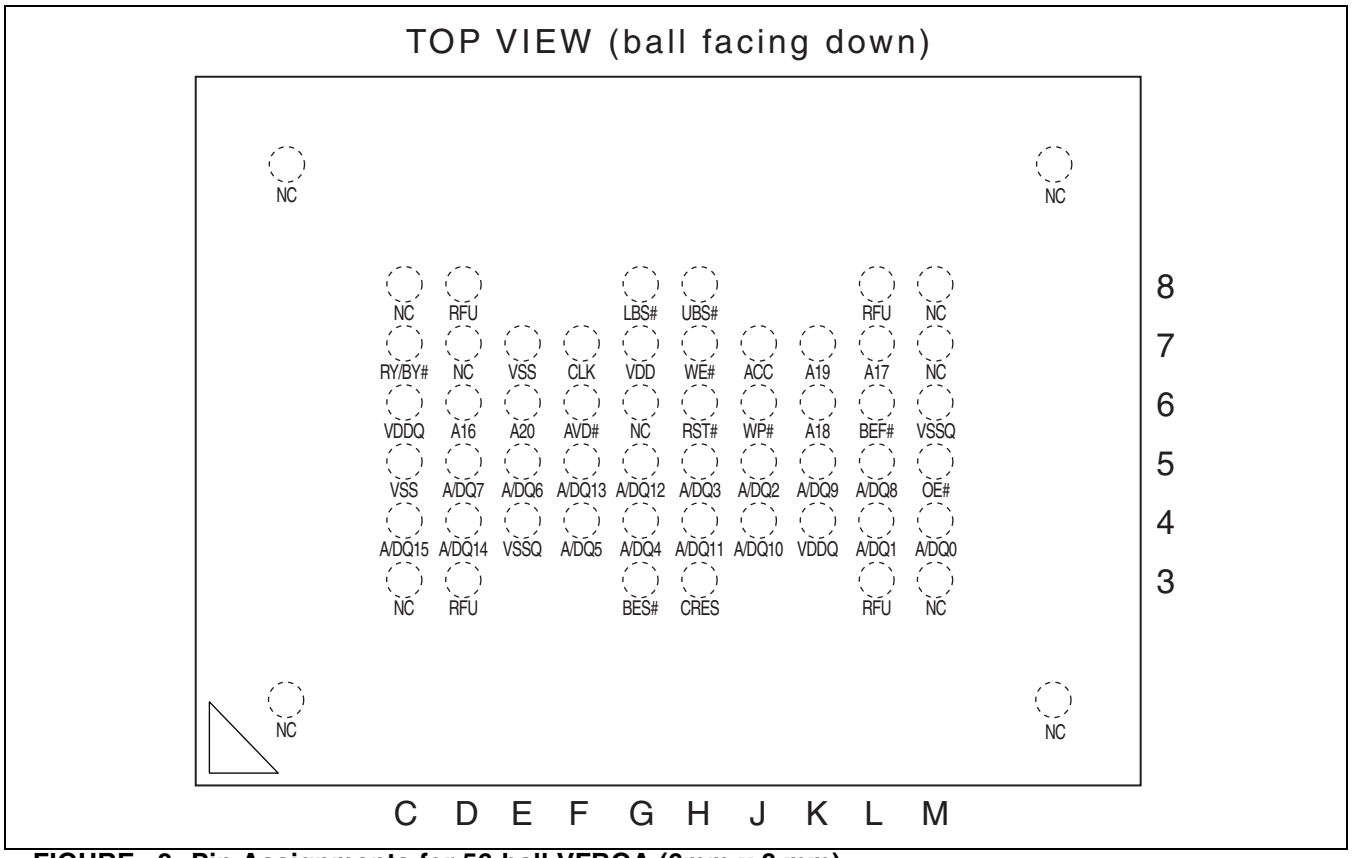

FIGURE 8: Pin Assignments for 56-ball VFBGA (6mm x 8 mm)

TABLE 15: Pin Descriptions

Symbol	Name	Functions
A_{20} -A_{16}	Address Inputs	To provide memory addresses.
A/DQ_{15}-A/DQ_0	Multiplexed Address/Data	Sixteen least-significant bit Addresses are multiplexed with Data Input/output. The outputs are in tri-state when OE# or BEF# is high.
BEF#	Flash Memory Enable	To activate the flash memory bank when BEF# is low.
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
RST#	Hardware Reset	To reset and return the flash memory to Read mode
RY/BY#	Ready Output	RY/BY# signal when the Flash memory is selected. WAIT signal when the PSRAM is selected.
CLK	Clock	To increment the internal address counter (after the initial output delay) when the part is in Burst Mode. CLK is not required in asynchronous mode.
AVD#	Address Valid Input	To indicate to the device that a valid Address is present on the Address Bus
WP#	Write Protect	To protect and unprotect top or bottom 8 KWord (4 outermost sectors) of the flash memory bank from Erase or Program operation.
A_{CC}	Vpp Power Supply	Supervoltage VH (11.4V to 12V) input to enable eight word programming of the flash memory bank. When at V_{IL} locks all sectors. Should be at V_{IH} for all other conditions.
V_{DDQ}	I/O Power Supply	To provide power for Input/Output Buffers.
V_{DD}	Power Supply	To provide 1.7-1.95V power supply voltage. V_{DD} and V_{DDQ} need to be shorted together in the application circuit.
V_{SS}	Ground	
V_{SSQ}	Ground for I/O Power Supply	V_{SS} and V_{SSQ} need to be shorted together in the application circuit.
NC	No Connection	Unconnected pins
RFU	Reserve for future use	Don't make any connection on these pins.
CRES	Configuration Register Enable (PSRAM)	When CRE is high, Write operations load the Refresh configuration register, Bus configuration register or Device ID register.
BES#	PSRAM Memory Enable	Activate the PSRAM when low.
LBS#	Lower Byte Control (PSRAM)	Gates the data on the lower byte of the data bus during a write operation or Data gated from the lower part of the selected address during a read operation.
UBS#	Upper Byte Control (PSRAM)	Gates the data on the upper byte of the data bus during a write operation or Data gated from the upper part of the selected address during a read operation.

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TABLE 16: Flash Operation Mode Selection

Mode	BEF#[1]	OE#	WE#	AVD#	CLK[2]	A/DQ15-0	A_{20-16}	RST#
Asynchronous Read	V_{IL}	V_{IL}	V_{IH}	Pulse Low	X[3]	I/O	AIN	V_{IH}
Program	V_{IL}	V_{IH}	V_{IL}	Pulse Low	X	I/O	AIN	V_{IH}
Erase	V_{IL}	V_{IH}	V_{IL}	Pulse Low	X	I/O	Sector or block address, XXH[2] for Chip-Erase	V_{IH}
Standby	V_{IH}	X	X	X	X	High Z	X	V_{IH}
Write Inhibit	X	V_{IL}	X	X	X	I/O/ DOUT	X	V_{IH}
	X	X	V_{IH}	X	X	High Z / DOUT	X	V_{IH}
Hardware Reset	X	X	X	X	X	High Z	X	V_{IL}
Product Identification Mode (Manufacturer)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Manufacturer's ID (00BFH)	See Table 9	See Table 9
Product Identification Mode (Device)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Device ID[4] (xxxxH)	See Table 9	See Table 9

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1. BEF# and BES# cannot be low at the same time.
2. Default Clock Active edge is the rising edge.
3. X can be V_{IL} or V_{IH}, but no other value.
4. Device ID for SST34WA32x3 is 975BH and for SST34WA32x4 is 975AH.

TABLE 17: Flash Burst Mode Selection

Mode	BEF#[1]	OE#	WE#	AVD#	CLK	DQ	Address	RST#
Load Starting Burst Address	V_{IL}	V_{IH}	V_{IH}	Pulse Low	Active Edge	X[2]	AIN	V_{IH}
Automatic Address Advance during Burst Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Active Edge	DOUT	X	V_{IH}
Terminate Current Burst Read (with BEF#)	V_{IH}	X	V_{IH}	X	Active Edge	High Z	X	V_{IH}
Terminate Current Burst Read with RST#	X	X	V_{IH}	X	X	High Z	X	V_{IL}
Terminate Current Burst Read and Start a New Burst Read	V_{IL}	V_{IH}	V_{IH}	Pulse Low	Active Edge	High Z / X	AIN	V_{IH}
Burst Suspend	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	High Z	X	V_{IH}

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1. BEF# and BES# cannot be low at the same time.
2. X can be V_{IL} or V_{IH}, but no other value.

TABLE 18: PSRAM Operation Mode Selection - Asynchronous

Mode[1]	BES#[2]	AVD#	WE#	OE#	UBS#	LBS#	CRES	Amax -16	A/DQ7-0	A/DQ15-8
Word Read	V_{IL}	Assert going low	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address in Valid	Address in/Data out Valid	
Lower Byte Read				V_{IL}	V_{IH}	V_{IL}	V_{IL}	Address in Valid	Address in/ Data out Valid	High-Z
Upper Byte Read				V_{IL}	V_{IL}	V_{IH}	V_{IL}	Address in Valid	High-Z	Address in/ Data out Valid
Word Write			V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Address in Valid	Address in/Data out Valid	
Lower Byte Write				V_{IH}	V_{IH}	V_{IL}	V_{IL}	Address in Valid	Address in/ Data out Valid	Data in Valid
Upper Byte Write				V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address in Valid	Data in Valid	Address in/ Data in Valid
Output Disable/ No Operation	V_{IL}	X	V_{IH}	V_{IH}	X	X	V_{IL}	X	High-Z	
Deep Power-Down[3]	V_{IH}	X	X	X	X	X	X	X	High-Z	
Standby	V_{IH}		X	X	X	X	X	X	High-Z	

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1. The clock signal (CLK) must remain low in asynchronous operating mode.
2. BEF# and BES# cannot be low at the same time.
3. The device enters Deep Power-Down mode by driving the chip Enable Signal, BES#, from Low to High with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until BES# goes Low again and is held Low for TCW. The Device is reading and programming the registers use CRES controlled method or the software method.

TABLE 19: PSRAM Bus Operation - Burst Mode

Mode	CLK[1]	BES#[2]	AVD#	WE#	OE#	UBS#/ LBS#	WAIT	CRES	Amax -16	A/DQ10-0
Initial Burst Read	rising	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Low-Z	V_{IL}	Address in Valid	Address in Valid
Subsequent Burst Read	rising	V_{IL}	V_{IH}	X	X	V_{IL}			X	Data out Valid
Initial Burst Write	rising	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			Address in Valid	Address in Valid
Subsequent Burst Write	rising	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}			X	Data in Valid
No Operation	rising	V_{IL}	X	V_{IH}	V_{IH}	X		V_{IL}	X	High-Z
Standby	V_{IL}	V_{IH}	X	X	X	X	High-Z	V_{IL}	X	High-Z
Deep Power-Down	V_{IL}	V_{IH}	X	X	X	X		X	X	High-Z

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1. The Configuration Register is output during the initial burst operation (read or write). The following read or write operations are similar to subsequent burst operations. BES# must be held Low for the equivalent of a single-word burst operation
2. BEF# and BES# cannot be low at the same time.

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TABLE 20: Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Word-Program	555H	AAH	2AAH	55H	555H	A0H	WA[3]	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA_X[4]	50H
Block-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA_X[4]	30H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Suspend	XXXH	B0H										
Resume	XXXH	30H										
Block Lock/ Unlock[5]	XXXH	60H	XXXH	60H	BLA_X[6]	60H						
Read Block Locking Register	555H	AAH	2AAH	55H	BK_X555H[4]	90H	See Table 22	See Table 22				
Entry/Query Security ID[7]	555H	AAH	2AAH	55H	555H	88H						
User Security ID Program	555H	AAH	2AAH	55H	555H	A5H	SIWA[8]	Data				
User Security ID Program Lock-Out	555H	AAH	2AAH	55H	555H	85H	XX	0000H				
Software ID Entry[9, 10]	555H	AAH	2AAH	55H	BK_X555H	90H	See Table 22	See Table 22				
CFI Query Entry	BK_X55H	98H										
Software ID Exit[11]/CFI Exit/ Sec ID Exit	XXH	F0H										
CFI Query Entry (3 cycles)	555H	AAH	2AAH	55H	BK_X555H	98H						
Software ID Exit/ CFI Exit/ Security ID Exit (3 cycles)	555H	AAH	2AAH	55H	555H	F0H						
Set Burst Mode Configuration Register	555H	AAH	2AAH	55H	CR_X555H[12]	C0H						
Eight Word Program	XXH	A0H[13]	See Table 21 for Bus Cycle Seq.	See Table 21 for Bus Cycle Seq.								
Programming Acceleration Mode Entry	555H	AAH	2AAH	55H	555H	20H						
Programming Acceleration Program[14]	XXH	A0H	WA	Data								
Programming Acceleration Program Reset[15]	XXH	90H	XXH	00H								

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1. Address format A_{11}-A_0 (Hex)
   Addresses A_{12}-A_{20} can be V_{IL} or V_{IH}, but no other value, for Command sequence of SST34WA32A3/32A4/3283/3284.

2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for Command sequence
3. WA = Program Word address.
4. SA_X for Sector-Erase; uses A_{20}-A_{11} address lines
   BA_X for Block-Erase; uses A_{20}-A_{13} address lines
5. BLR indicates Block Locking Register Data: 0000H = Block Unlocked, 0001H = Block Locked.
6. BLA_X indicates the Address of the Block to be Locked/Unlocked; uses A_{20} -A_{13} address lines.
   This is composed by the Block Address (BA) and either A_6 = 1 to Unlock or A_6 = 0 to Lock.
7. With A_{20}-A_8 = 0; Security ID information is read with A_7-A_0
   SST Factory Unique Id is read at Address Range: 000000H to 000007H (128-bit). This segment is always locked by SST.
   User ID is read at Address range: 000080H to 0000FFH (128-words).
   Lock Status of User Segment is read with A_7 to A_0 = 00007FH. Unlocked: DQ_3 = 1 / Locked: DQ_3 = 0.
8. SIWA: Security ID Program Word Address: User ID can be written at Address range: 000080H to 0000FFH (128-words).
9. The device does not remain in Software Product Identification mode if Powered Down.
10. With A_{18}-A_1 =0 and A_{20}-A_{19} = BK (Bank Address), address of the Bank that is being switched to Software ID Mode:
    SST Manufacturer ID = 00BFH, is read with A1 = 0 and A0 = 0
    SST34WA32x3 Device ID = 975BH, is read with A1 = 0 and A0 = 1
    SST34WA32x4 Device ID = 975AH, is read with A1 = 0 and A0 = 1
11. Both Software ID Exit operations are equivalent.
12. CR = Burst Mode Configuration Register Value on A_{17}-A_{12} (see Programmable WAIT State Configuration Section).
13. Eight Word Program command can only be executed if ACC is at the Supervoltage VH. ACC must be at the Supervoltage VH before the “A0H” command is issued in order to enable the Eight Words Program Command.
14. The Programming Acceleration command sequence is required prior to this command sequence.
15. The Programming Acceleration Reset command is required to return to normal read mode when the chip is in the Programming Acceleration mode.

TABLE 21: Eight Word Program Software Command Sequence

Bus Cycle	Address[1]	Data[2]	Comment
1	XXXXH[3]	A0H	Eight Word Program Command
2	WA[4]	DATA A	Will program “DATA A” at Address WA
3	XXXXH	DATA B	Will program “DATA B” at Address WA + 1
4	XXXXH	DATA C	Will program “DATA C” at Address WA +2
5	XXXXH	DATA D	Will program “DATA D” at Address WA +3
6	XXXXH	DATA E	Will program “DATA E” at Address WA +4
7	XXXXH	DATA F	Will program “DATA F” at Address WA +5
8	XXXXH	DATA G	Will program “DATA G” at Address WA +6
9	XXXXH	DATA H	Will program “DATA H” at Address WA +7

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1. Address format A_{11}-A_0 (Hex).
   Addresses A_{12}- A_{20} can be V_{IL} or V_{IH}, but no other value, for Command sequence of SST34WA32A3/32A4/3283/3284.
2. DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, for Command sequence.
3. X can be V_{IL} or V_{IH}, but no other value.
4. WA: Program Word Address of first word to be programmed. In Eight-Word Program Mode WA must be 8-word boundary aligned (A_0=A_1=A_2=0).

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TABLE 22: Software ID and Read Block Locking Registers

Command Sequence	1st Bus Cycle (Write)		2nd Bus Cycle (Write)		3rd Bus Cycle (Write)		4th Bus Cycle (Read)	
	Addr[1]	Data[2]	Addr	Data	Addr	Data	Addr	Data
Software ID Entry: Manufacturer ID	555H	AAH	2AAH	55H	BK_X555H[3]	90H	BK_XX00	00BFH
Software Id Entry: Device ID	555H	AAH	2AAH	55H	BK_X555H	90H	BK_XX01	xxxxH[4]
Software Id Entry: Read Block Locking Status	555H	AAH	2AAH	55H	BK_X555H[3]	90H	BA_XX02	BLR[5]

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1. Address format A_{11}-A_0 (Hex).
   Addresses A_{12}-A_{20} can be V_{IL} or V_{IH}, but no other value, for Command sequence of SST34WA32A3/32A4/3283/3284.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for Command sequence.
3. BKX indicates the Bank Address: uses A_{20}-A_{19} address lines.
   BAX indicates the Address of the Block to be Locked/Unlocked; uses A_{20}-A_{13} address lines.
   This is composed by the Block Address (BAX).
4. SST34WA32x3 is 975BH and for SST34WA32x4 is 975AH
5. BLR indicates Block Locking Register Data: 0000H = Block Unlocked, 0001H = Block Locked.

TABLE 23: CFI Query Identification String[1]

Address	Data	Description
10H	0051H	Query Unique ASCII string “QRY”
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set
14H	0007H	
15H	0040H	Address for Primary Extended Table
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	0000H	

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1. Refer to CFI publication 100 for more details.

TABLE 24: System Interface Information

Address	Data	Description
1BH	0017H	V_{DD} min (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1CH	0019H	V_{DD} max (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1DH	00B4H	ACC min (00H = no ACC pin)
1EH	00C0H	ACC max (00H = no ACC pin)
1FH	0003H	Typical time out for Word-Program 2^N µs (2^3 = 8 µs)
20H	0000H	Typical time out for min size buffer program 2^N µs (00H = not supported)
21H	0004H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	0005H	Typical time out for Chip-Erase 2^N ms (2^5 = 32 ms)
23H	0001H	Maximum time out for Word-Program 2^N times typical (2^1 x 2^3 = 16 µs)
24H	0000H	Maximum time out for buffer program 2^N times typical
25H	0001H	Maximum time out for individual Sector/Block-Erase 2^N times typical (2^1 x 2^4 = 32 ms)
26H	0001H	Maximum time out for Chip-Erase 2^N times typical (2^1 x 2^5 = 64 ms)

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TABLE 25: Device Geometry Information - SST34WA32x3

Address	Data	Description
27H	0016H	Device size = 2^N Bytes (16H = 22; 2^{22} = 4 MByte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	Maximum number of bytes in multi-byte write = 2^N(00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Block sizes supported by device
2DH	0003H	Block Information (y + 1 = Number of blocks; z x 256B = block size)
2EH	0000H	y = 03H + 1 = 4 blocks
2FH	0040H	
30H	0000H	z = 40H x 256 Bytes = 16 KBytes/block
31H	003EH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	0000H	y = 3EH + 1 = 63 blocks
33H	0000H	
34H	0001H	z = 100H x 256 Bytes = 64 KByte/block
35H	0000H	
36H	0000H	
37H	0000H	
38H	0000H	
39H	0000H	
3AH	0000H	
3BH	0000H	
3CH	0000H	

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TABLE 26: Device Geometry Information - SST34WA32x4

Address	Data	Description
27H	0016H	Device size = 2^N Bytes (16H = 22; 2^{22} = 4 MByte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	Maximum number of bytes in multi-byte write = 2^N(00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Block sizes supported by device
2DH	003EH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
2EH	0000H	y = 3EH + 1 = 63 blocks
2FH	0000H	
30H	0001H	z = 100H x 256 Bytes = 64 KByte/block
31H	0003H	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	0000H	y = 03H + 1 = 4 blocks
33H	0040H	
34H	0000H	z = 40H x 256 Bytes = 16 KBytes/block
35H	0000H	
36H	0000H	
37H	0000H	
38H	0000H	
39H	0000H	
3AH	0000H	
3BH	0000H	
3CH	0000H	

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TABLE 27: Primary Vendor-Specific Extended Query

Address	Data	Description
40H	0050H	Query Unique ASCII string “PRI”
41H	0052H	
42H	0049H	
43H	0031H	Major version number, ASCII
44H	0033H	Minor version number, ASCII
45H	0005H	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0001 = 0.18 µm
46H	0002H	Erase-Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47H	0001H	Block Protect 0 = Not Supported, X = Number of blocks in per group
48H	0000H	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49H	0005H	Sector Protect/Unprotect scheme 00 = Not Supported, 01 = Supported
4AH	0018H	Simultaneous Operation Number of Sectors in all banks except boot bank
4BH	0001H	Burst Mode Type 00 = Not Supported, 01 = Supported
4CH	0000H	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4DH	00B4H	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4EH	00C0H	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4FH	00XXH	Top/Bottom Boot Sector Flag 01h = Bottom Boot Device, 02h = Top Boot Device
50H	0000H	Program Suspend. 00h = not supported
57H	0004H	Bank Organization: X = Number of banks
58H	0013H (SST34WA32x3) 0010H (SST34WA32x4)	Bank A Region Information. X = Number of blocks in bank
59H	0010H	Bank B Region Information. X = Number of blocks in bank
5AH	0010H	Bank C Region Information. X = Number of blocks in bank
5BH	0010H (SST34WA32x3) 0013H (SST34WA32x4)	Bank D Region Information. X = Number of blocks in bank

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Advance Information

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on ACC Pin to Ground Potential . . . . . -0.5V to +14V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{DD}
Extended	-20°C to +85°C	1.7V-1.95V

AC Conditions of Test

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 43 and 44	

DC Characteristics

TABLE 28: DC Operating Characteristics V_{DD} = 1.7-1.95V

Symbol	Parameter	Freq	Limits			Test Conditions
			Min	Max	Units	
I_{DD}	Flash Asynchronous Read	5 MHz		10	mA	BEF#=V_{IL}, OE#=WE#=V_{IH}, Array background is 55AAH
	PSRAM Asynchronous Read/Write			20	mA	BEF#=V_{IH}, BES#=V_{IL}
	Program and Erase			40	mA	BEF#=WE#=V_{IL}, OE#=A_{CC}=V_{IH}
	Concurrent Read/Write			60	mA	BEF#=V_{IL}, OE#=V_{IH}
I_{DDB}	Flash Active V_{DD} Burst Read Current	54 MHz		30	mA	BEF#=V_{IL}, OE#=V_{IH}, WE#=V_{IH}, Array background is 55AAH
	PSRAM Initial Access, Burst Read/Write			25	mA	BEF#=V_{IH}, BES#=V_{IL}, OE# = V_{IH}, Array background is 0H
	PSRAM Continuous Burst Write			30	mA	BEF#=V_{IH}, BES#=V_{IL}, WE#=V_{IL}, OE# = V_{IH}
I_{SB}	Standby V_{DD} Current			120	µA	BEF#= V_{DD} -0.1V BES# = V_{DD}-0.1V RST#= V_{DD} -0.1V All other inputs= 0.1V or V_{DD}-0.1V
I_{LI}	Input Leakage Current			1	µA	V_{IN} =GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			1	µA	V_{OUT} =GND to V_{DD}, V_{DD}=V_{DD} Max
I_H	Supervoltage Current for ACC Eight-Word Program			10	mA	V_{DD}=V_{DD} Max, A_{CC}=V_H Max
V_{IL}	Input Low Voltage			0.4	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage		V_{DD} - 0.4		V	V_{DD}=V_{DD} Max
V_{OLF}	Flash Output Low Voltage			0.1	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OHF}	Flash Output High Voltage		V_{DD}-0.1		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min
V_{OLS}	PSRAM Output Low Voltage			0.2V_{DD}	V	I_{OL}=0.2 mA, V_{DD}=V_{DD} Min, BCR[5:4]=01b
V_{OHS}	PSRAM Output High Voltage		0.8V_{DD}		V	I_{OH}=-0.2 mA, V_{DD}=V_{DD} Min, BCR[5:4]=01b
V_H	Supervoltage for ACC Eight-Word Program		11.4	12	V	V_{DD} = 1.8V
V_{LKO}	Flash Low V_{DD} Lock-Out Voltage		1.0	1.4	V	

T28.0 1358

TABLE 29: Capacitance (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	10 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10 pF

T29.0 1358

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 30: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

TABLE 30: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 31: Flash Synchronous/Burst Read (54MHz/66MHz) Cycle Timing Parameters V_{DD} = 1.7-1.95V[1]

Symbol	Parameter	54 MHz		66 MHz		Units
		Min	Max	Min	Max	
T_{IACC}	Initial Access time		87.5		70	ns
T_{BACC}	Burst Access Time, Valid Clock to Output Delay		13.5		11.5	ns
T_{ACS}	Address Setup Time to CLK[2]	5		4		ns
T_{ACH}	Address Hold Time from CLK[2]	7		6		ns
T_{BDH}	Data Hold Time from Next Clock Cycle	3		3		ns
T_{OE}	OE# to Data Valid (OE# to RY/BY# Valid)		13.5		11.5	ns
T_{CEZ}	BEF# to High-Z		10		10	ns
T_{OEZ}	OE# to High-Z		10		10	ns
T_{CES}	BEF# Setup Time to CLK	5		4		
T_{RACC}	RY/BY# Access Time from CLK		13.5		11.5	ns
$T_{RY/BY\#S}$	RY/BY# Setup Time to CLK	5		4		ns
T_{AVDS}	AVD# setup time to CLK	5		5		ns
T_{AVDH}	AVD# hold time from CLK	7		6		ns
T_{AVDO}	AVD# High to OE# Low	7		6		ns
T_{CKA}	CLK to Access Resume		13.5		11.5	ns
T_{OECH}	OE# Hold time from CLK for burst-suspend	5		4		ns
T_{AAH}	Address Hold Time from Rising Edge of AVD#	7		6		ns

T31.1358

1. Not 100% tested.
2. Test Conditions:
   Output Load: V_{DD}: 30pF
   Input Pulse Levels: 0.0V to V_{DD}
   Input: 0.5 x V_{DD}
   Input Rise and Fall Times: 5ns
   Timing measurements reference level
   Output: 0.5 x V_{DD}

TABLE 32: Flash Asynchronous Read Cycle Timing Parameters V_{DD} = 1.7-1.95V

Symbol	Parameter	54 MHz		66 MHz		Units
		Min	Max	Min	Max	
T_{CE}	Access Time from BEF# Low		70		70	ns
T_{ACC}	Asynchronous Access Time[1]		70		70	ns
T_{AVDP}	AVD# Low Time	12		11		ns
T_{AAS}	Address Setup Time to Rising Edge of AVD#	5		4		ns
T_{AAH}	Address Hold Time from Rising Edge of AVD#	7		6		ns
T_{OE}	OE# to Data Valid		13.5		11.5	ns
T_{OEH}	Output Enable Hold Time from WE# high (Read Operation)	0		0		ns
	Output Enable Hold Time from WE# high (Toggle and Data Poll)	10		10		ns
T_{OEZ}	Output Enable to High-Z[2]		10		10	ns
T_{CEZ}	BEF# to High-Z[2]		10		10	ns

T32.0 1358

1. Asynchronous Access Time is from the last of either stable addresses or the falling edge of AVD#
2. Not 100% tested

TABLE 33: PSRAM Asynchronous Read Cycle Timing Parameters[1] V_{DD} = 1.7-1.95V

Symbol	Parameter	Min	Max	Units
T_{ACCS}	Address Access time		70	ns
T_{AAVDS}	AVD# Access Time		70	ns
T_{AAHS}	Address Hold from AVD# High	2		ns
T_{AASS}	Address Setup to AVD# High	10		ns
T_{BYAS}	LBS#/UBS# Access Time		70	ns
T_{BYHZS}	LBS#/UBS# Disable to A/DQ High-z		8	ns
T_{BYLZS}	LBS#/UBS# Enable to Low-z Output	10		ns
T_{BEPS}	BES# Low Pulse Width		10	µs
T_{BEWS}	BES# Low to WAIT Valid	1	7.5	ns
T_{BES}	BES# Access Time		70	ns
T_{BVS}	BES# Low to AVD# HIGH	7		ns
T_{BHZS}	BES# High to A/DQ and WAIT High-z		8	ns
T_{BLZS}	BES# Low to Low-z Output	10		ns
T_{OES}	OE# Low to Valid Output		20	ns
T_{OHZS}	OE# High to A/DQ High-z		8	ns
T_{OLZS}	OE# Low to Low-z Output	3		ns
T_{RCS}	Read Cycle Time	70		ns
T_{VPLS}	AVD# Pulse Width Low	5		ns
T_{VPHS}	AVD# Pulse Width High	10		ns

T33.1358

1. All tests are performed with the outputs configured for the default setting of full drive strength (BCR[5:4]=00B).

TABLE 34: PSRAM Burst Read Cycle Timing Parameters[1] V_{DD} = 1.7-1.95V

Symbol	Parameter	54 MHz		66 MHz		Units
		Min	Max	Min	Max	
T_{ACCS}	Address Access Time (Fixed Latency)		70		70	ns
T_{AAVDS}	AVD# Access Time (Fixed Latency)		70		70	ns
T_{IACCS}	Initial Access Time (Variable Latency)[2]		65		55	ns
T_{BACCS}	Burst Access Time (CLK Output Delay)		11		11	ns
T_{AAHS}	Address Hold from AVD# HIGH (Fixed Latency)	3		2		ns
T_{OES}	OE# LOW to Valid Output		20		20	ns
T_{BPHS}	BES# HIGH between Subsequent Burst or MIxed Model Operations[3]	10		8		ns
T_{BEPS}	BES# Low Pulse Width[3]		10		10	µs
T_{BEWS}	BES# or AVD# LOW to WAIT Valid	1	9	1	7.5	ns
T_{BEAS}	BES# Access Time (Fixed Latency)		70		70	ns
T_{BESS}	BES# Setup Time to Active CLK Edge	7		5		ns
T_{HDS}	Hold Time from Active CLK Edge	3		2		ns
T_{BHZS}	BES# High to A/DQ and WAIT High-Z Output		8		8	ns
T_{CWS}	CLK to WAIT Valid		11		11	ns
T_{BDHS}	Output HOLD from CLK	2		2		ns
T_{OHZS}	OE# High to A/DQ High-Z Output		8		8	ns
T_{OLZS}	OE# Low to Low-Z Output	3		3		ns
T_{SPS}	Setup Time to Active CLK Edge	5		3		ns

T34.0 1358

1. All tests are performed with the outputs configured for the default setting of full drive strength (BCR[5:4]=00B).
2. Values are valid for T_{CLK} (Min.) with no refresh collision.
3. A refresh opportunity must be provided every T_{BEPS}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked BES# HIGH, or b) BES# HIGH for longer than 15ns.

TABLE 35: PSRAM Asynchronous WRITE Cycle Timing Parameters[1] V_{DD} = 1.7-1.95V

Symbol	Parameter	Min	Max	Units
T_{ASTS}	Address Setup Time	0		ns
T_{AAHS}	Address Hold from AVD# HIGH	2		ns
T_{AASS}	Address Setup to AVD# HIGH	10		ns
T_{AWS}	Address Valid to End of Write	70		ns
T_{BYWS}	LBS#/UBS# Select to End of Write	70		ns
T_{BEWS}	BES# or AVD# Low to WAIT Valid	1	7.5	ns
T_{BPHS}	BES# HIGH between Subsequent Asynchronous Operations	6		ns
T_{BVS}	BES# Low to AVD# HIGH	7		ns
T_{BWS}	BES# Low to End of Write	70		ns
T_{DHS}	Data Hold from Write Time	0		ns
T_{DSS}	Data Write Setup Time	20		ns
T_{BHZS}	BES# High to WAIT High-Z Output		8	ns
T_{BLZS}	BES# Low to Low-Z Output	10		ns
T_{OEWS}	End Write to Low-Z Output	5		ns
T_{VPLS}	AVD# Pulse Width Low	5		ns
T_{VPHS}	AVD# Pulse Width High	10		ns

TABLE 35: PSRAM Asynchronous WRITE Cycle Timing Parameters[1] V_{DD} = 1.7-1.95V

Symbol	Parameter	Min	Max	Units
T_{VWS}	AVD# Setup to End of Write	70		ns
T_{WCS}	Write Cycle Time	70		ns
T_{ODWS}	Write to A/DQ High-Z Output		8	ns
T_{WPLS}	Write Pulse Width Low[2]	45		ns
T_{WPHS}	Write Pulse Width High	10		ns
T_{WRS}	Write Recovery Time	0		ns
T_{AWS}	AVD# High to Write Enable Low	0		ns

T35.0 1358

1. All tests are performed with the outputs configured for the default setting of full drive strength (BCR[5:4]=00B).
2. WE# LOW time must be limited from T_{BPHS} to T_{BEPS} (10µs)

TABLE 36: PSRAM Burst WRITE Cycle Timing Parameters[1] V_{DD}= 1.7-1.95V

		54 MHz		66 MHz		
Symbol	Parameter	Min	Max	Min	Max	Units
T_{AVS}	Address and AVD# Low setup time[2]	0		0		ns
T_{AAHS}	Address Hold from AVD# High (Fixed Latency)	3		2		ns
T_{BPHS}	BES# High between Subsequent Burst or Mixed Mode Operations[3]	10		8		ns
T_{BEPS}	BES# Low Pulse Width[3]		10		10	µs
T_{BEWS}	BES# Low to WAIT Valid	1	9	1	7.5	ns
T_{BESS}	BES# Setup to CLK Active Edge	7		5		ns
T_{HDS}	Hold Time from Active CLK Edge	3		2		µs
T_{BHZS}	BES# High to WAIT High-Z Output		8		8	ns
T_{CAVDS}	Last Clock to AVD# Low (Fixed Latency)	6		6		ns
T_{CWS}	Clock to WAIT Valid		11		11	ns
T_{SPS}	Setup Time to Activate CLK Edge	5		3		ns

T36.0 1358

1. All tests are performed with the outputs configured for the default setting of full drive strength (BCR[5:4]=00B).
2. T_{AVS} required if T_{BESS} > 20ns.
3. A refresh opportunity must be provided every T_{BEPS}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked BES# HIGH, or b) BES# HIGH for longer than 15ns.

TABLE 37: Program/Erase Cycle Timing Parameters[1] V_{DD} = 1.7-1.95V

Symbol	Parameter	54 MHz		66 MHz		Units
		Min	Max	Min	Max	
T_{BP}	Word-Program Time		15		15	µs
T_{WC}	Write Cycle Time	70		45		ns
T_{AVDP}	AVD# Low Time	12		11		ns
T_{CLAH}	BEF# Low to AVD# High	10		10		ns
T_{DS}	Data Setup Time to WE#	40		25		ns
T_{DH}	Data Hold Time to WE#	0		0		ns
T_{GHWL}	Read Recovery Time before Write	0		0		ns
T_{CH}	BEF# Hold Time to WE#	0		0		ns
T_{WP}	WE# Pulse Width	45		25		ns
T_{WPH}	WE# Pulse Width High	25		20		ns
T_{SRW}	Latency Between Read and Write Operations	0		0		ns
T_{CS}	BEF# Set Up Time to WE#	0		0		ns
T_{AHWL}	AVD# High to WE# Low	6		5		ns
T_{IDA}	Software ID Access and Exit Time		150		150	ns
T_{SE}	Sector Erase Time		25		25	ms
T_{BE}	Block Erase Time		25		25	ms
T_{SCE}	Chip Erase Time		50		50	ms
T_{ES}	Erase-Suspend Latency Time		15		15	µs
T_{ERH}	Erase-Resume Hold Time to the next Erase-Suspend	330		330		µs
T_{VH}	Rise time to the Supervoltage VH		500		500	ns
T_{VLHT}	Voltage Transition Time		1		1	µs

T37.0 1358

1. Not 100% tested.

TABLE 38: Power Up Timings[1]

Symbol	Parameter	Minimum	units
TPU-READ	Power-up to Read Operation	100	µs
TPU-WRITE	Power-up to Write Operation	100	µs
T_{RSTH}	RST# Low Hold Time after V_{DD}/V_{DDQ} setup	50	µs

T38.0 1358

1. Not 100% tested.

TABLE 39: Flash Hardware Reset

Symbol	Parameter	Min	Max	Units
TREADYW	RST# pin Low to Read Mode (During Embedded Algorithm)[1]		35	µs
TREADY	RST# pin Low to Read Mode (NOT During Embedded Algorithm)[1]		500	ns
TRP	RST# Pulse Width	500		ns
TRH	RST# High Time Before Read	200		ns
TRPD	RST# Low to Stand-By Mode	20		us

T39.0 1358

1. Not 100% tested.

TABLE 40: Clock Input AC Parameters[1]

Symbol	Parameter	54 MHz		66 MHz		Units
		Min	Max	Min	Max	
F_{CLK}	CLK Frequency		54		66	MHz
T_{CLK}	CLK Period	18.5		15		ns
T_{CH}	CLK High Time from 90% V_{DD} – 90% V_{DD}	2		2		ns
T_{CL}	CLK Low Time from 10% V_{DD} – 10% V_{DD}	2		2		ns
T_{CHCL}	CLK Fall / Rise Time from 90% – 10% / 10% – 90%		3		3	ns
T_{CHLH}	CLK High / Low Time from 50% V_{DD} – 50% V_{DD}	7.5		6.5		ns

T40.0 1358

1. Not 100% tested.

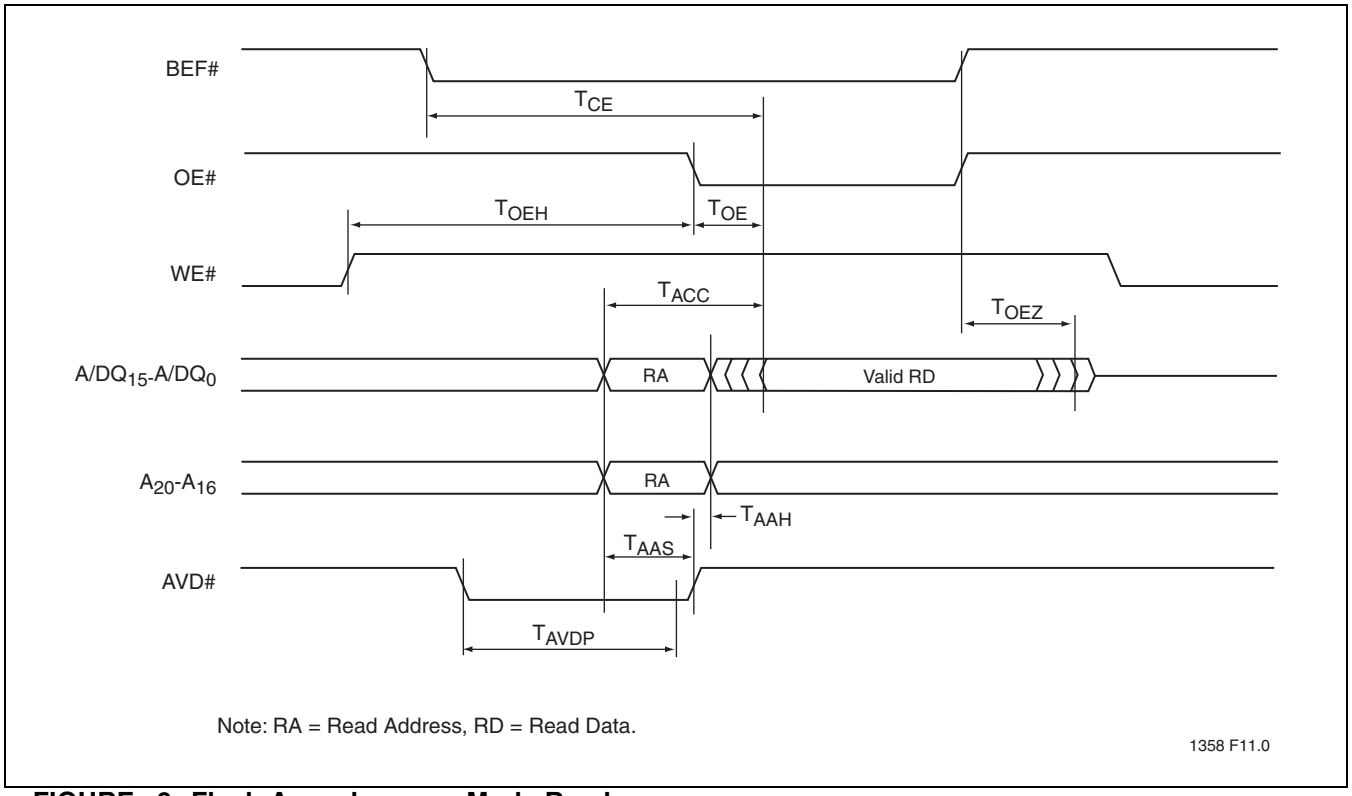


FIGURE 9: Flash Asynchronous Mode Read

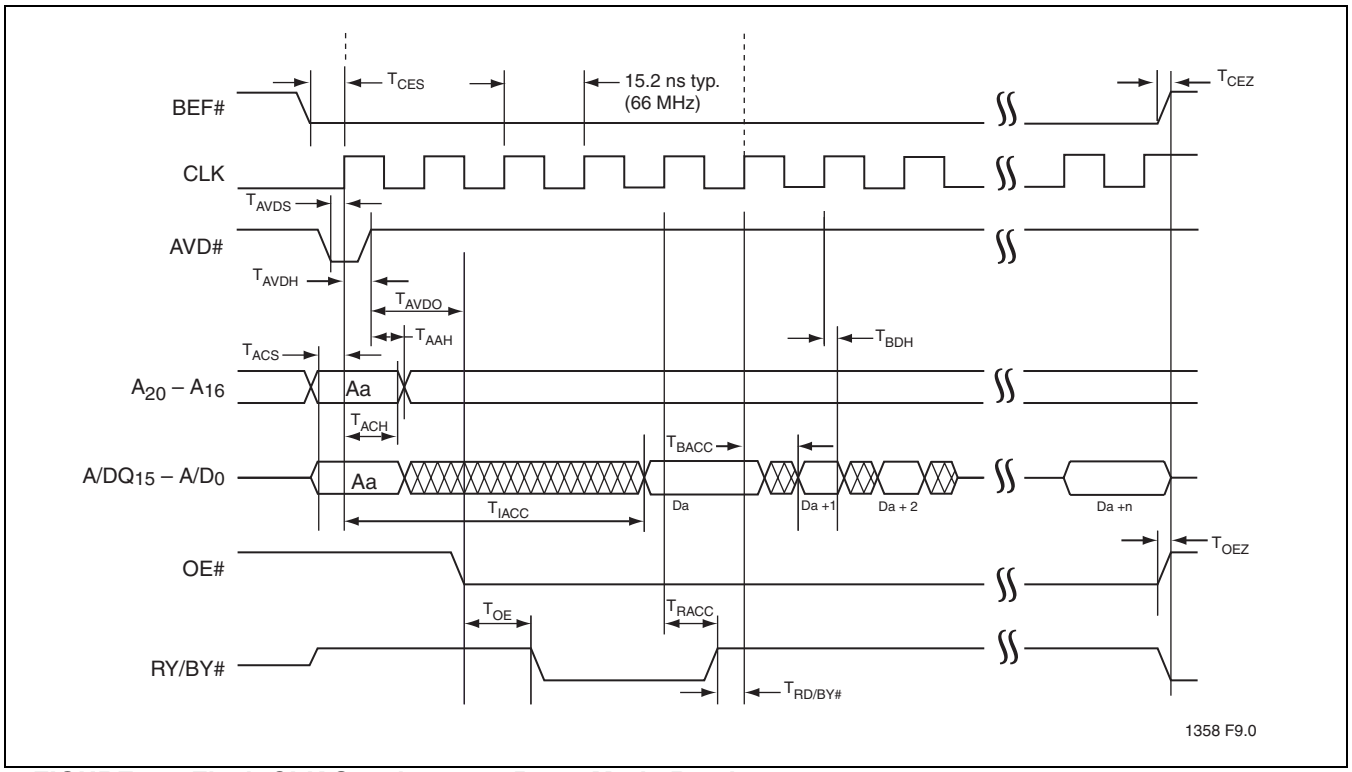
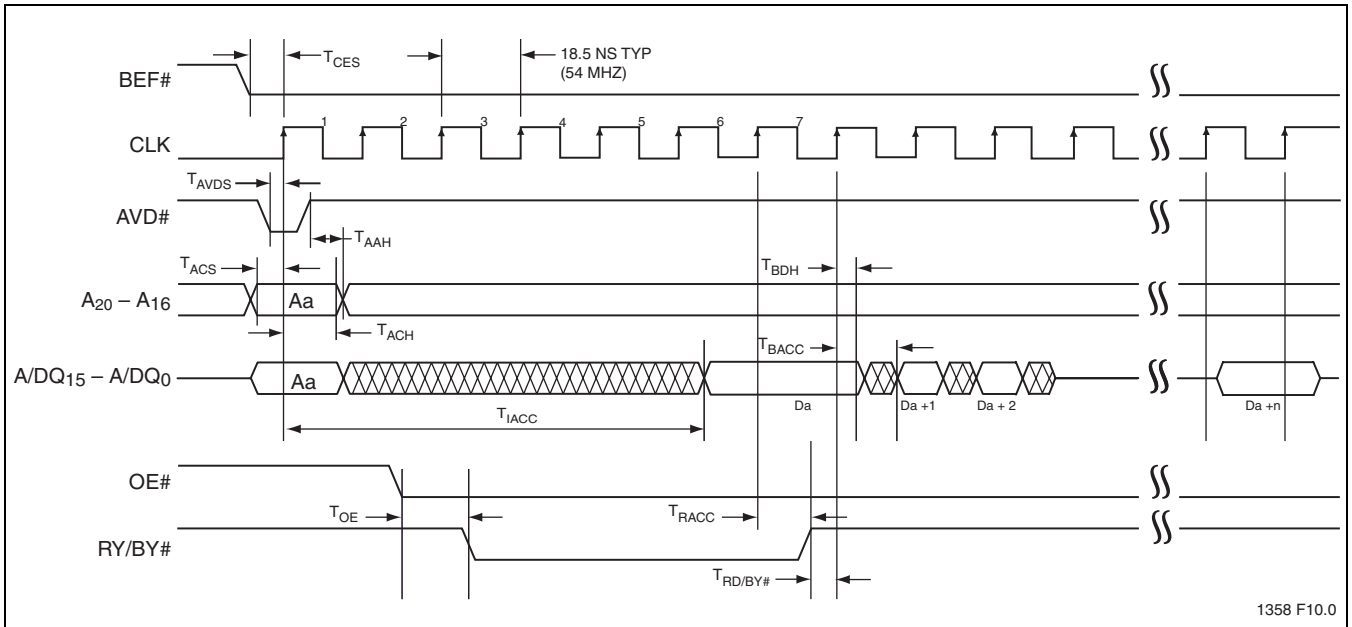


FIGURE 10: Flash CLK Synchronous Burst Mode Read



Note: Figure assumes seven wait states for initial access, 54 MHz clock, and automatic detect synchronous read.
d0-d7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest.
Data will wrap around within the 8 words, non-stop unless the RESET# is asserted low, or AVD# locks in another address.
The device will output RD/BY# with valid data.

FIGURE 11: Flash 8-Word Linear Burst with Wrap-Around

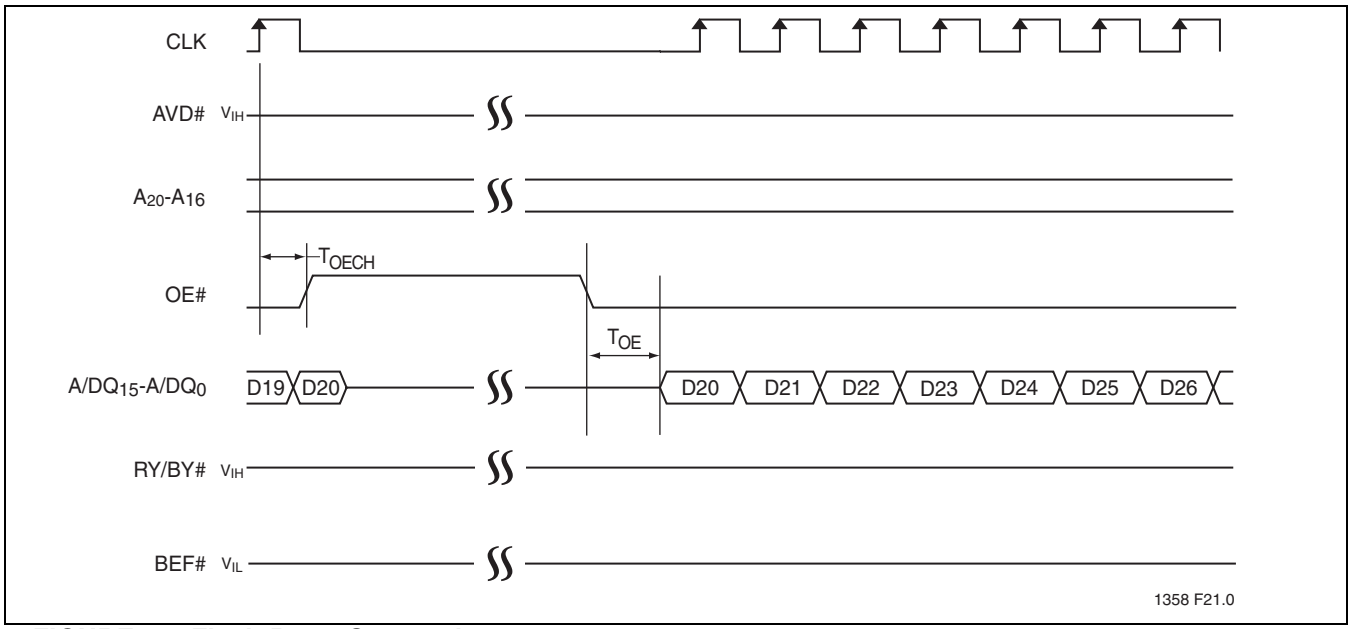
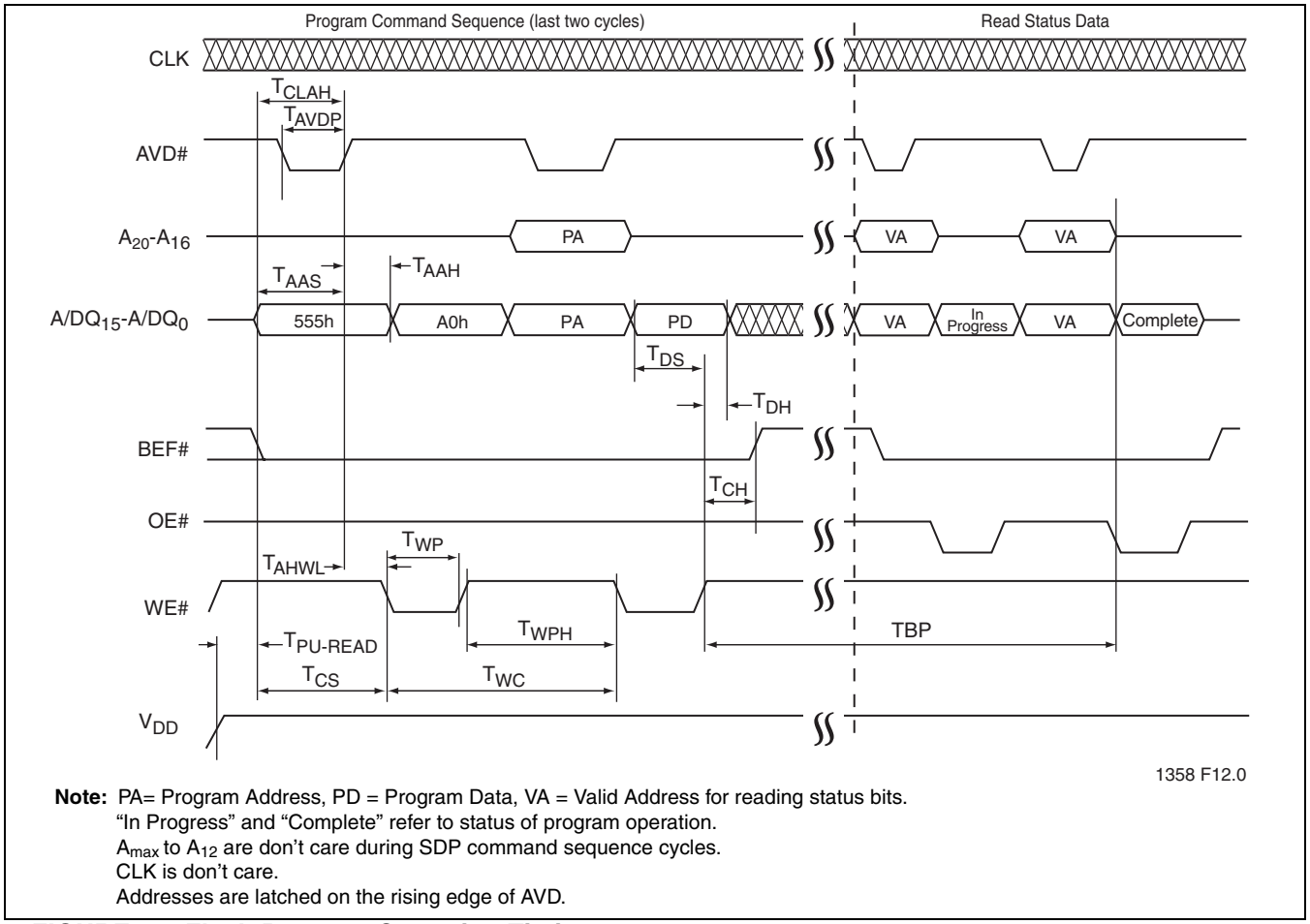
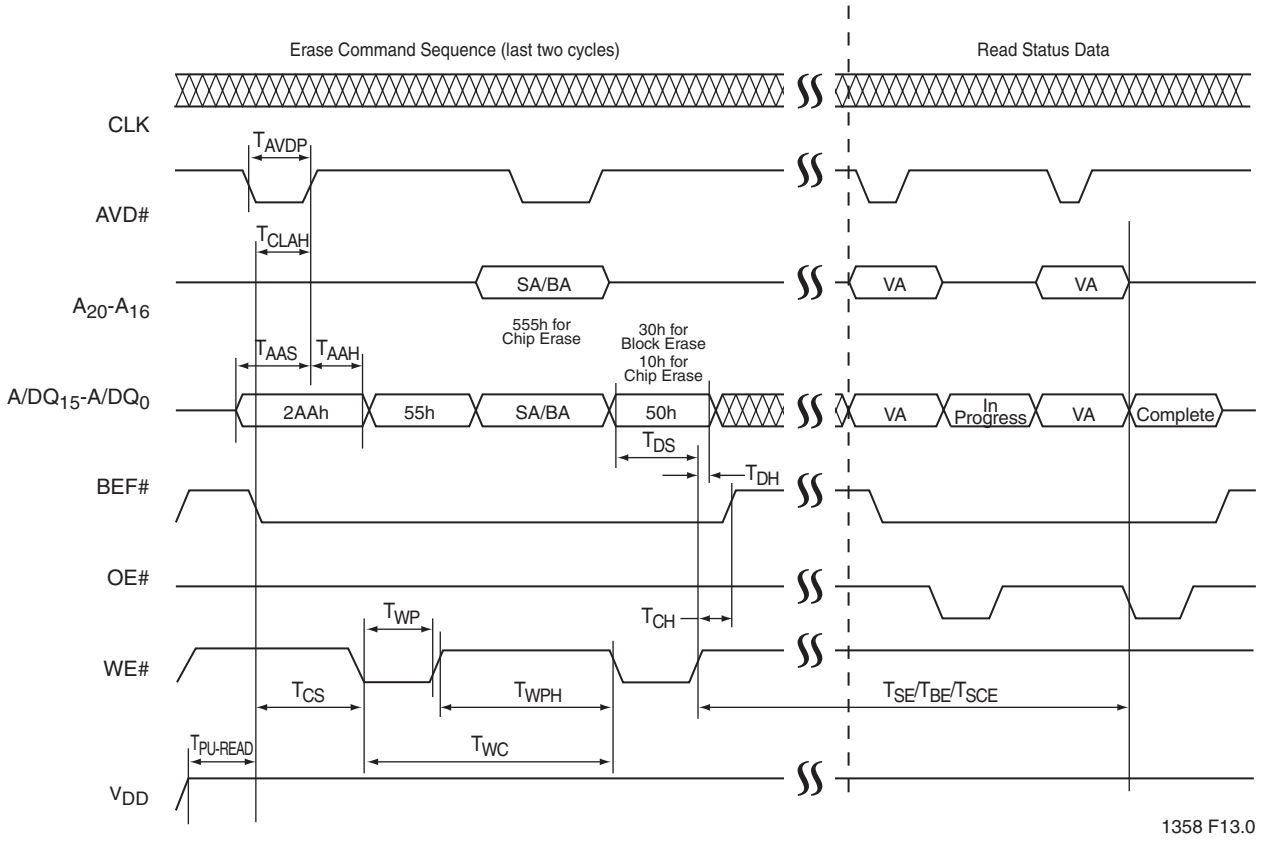


FIGURE 12: Flash Burst Suspend



Note: PA= Program Address, PD = Program Data, VA = Valid Address for reading status bits.
"In Progress" and "Complete" refer to status of program operation.
A_{max} to A_{12} are don't care during SDP command sequence cycles.
CLK is don't care.
Addresses are latched on the rising edge of AVD.

FIGURE 13: Flash Program Operation Timings



Note: SA is the sector address for Sector Erase.
BA is the block address for Block Erase.
Address bits A_{20} to A_{12} are don't care during SDP cycles in the command sequence.

FIGURE 14: Flash Chip/Block/Sector Erase Command Sequence

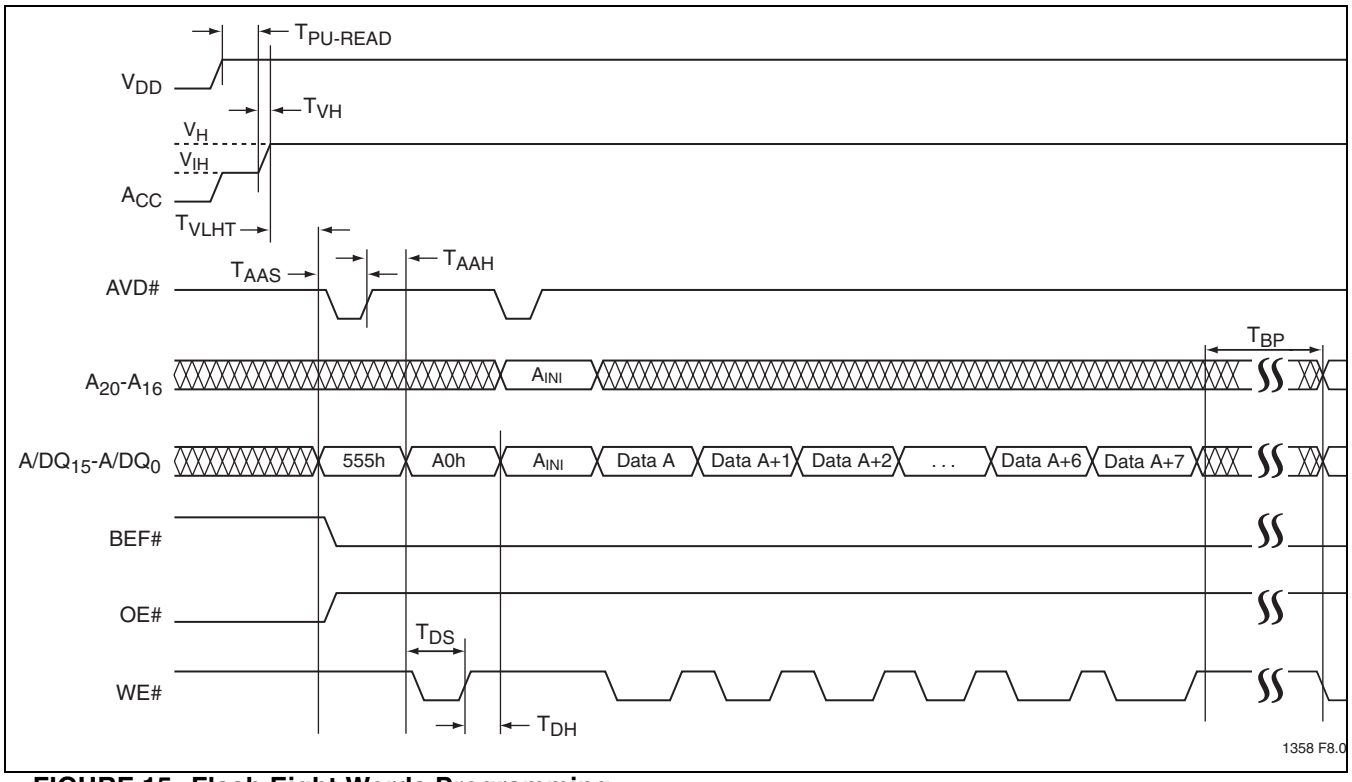
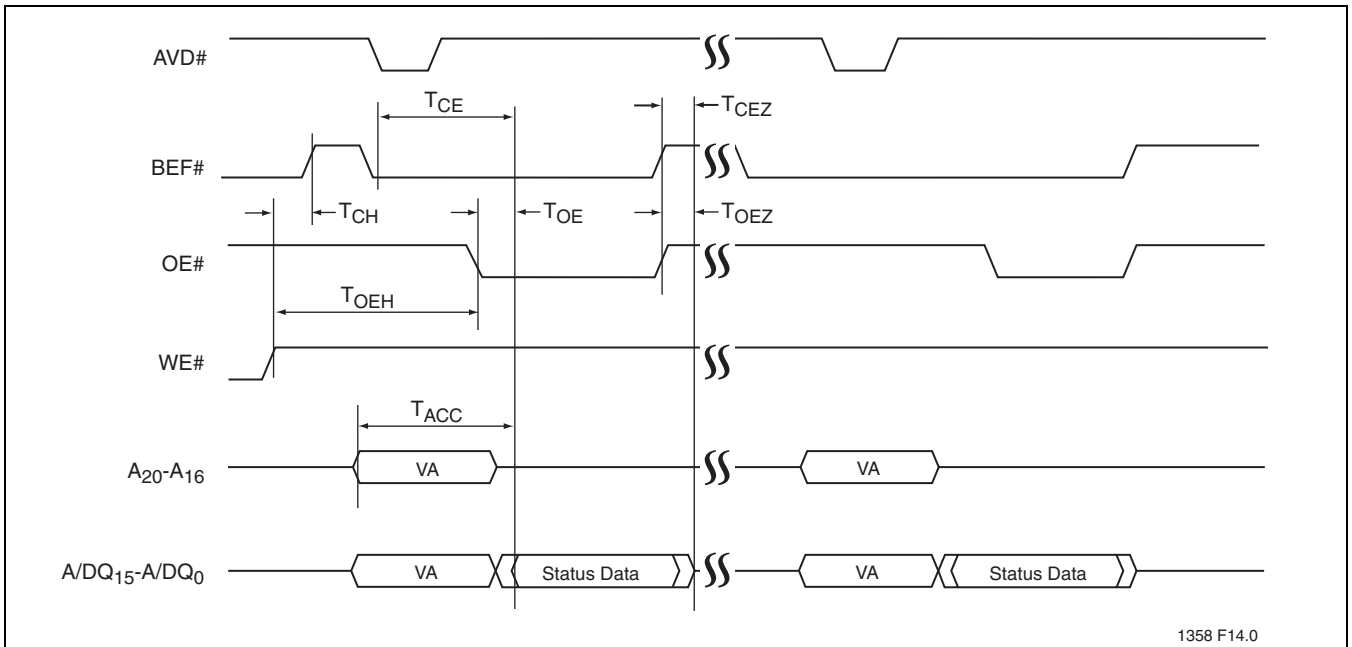
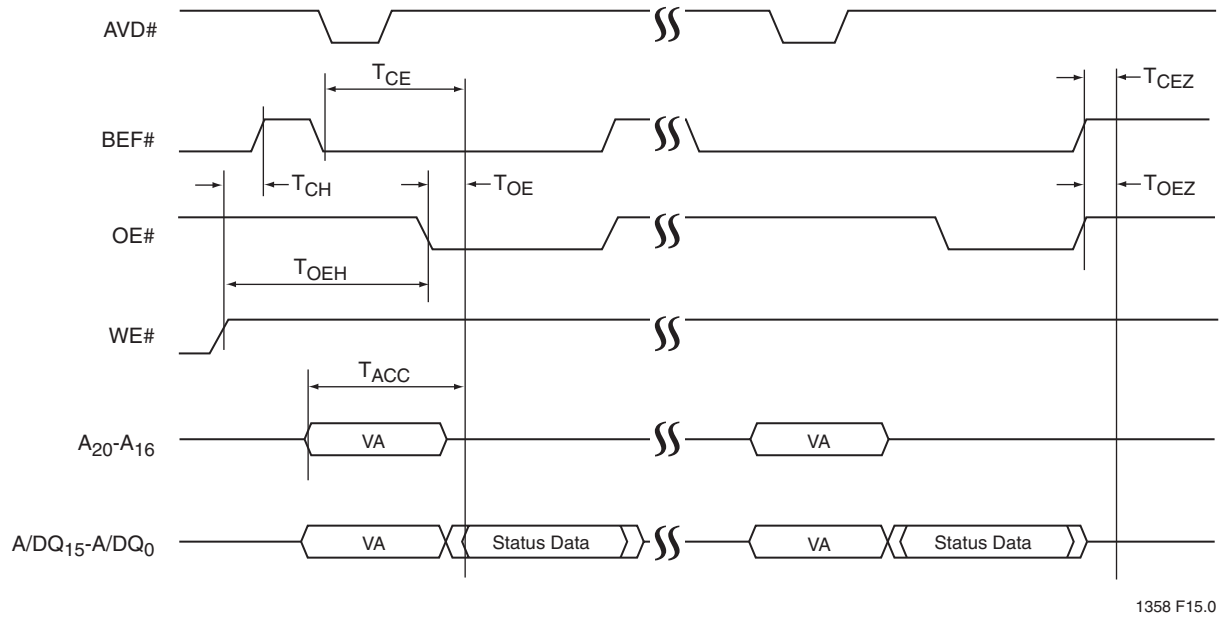


FIGURE 15: Flash Eight Words Programming



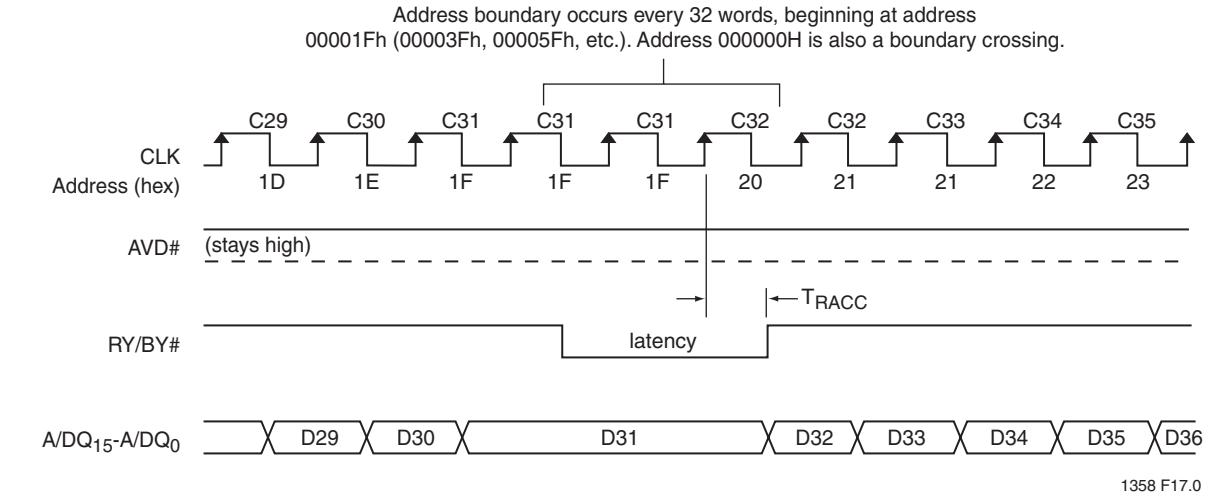
Note: VA = Valid Address. Two Read cycles are required to determine status.
When the Embedded Algorithm operation is complete, the Data# Polling will output true data.
AVD# must toggle between data reads.

FIGURE 16: Flash Data# Polling Timings (During Embedded Algorithms)



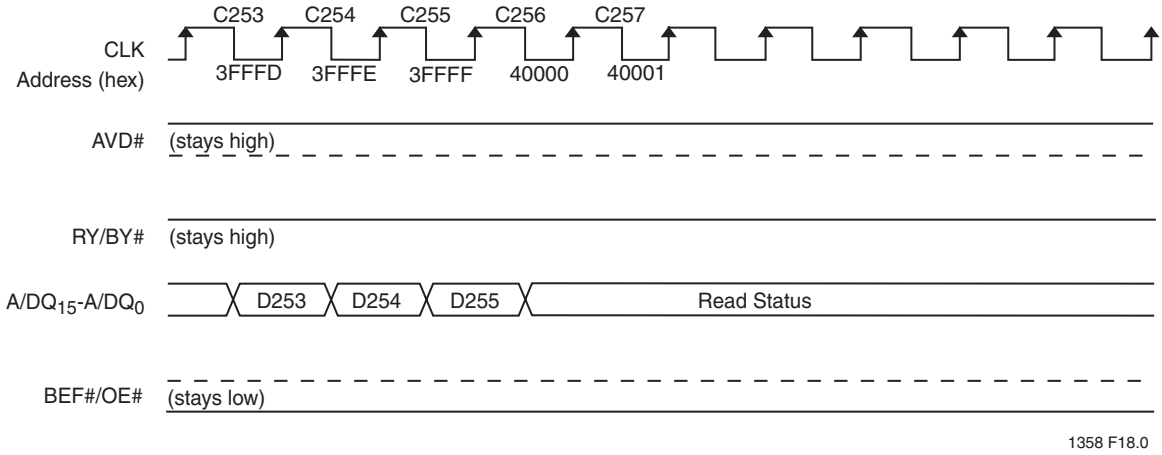
Note: VA = Valid Address. Two Read cycles are required to determine status.
When the Embedded Algorithm operation is complete, the Data# Polling will output true data.
AVD# must toggle between data reads.

FIGURE 17: Flash Toggle Bit Timings (During Embedded Algorithms)



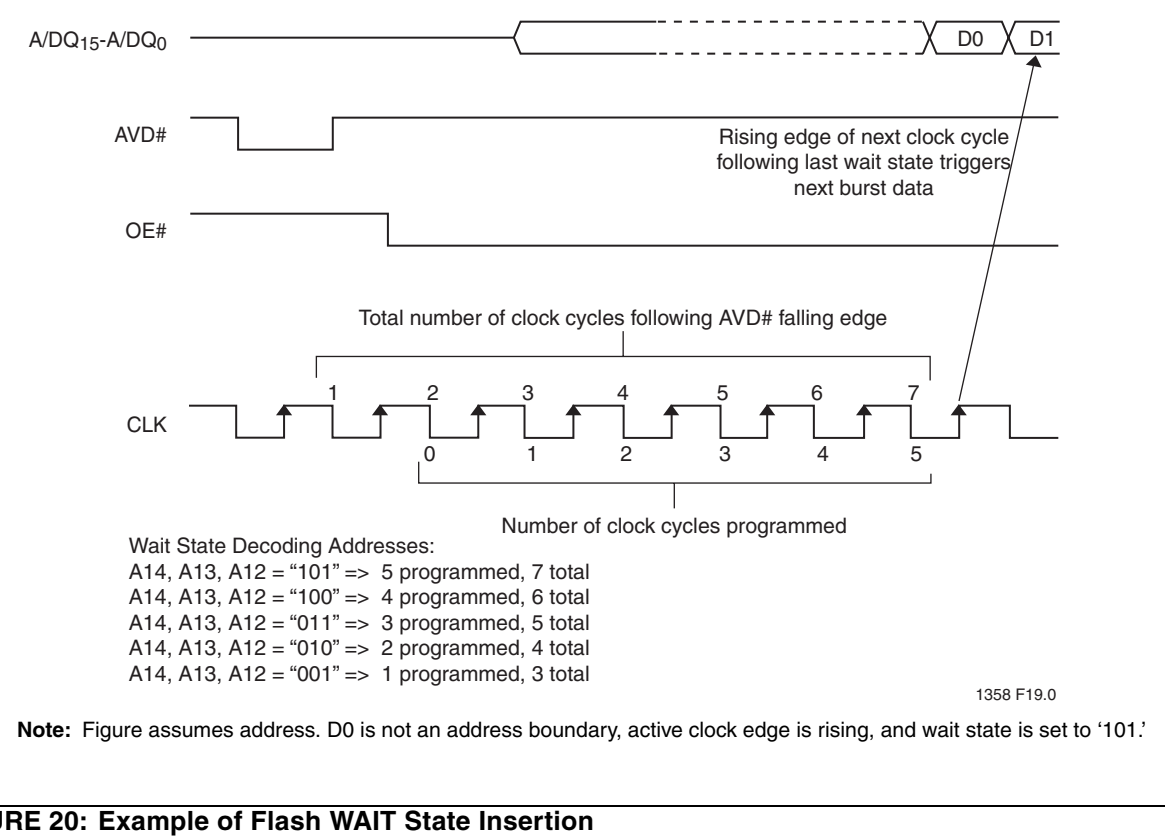
Note: Cxx indicates which clock triggers Dxx at the output. For example, C30 triggers D30.
The figure shows that the device does not cross a bank when performing an erase or program operation.
The latency with boundary crossing happens at the 32-word boundary.

FIGURE 18: Flash Latency with Boundary Crossing



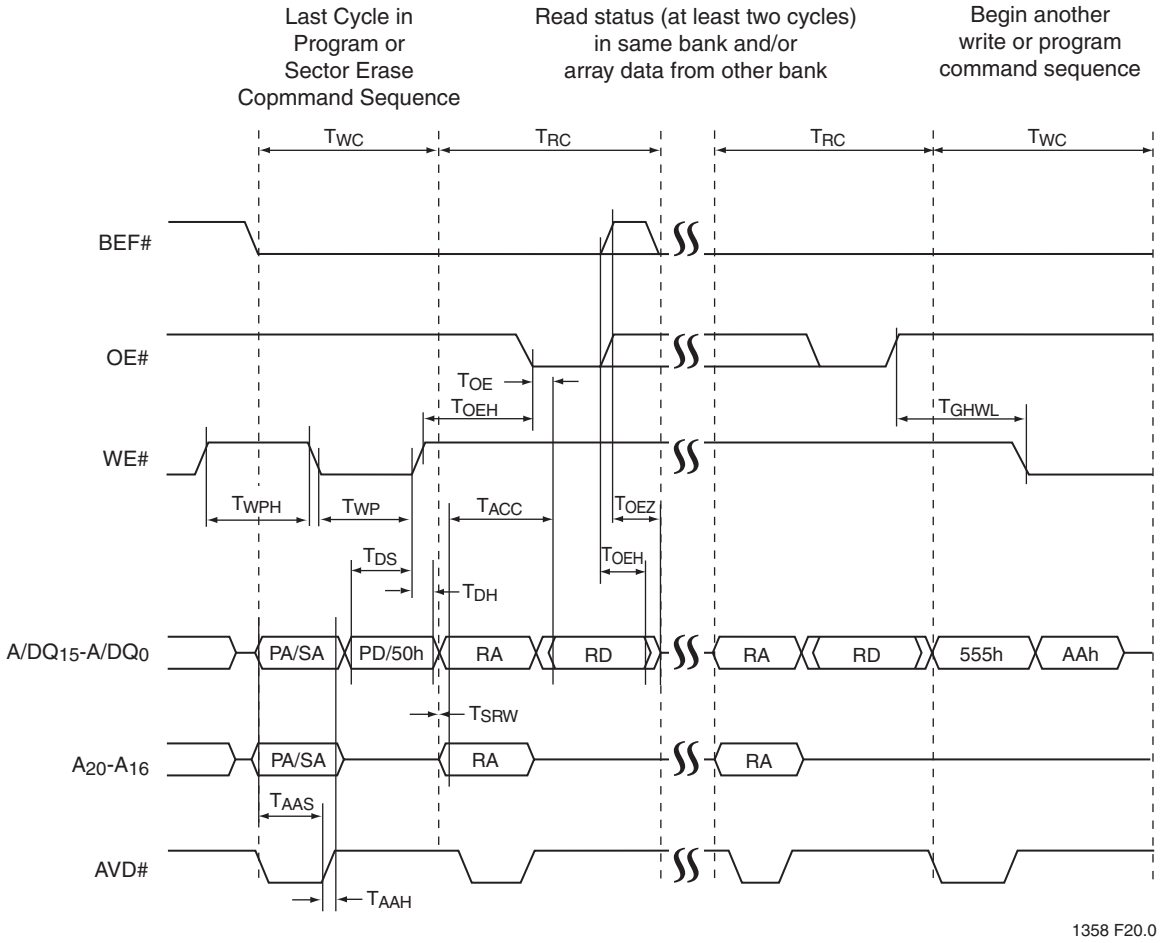
Note: Cxxx indicates which clock triggers Dxxx at the output. For example, C253 triggers D253.
The figure shows that the device cross a bank when performing an erase or program operation.

FIGURE 19: Flash Boundary Crossing into Program/Erase Bank



Note: Figure assumes address. D0 is not an address boundary, active clock edge is rising, and wait state is set to ‘101.’

FIGURE 20: Example of Flash WAIT State Insertion



Note: Breakpoints in waveforms indicate that the system may alternately read array data from the “non-busy bank” while checking the status of the program or erase operation in the “busy” bank.
The system should read status twice to ensure valid information.

FIGURE 21: Flash Back-to-Back Read/Write Cycle Timings

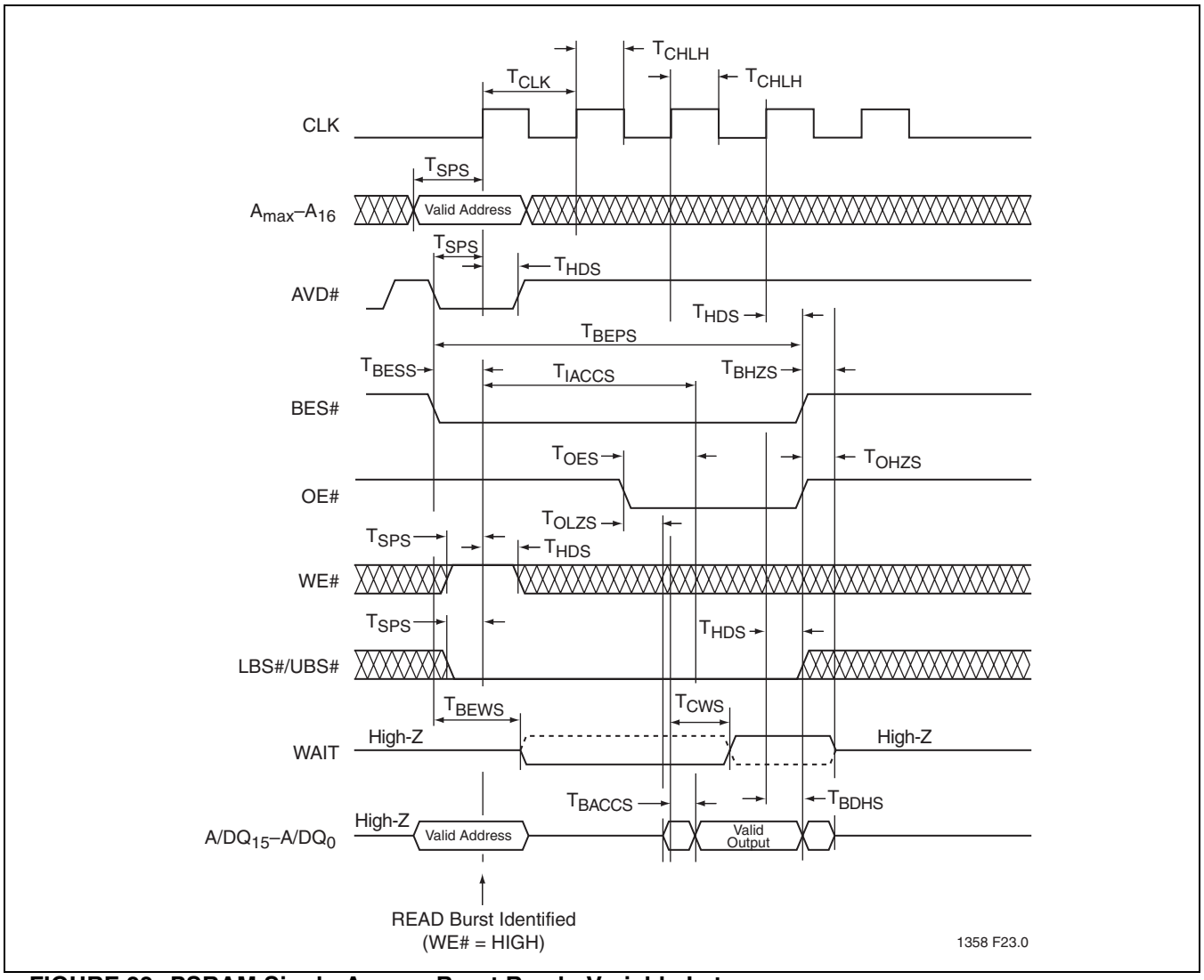
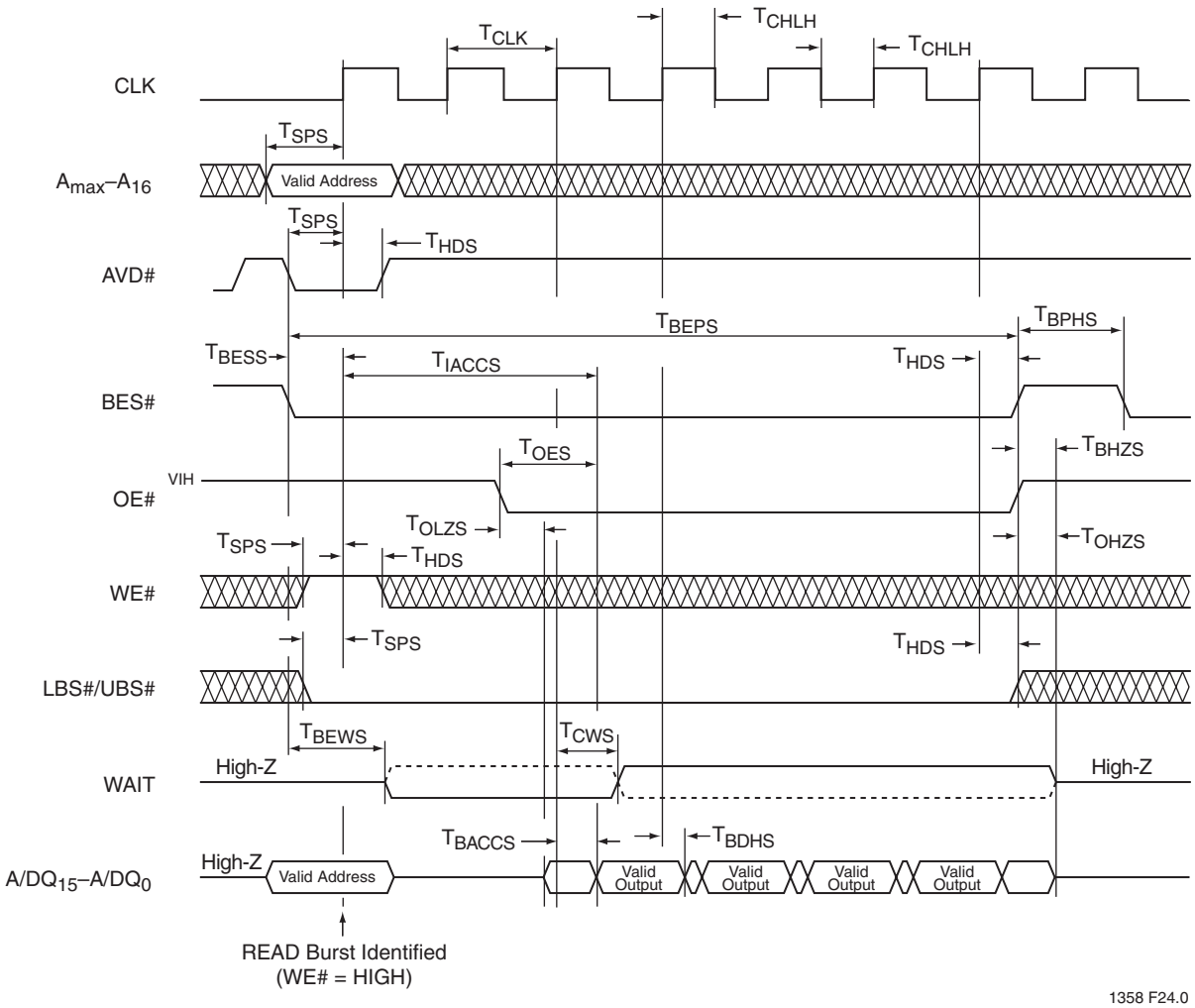
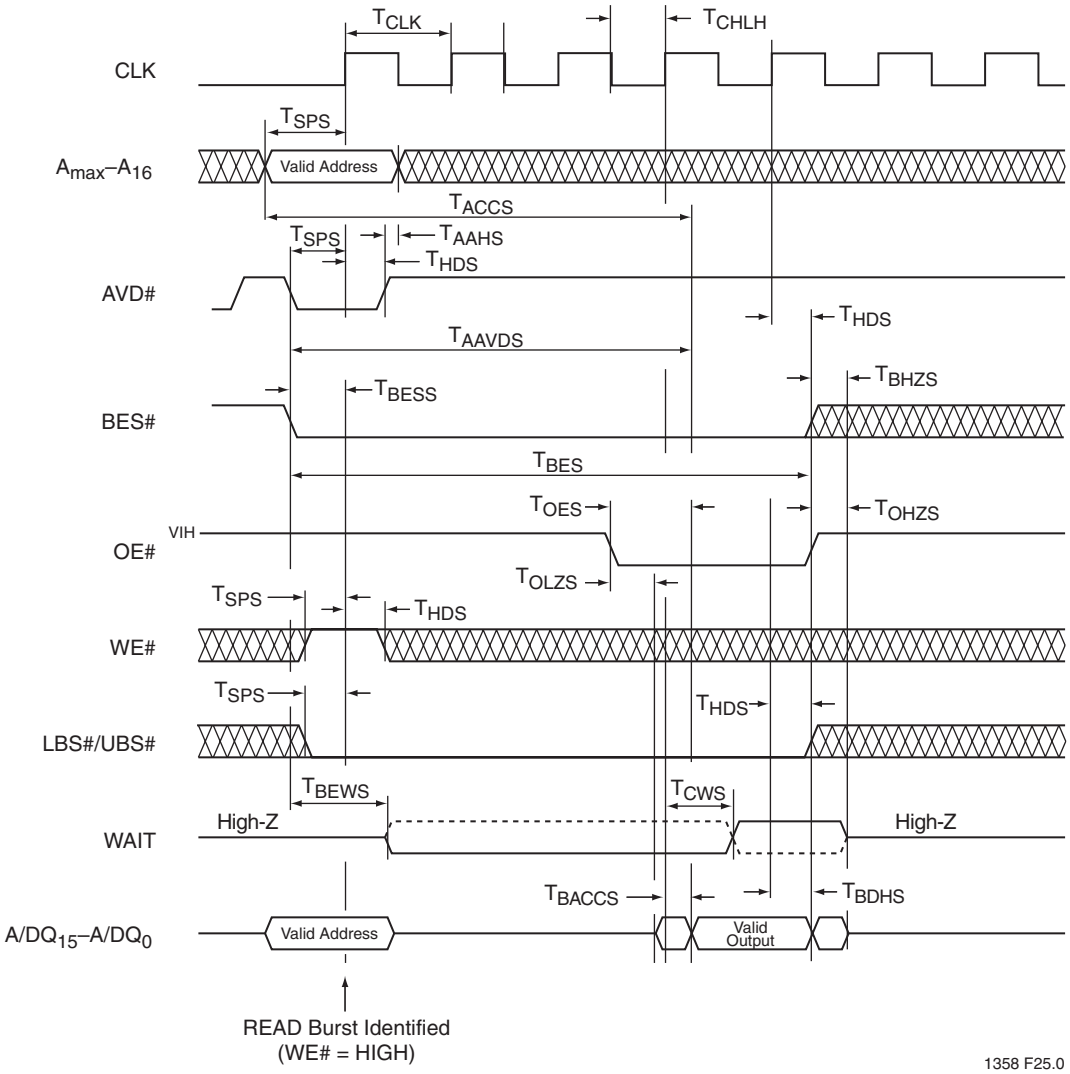


FIGURE 22: PSRAM Single-Access Burst Read - Variable Latency



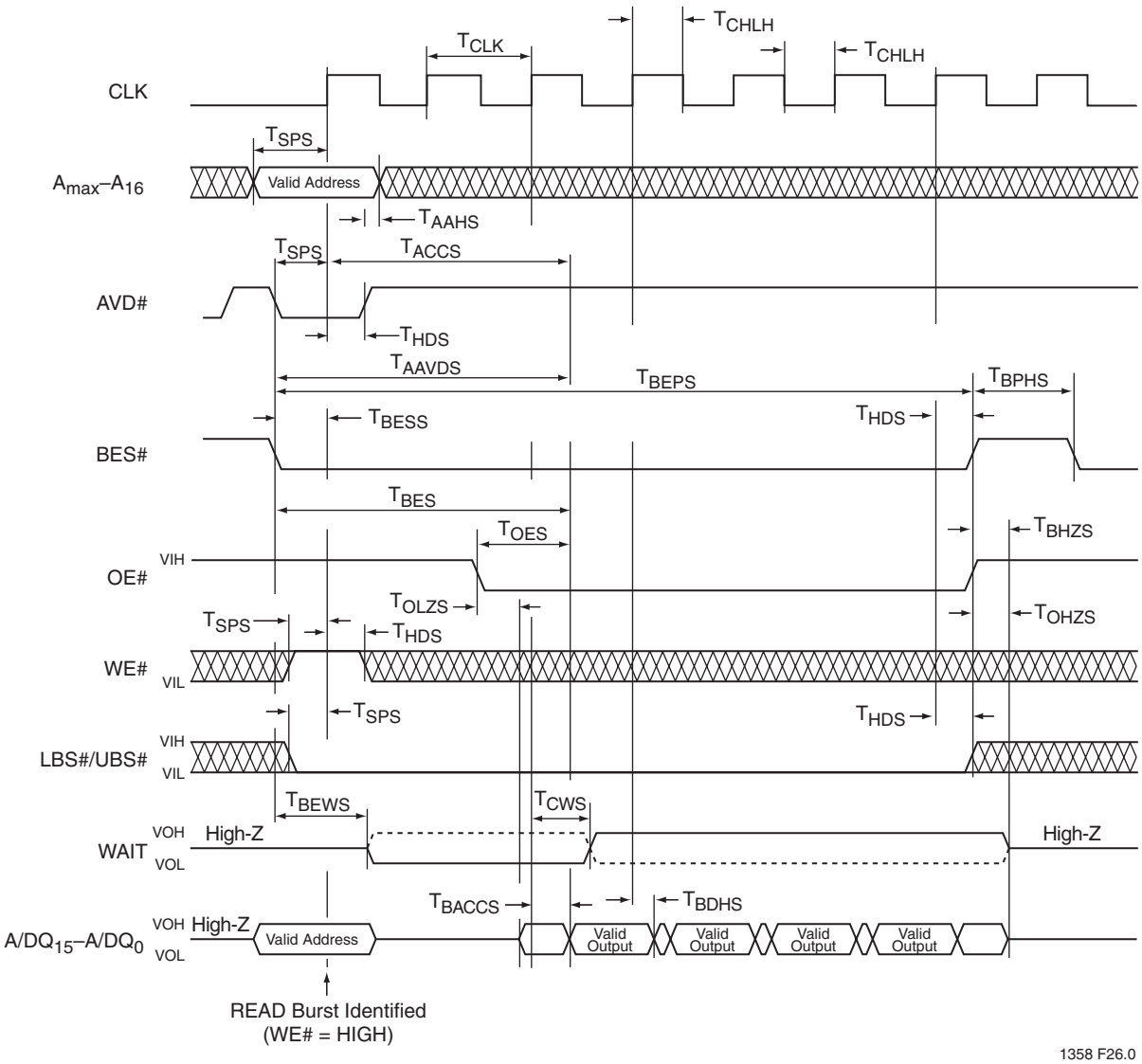
Note: Non-default BCR settings : Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

FIGURE 23: PSRAM 4-Word Burst Read Operation - Variable Latency



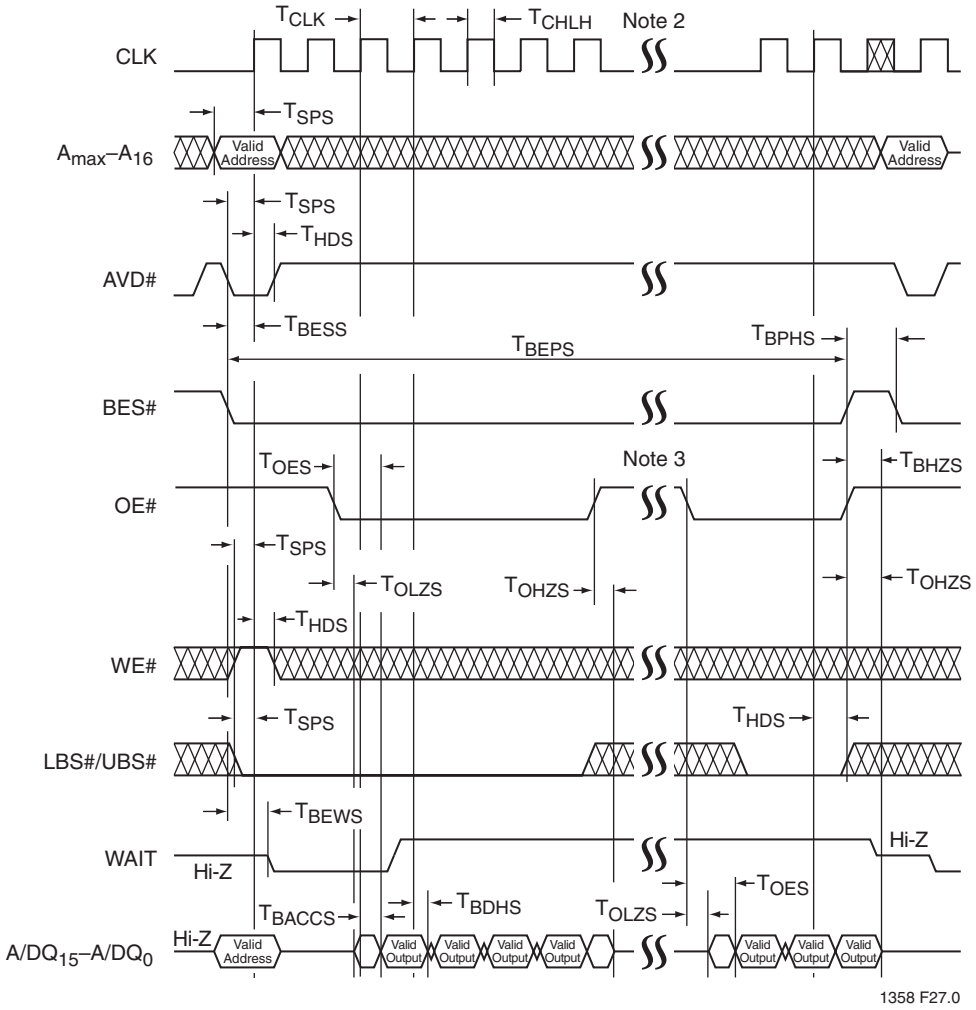
Note: Non-default BCR setting: Fixed Latency; Latency code three (four clocks); WAIT active LOW; WAIT asserted during delay.

FIGURE 24: PSRAM Single-Access burst Read - Fixed Latency



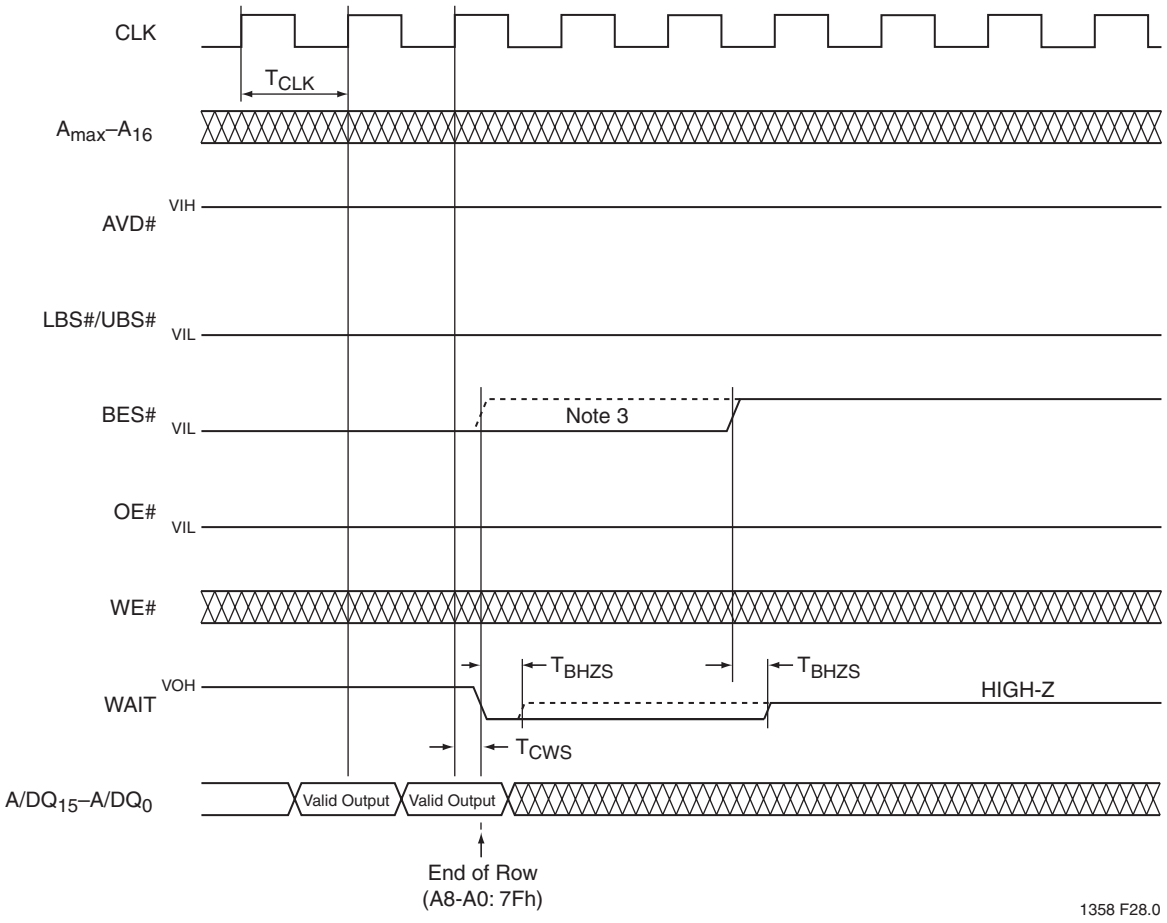
Note: Non-default BCR setting: Fixed Latency; Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

FIGURE 25: PSRAM 4-Word Burst Read - fixed Latency



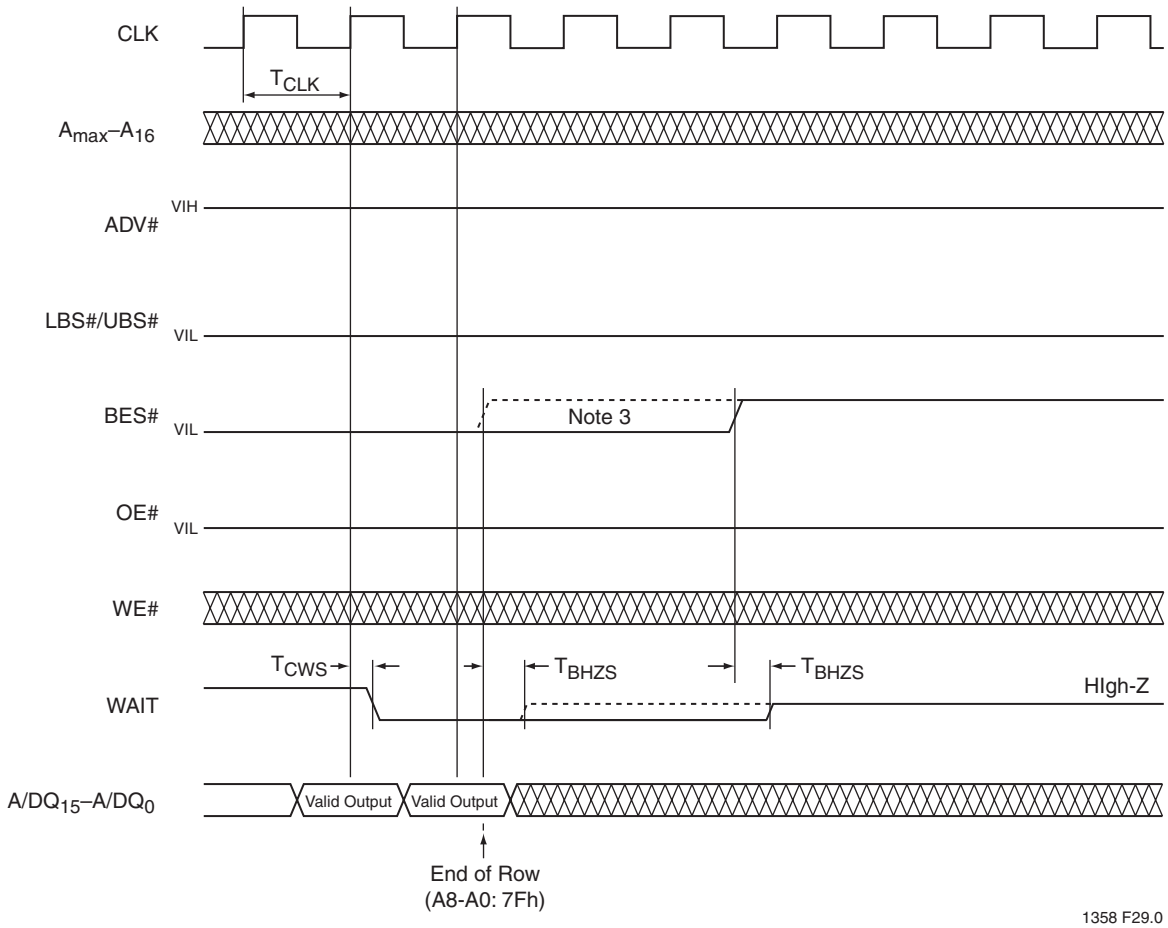
Note: 1. Non-default BCR settings for READ burst suspend: Fixed or Variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. During Burst Read Suspend operations, the Clock signal must be stopped (Low). CLK must be static with no LOW-to-HIGH transitions during burst suspend.
3. OE# can stay LOW during burst suspend. If OE# is LOW. A/DQ[15:0] will continue to output valid data.

FIGURE 26: PSRAM Read Burst Suspend



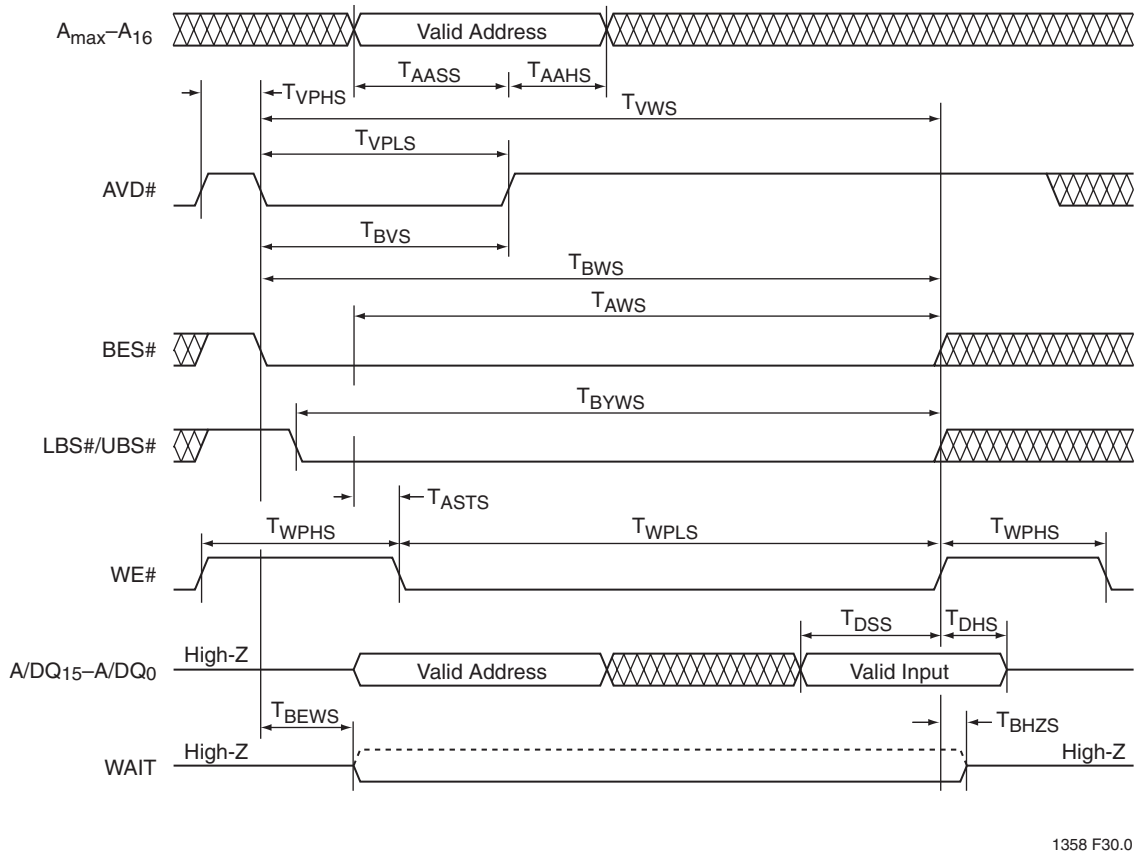
Note: 1. Non-default BCR settings for continuous burst READ, BCR[8] = 0: WAIT active LOW; WAIT asserted during delay. Do not cross row boundaries.
2. BES# must not remain LOW longer than T_{BEPS}.
3. The Bank Enable signal, BES# must go High before the third Clock cycle after the WAIT signal goes Low.

FIGURE 27: PSRAM Continuous Burst Read with Output Delay BCR[8] = 0 for variable latency end-of-row condition



Note: 1. Default BCR settings for continuous burst READ, BCR[8] = 1: WAIT active LOW; WAIT asserted one data cycle before delay. Do not cross row boundaries.
2. BES# must not remain LOW longer than T_{BEPS}.
3. The Chip Enable signal, BCR8 were set to 1, BES# would have to go Low before the fourth Clock cycle after WAIT signal goes Low.

FIGURE 28: PSRAM Continuous Burst Read with Output Delay BCR[8] = 1 for variable latency end-of-row condition



Note: 1. Data Inputs are Hi-Z if BES# is high, VIH
2. When BES# is Low, VIL (device selected). WE# must not remain Low, for longer than T_{BYWS}.
3. The end of the Write operation is controlled by BES#, LBS#/UBS#, or WE#, whichever is de-asserted first.

FIGURE 29: PSRAM Asynchronous Write Using AVD#

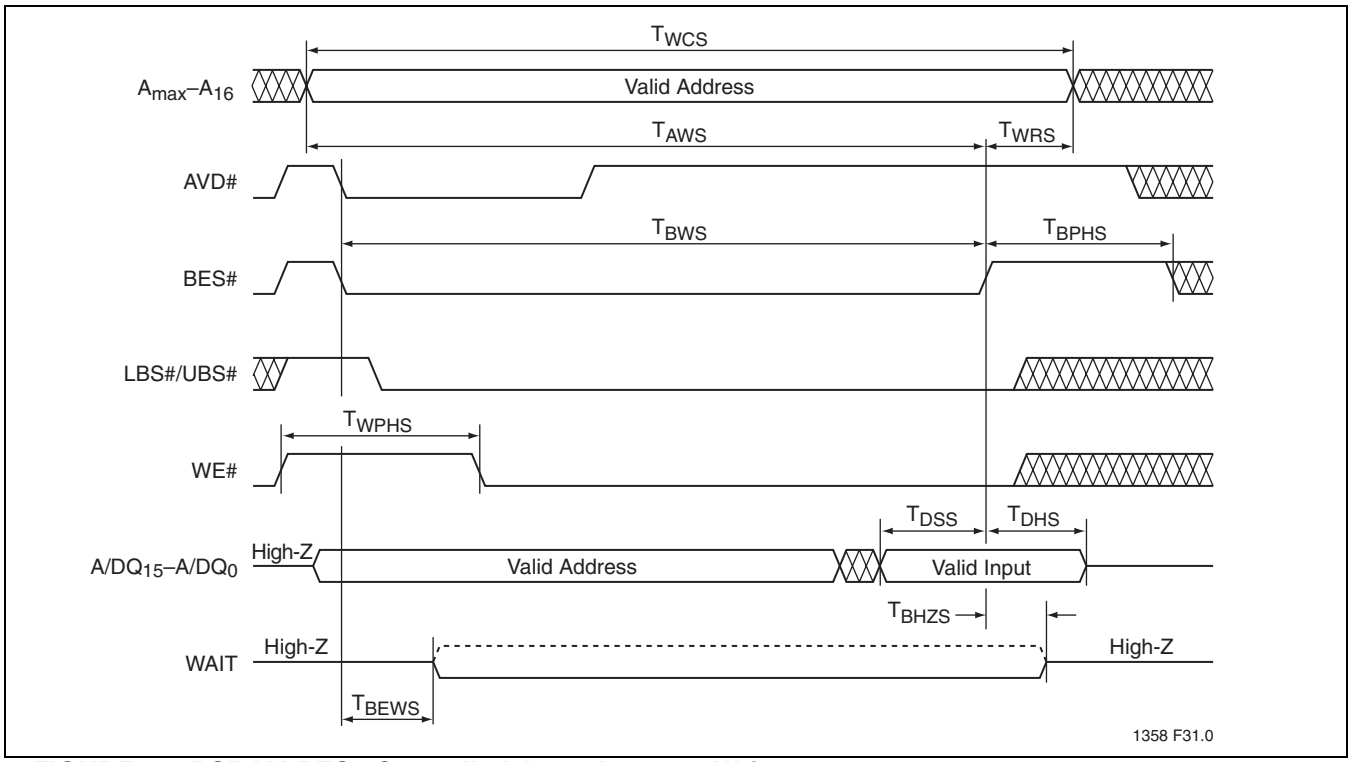


FIGURE 30: PSRAM BES# Controlled Asynchronous Write

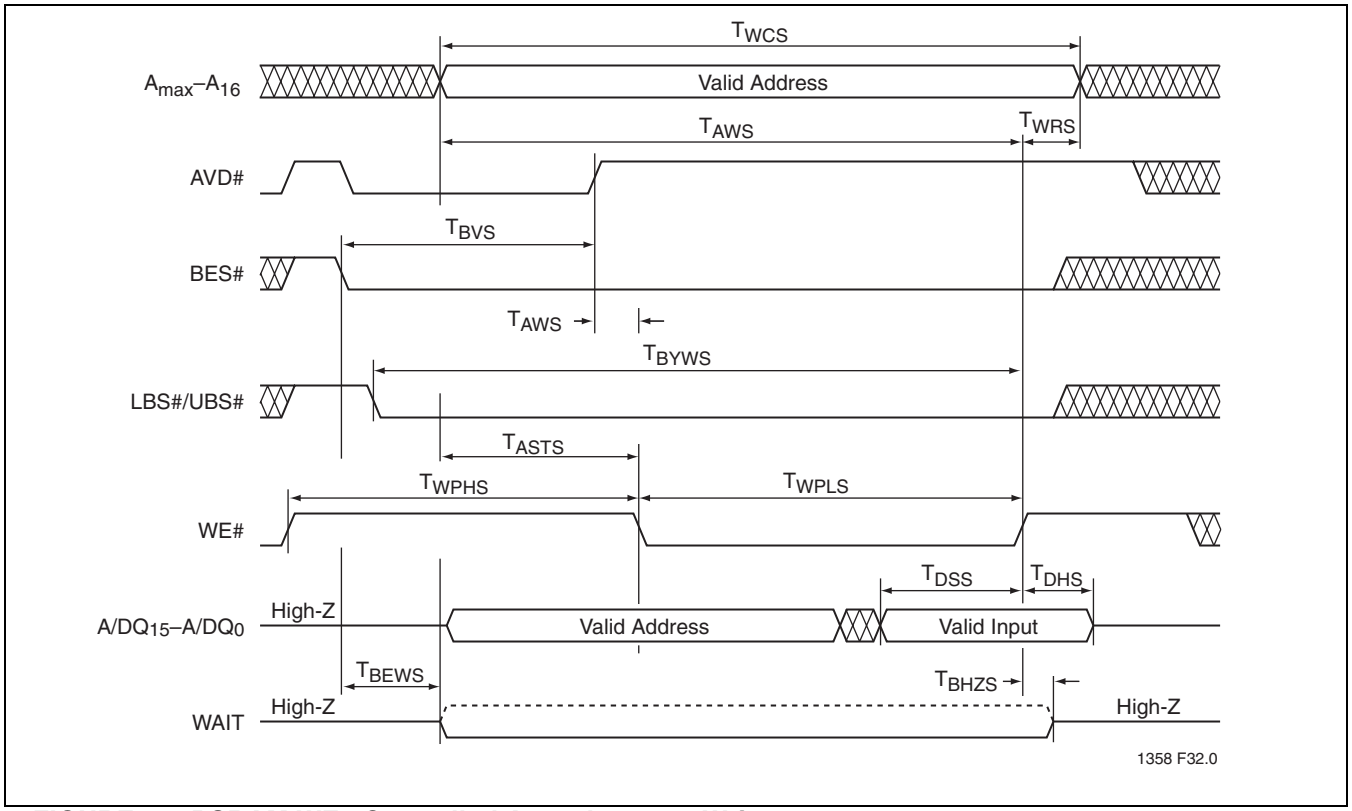
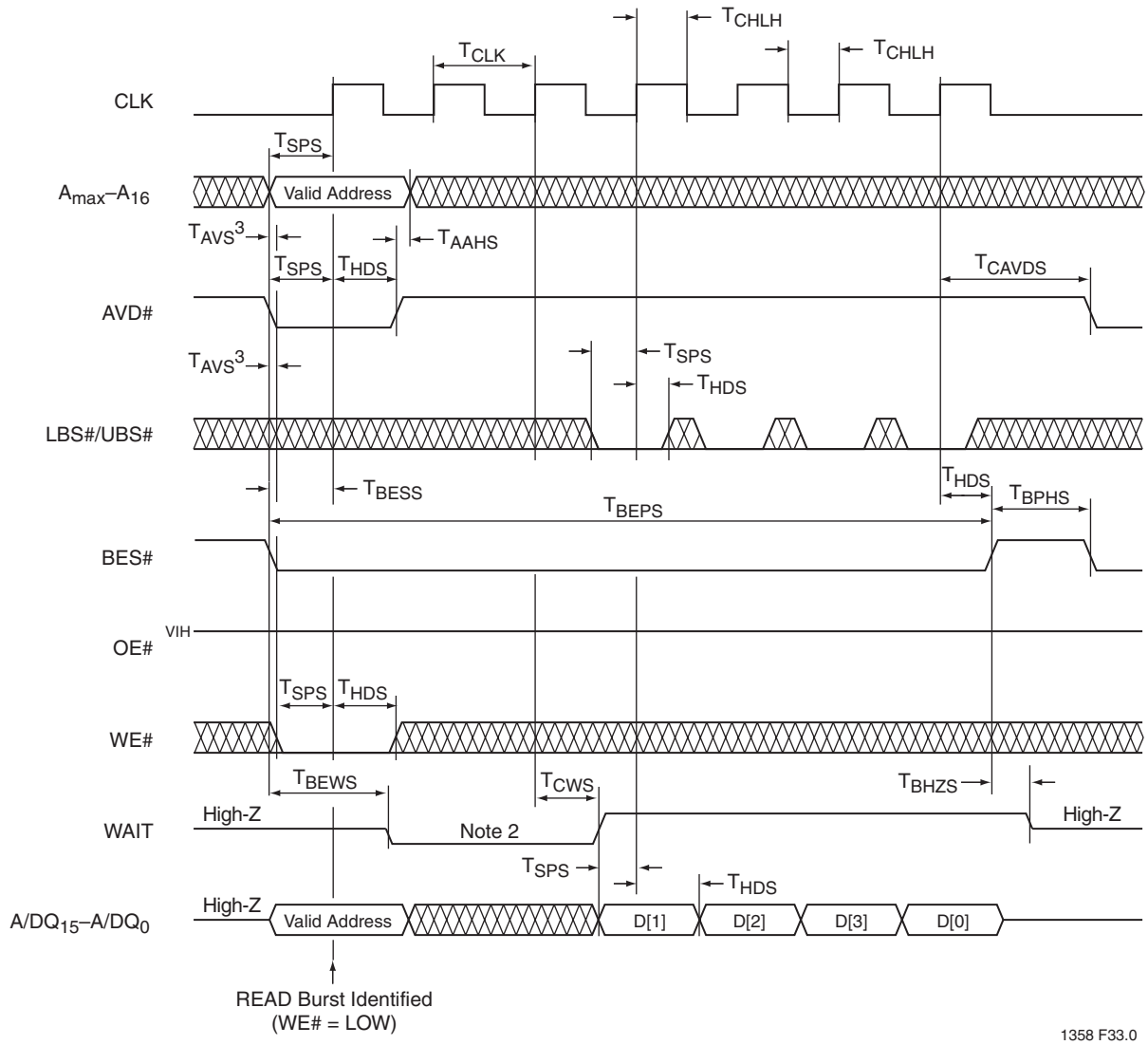
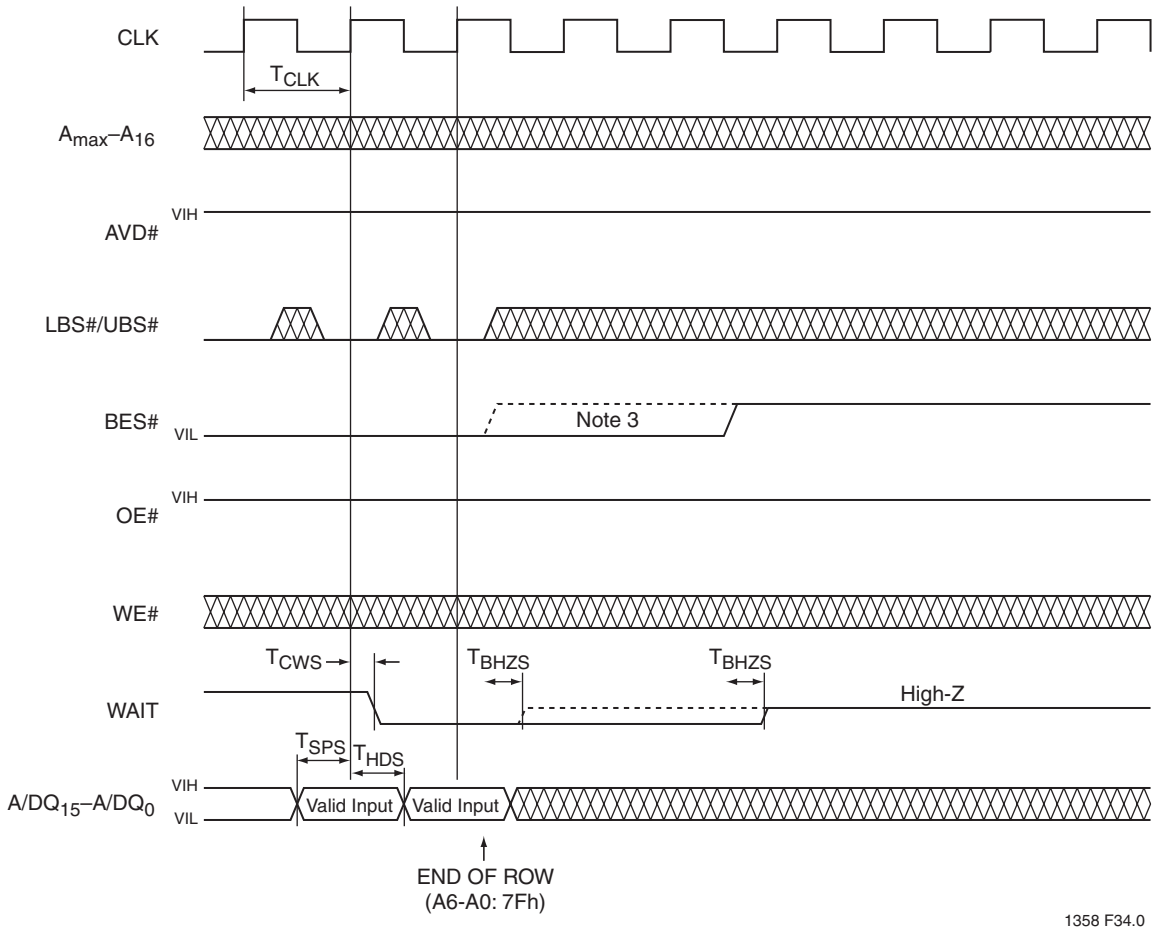


FIGURE 31: PSRAM WE# Controlled Asynchronous Write



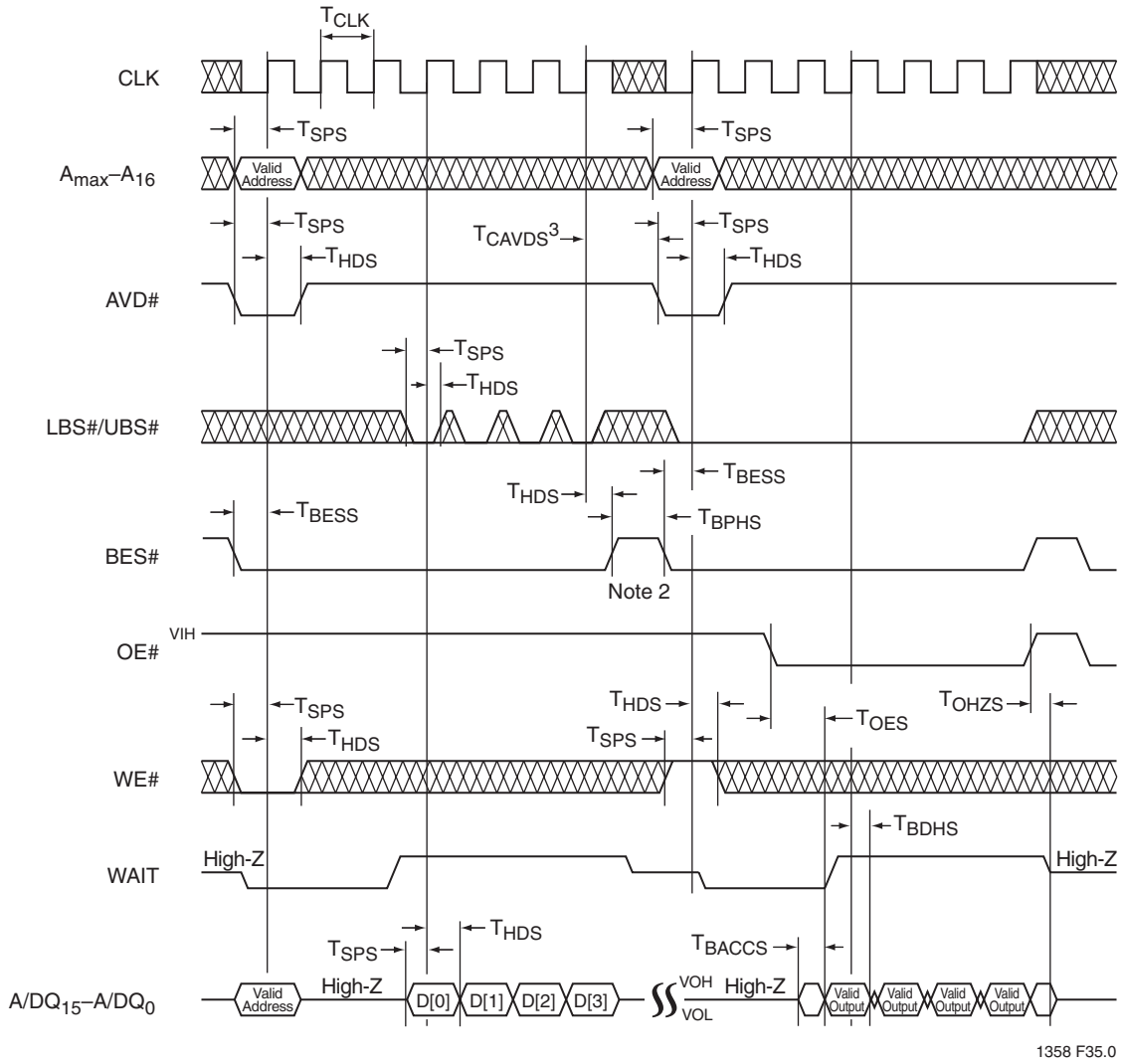
Notes: 1. Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay: burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed latency. LC = Latency Code (BCR[13:11]).
3. T_{AVS} required if T_{BESS} > 20ns.

FIGURE 32: PSRAM Burst Write - Fixed Latency



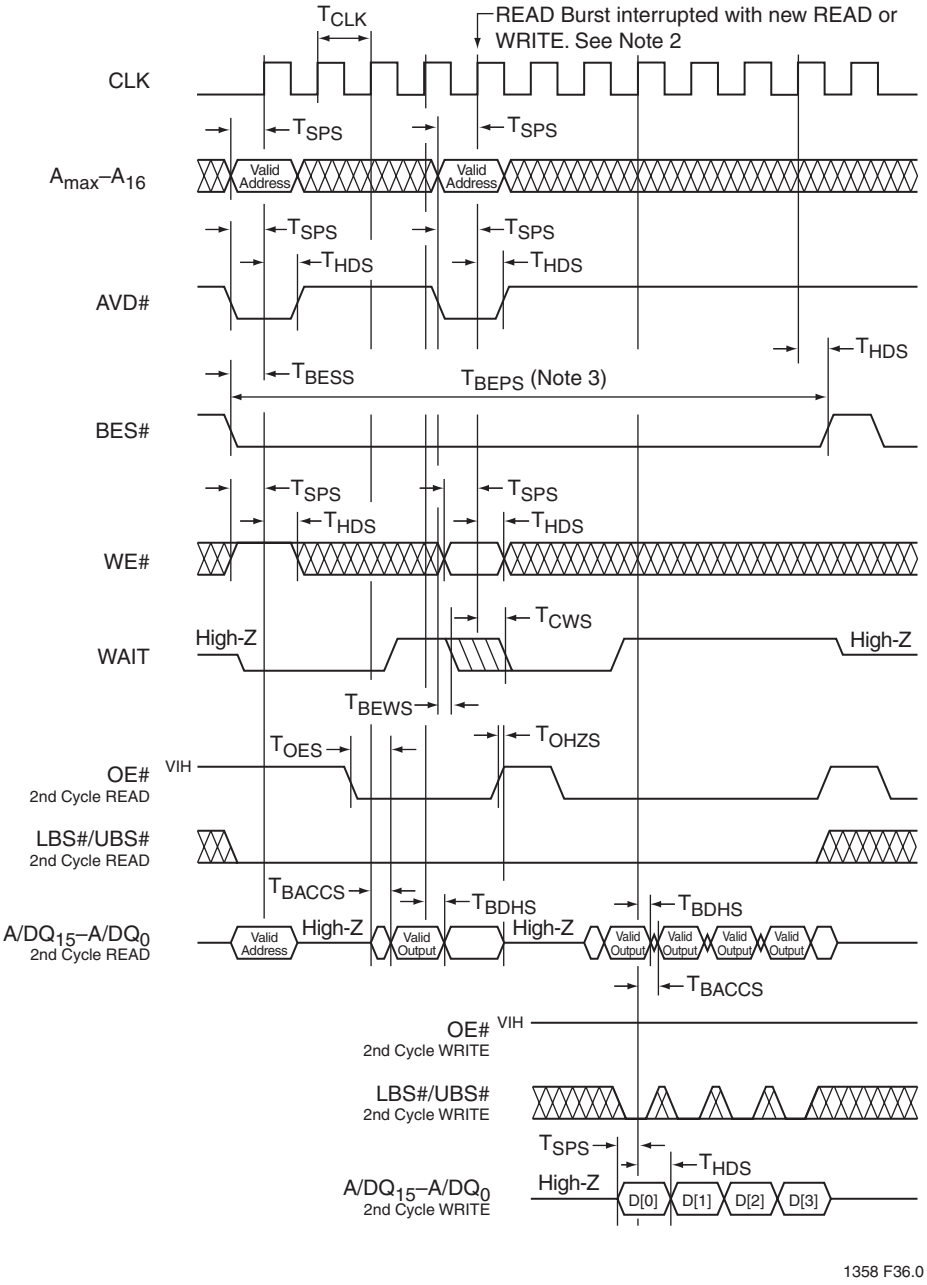
Notes: 1. Default BCR settings for continuous burst WRITE, BCR[8] = 1: WAIT active LOW. WAIT asserted one data cycle before delay.
2. BES# must not remain LOW longer than T_{BEPS}.
3. The Chip Enable signal, BES# must go High before the fourth Clock cycle after the WAIT signal goes Low. If BCR[8] were set to 0, BES# would have to go Low before the third Clock cycle after WAIT signal goes Low.

FIGURE 33: PSRAM Continuous Burst Write with Output Delay BCR[8] = 1 for end-of-row Condition



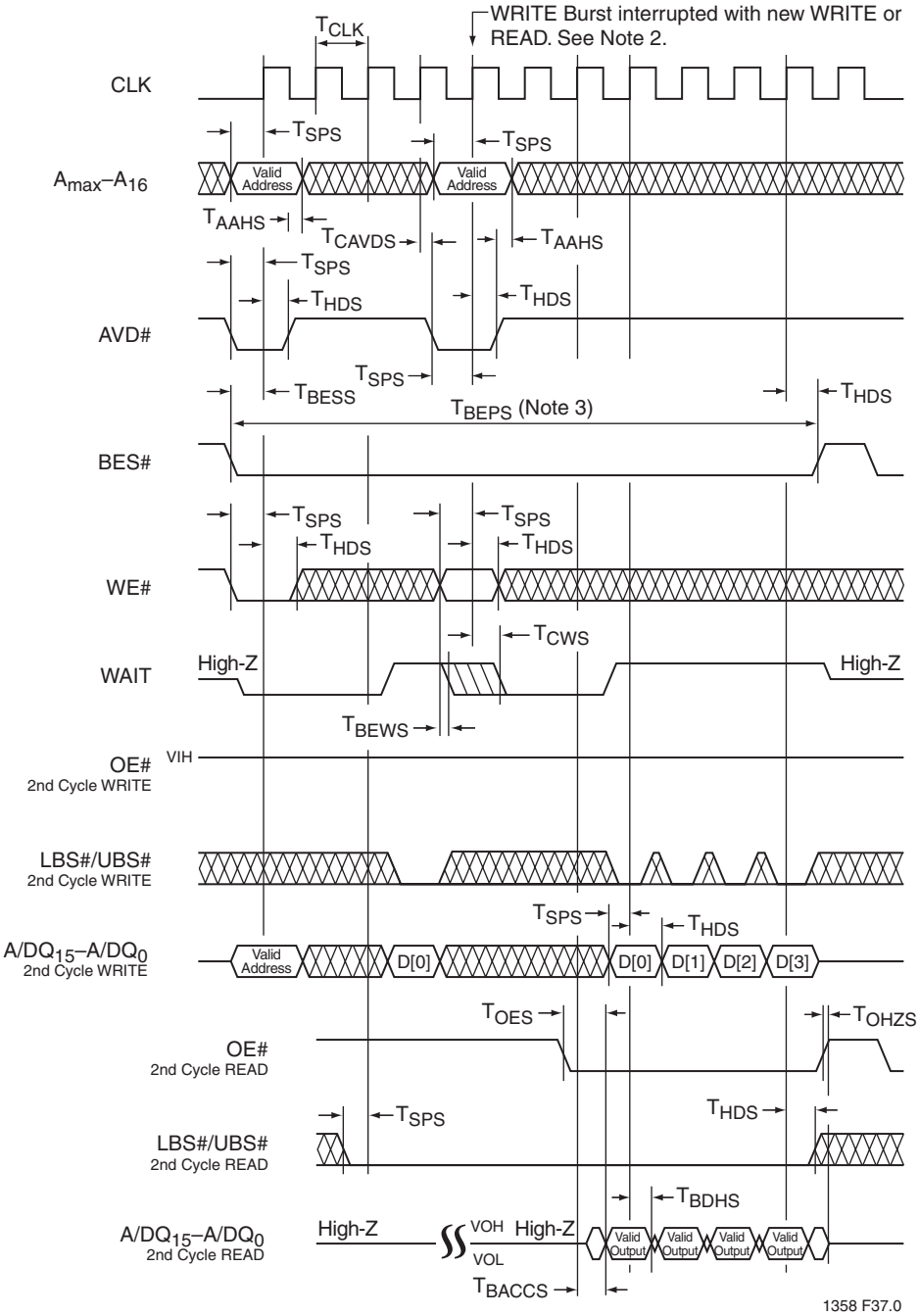
Notes: 1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A refresh opportunity must be provided every T_{BEPS}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked BES# HIGH, or b) BES# HIGH for longer than 15ns. BES# can stay LOW between burst READ and burst WRITE operations, but BES# must not remain LOW longer than T_{BEPS}. See burst interrupt diagrams for cases where BES# stays LOW between bursts.
3. Only fixed latency requires T_{CAVDS}.

FIGURE 34: PSRAM Burst Write Followed by Burst Read



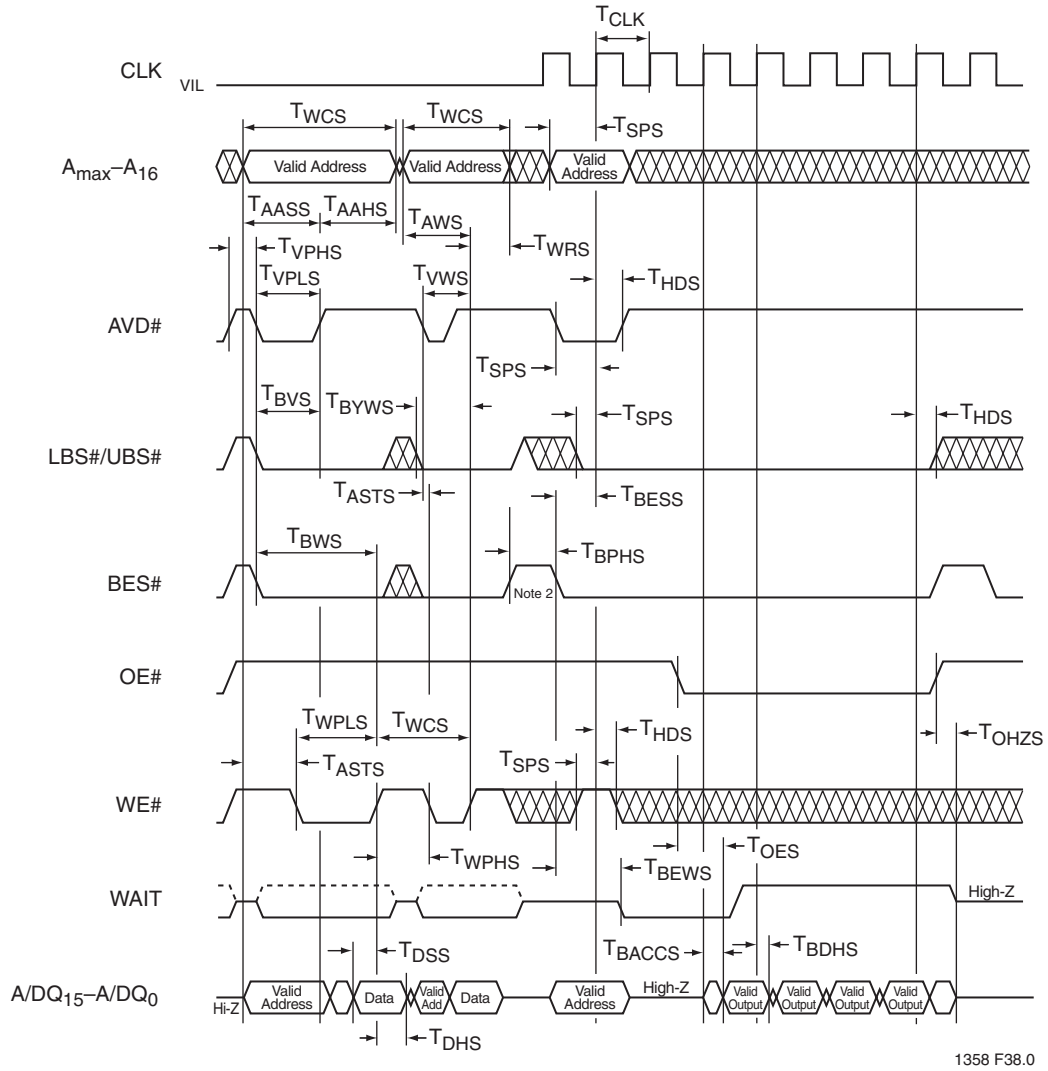
Notes: 1. Non-default BCR settings for burst READ interrupted by burst READ or WRITE: Fixed latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Burst interrupt shown on first allowable clock (i.e., after the first data received by controller).
3. BES# can stay LOW between burst operations, but BES# must not remain LOW longer than T_{BEPS}.

FIGURE 35: PSRAM Burst Read Interrupted by Burst Read or Write



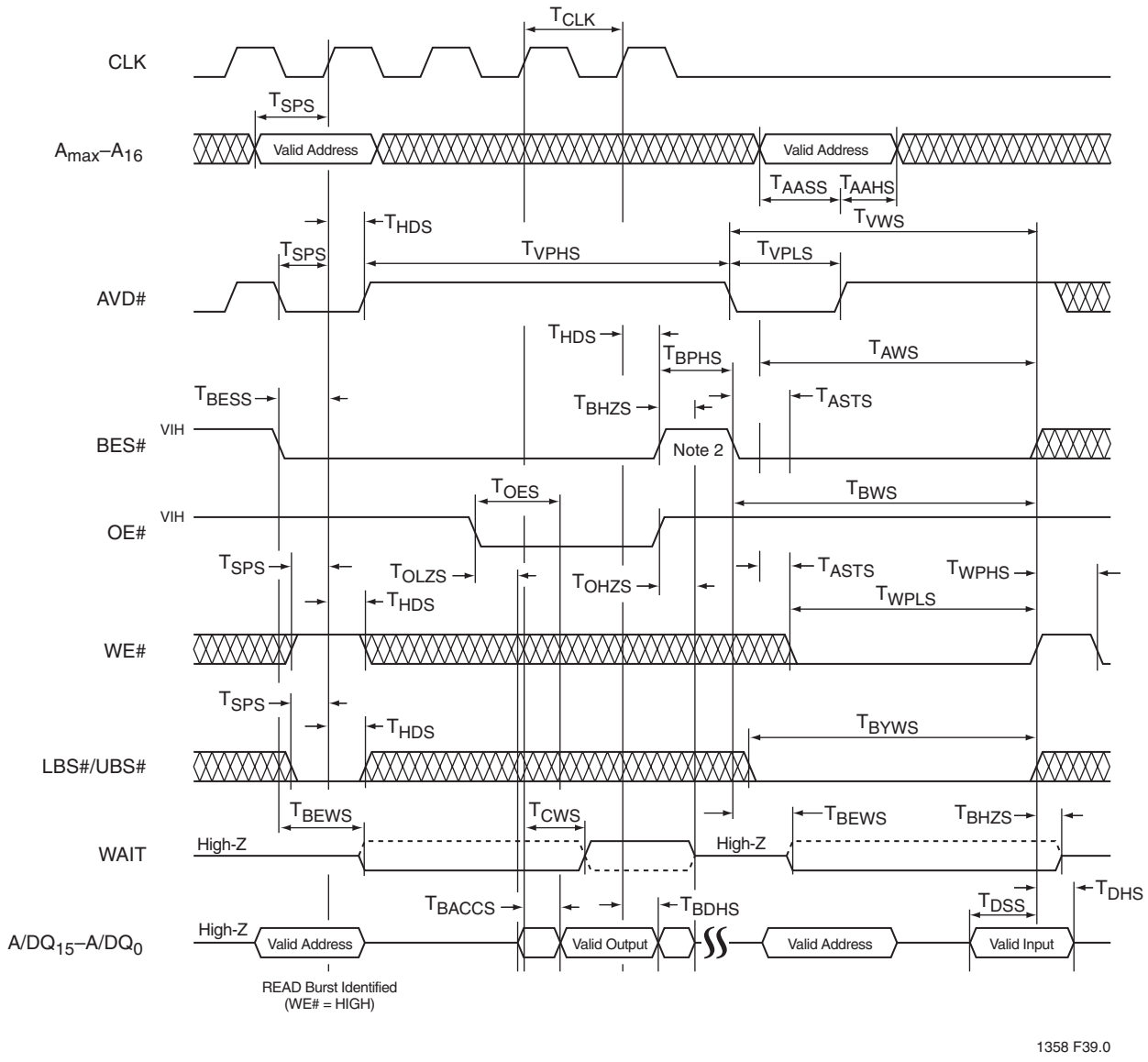
Notes: 1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. BES# can stay LOW between burst operations, but BES# must not remain LOW longer than T_{BEPS}.

FIGURE 36: PSRAM Burst Write Interrupted by Burst Write or Read - Fixed Latency



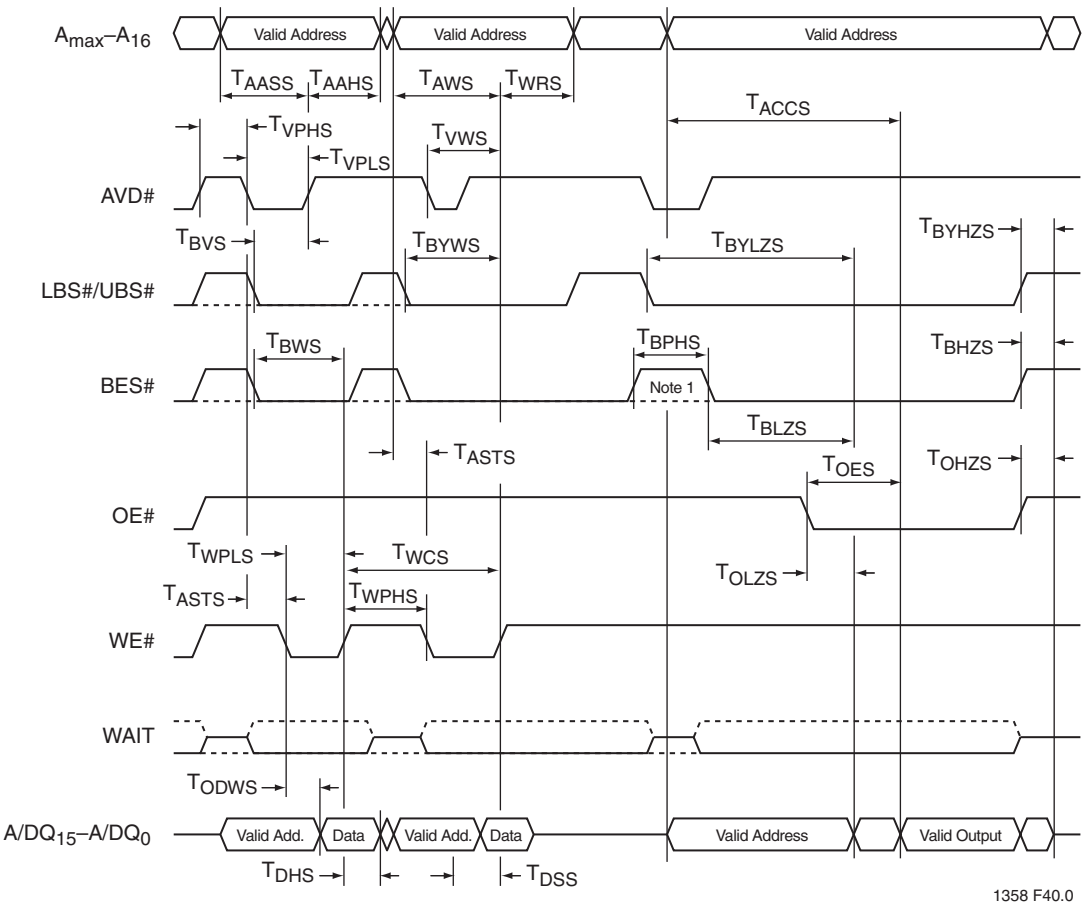
Notes: 1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, BES# must go HIGH. BES# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every T_{BEPS}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked BES# HIGH, or b) BES# HIGH for longer than 15ns.

FIGURE 37: PSRAM Asynchronous Write Followed by Burst Read



Notes: 1. Non-default BCR settings for burst READ followed by asynchronous WRITE using AVD#: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, BES# must go HIGH. BES# can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of AVD#. A refresh opportunity must be provided every T_{BEPS}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked BES# HIGH, or b) BES# HIGH for longer than 15ns.

FIGURE 38: PSRAM Burst Read Followed by Asynchronous Write Using AVD#



Note: 1. When configured for synchronous mode (BCR[15] = 0), BES# must remain HIGH for at least 6ns (T_{BPHS}) to schedule the appropriate refresh interval. Otherwise, T_{BPHS} is only required after BES#-controlled WRITEs.

FIGURE 39: PSRAM Asynchronous Write Followed by Asynchronous Read

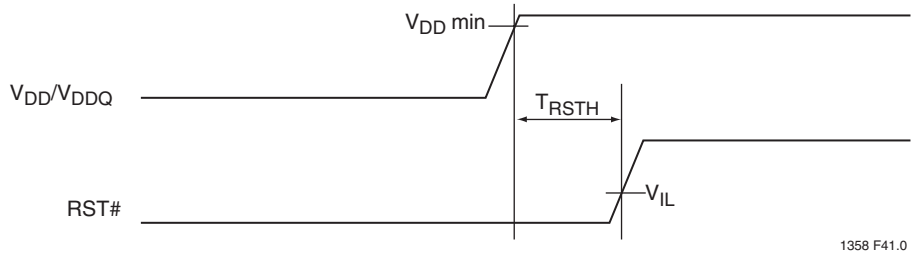


FIGURE 40: V_{DD} Power Up Diagram

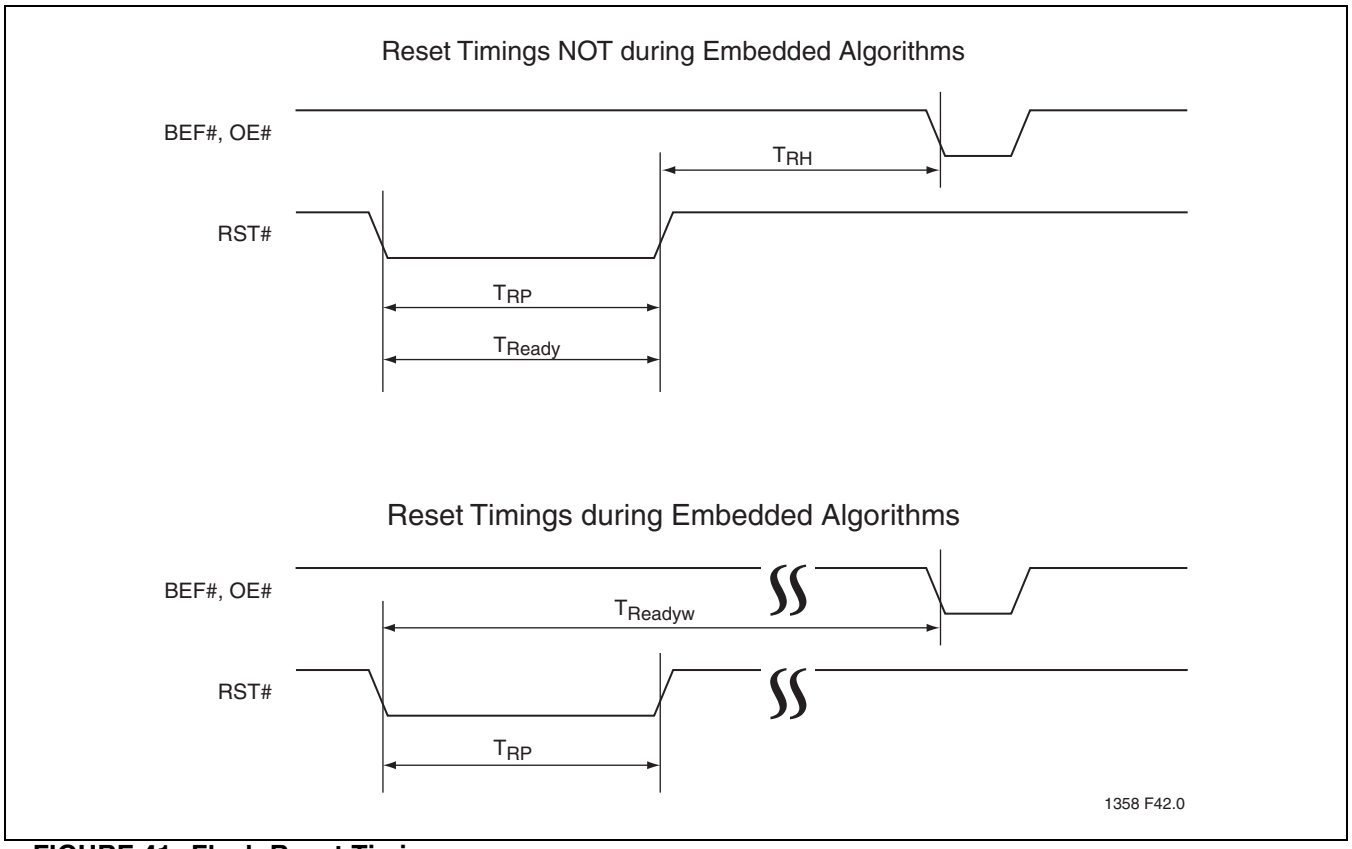


FIGURE 41: Flash Reset Timings

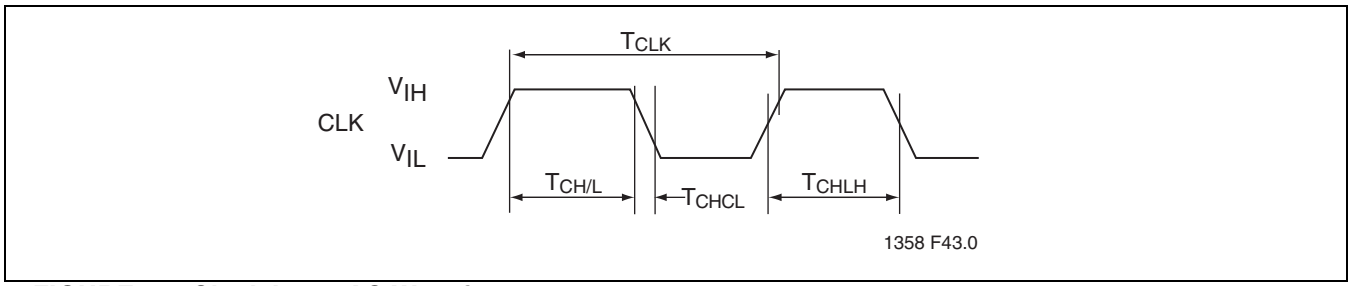
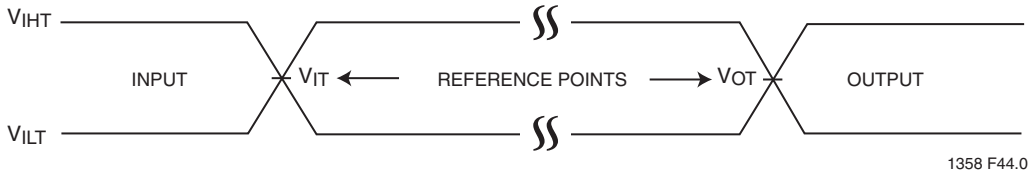


FIGURE 42: Clock Input AC Waveform



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for logic '1' and V_{ILT} (0.1V_{DD}) for logic '0.' Measurement reference points for inputs and outputs are V_{IT} (0.5VDD) and V_{OT} (0.5V_{DD}). Input rise and fall times 10%–90% are <5ns.

Note: $V_{IT} = V_{INPUT}$ Test
$V_{OT} = V_{OUTPUT}$ Test
$V_{IHT} = V_{INPUT\ HIGH}$ Test
$V_{ILT} = V_{INPUT\ LOW}$ Test

FIGURE 43: Flash AC Input/Output Reference Waveforms

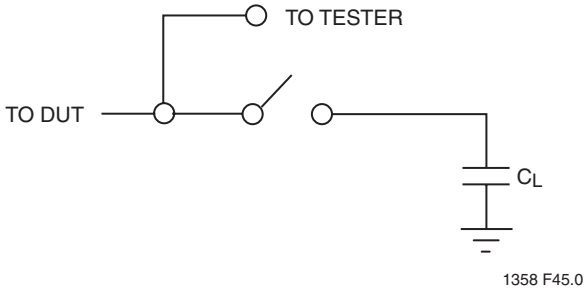
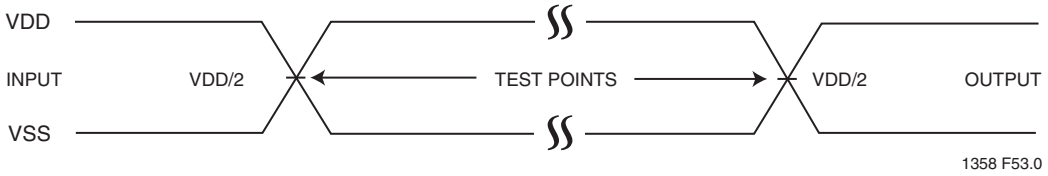
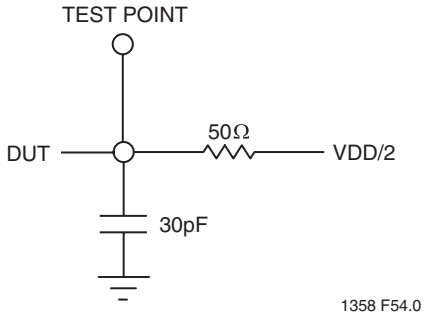


FIGURE 44: Flash Test Load Example



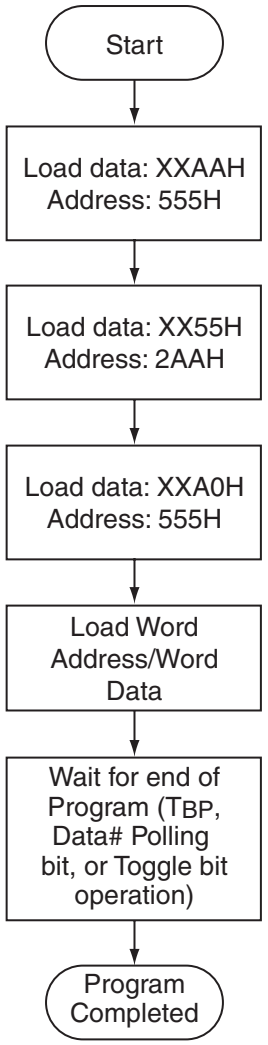
Note: AC test inputs are driven at V_{DD} for logic '1' and V_{SS} for logic '0.' Measurement reference points for inputs and outputs are $V_{DD/2}$ and $V_{DD/2}$. Input rise and fall times 10%–90% are <1.6ns.

FIGURE 45: PSRAM AC Input/Output Reference Waveforms



Note: All test are performed with the outputs configured for default setting of full drive strength (BCR[5:4]=00b).

FIGURE 46: PSRAM AC Test Load Example



Note: X can be V_{IL} or V_{IH}, but not other value.

FIGURE 47: Flash Word-Program Algorithm

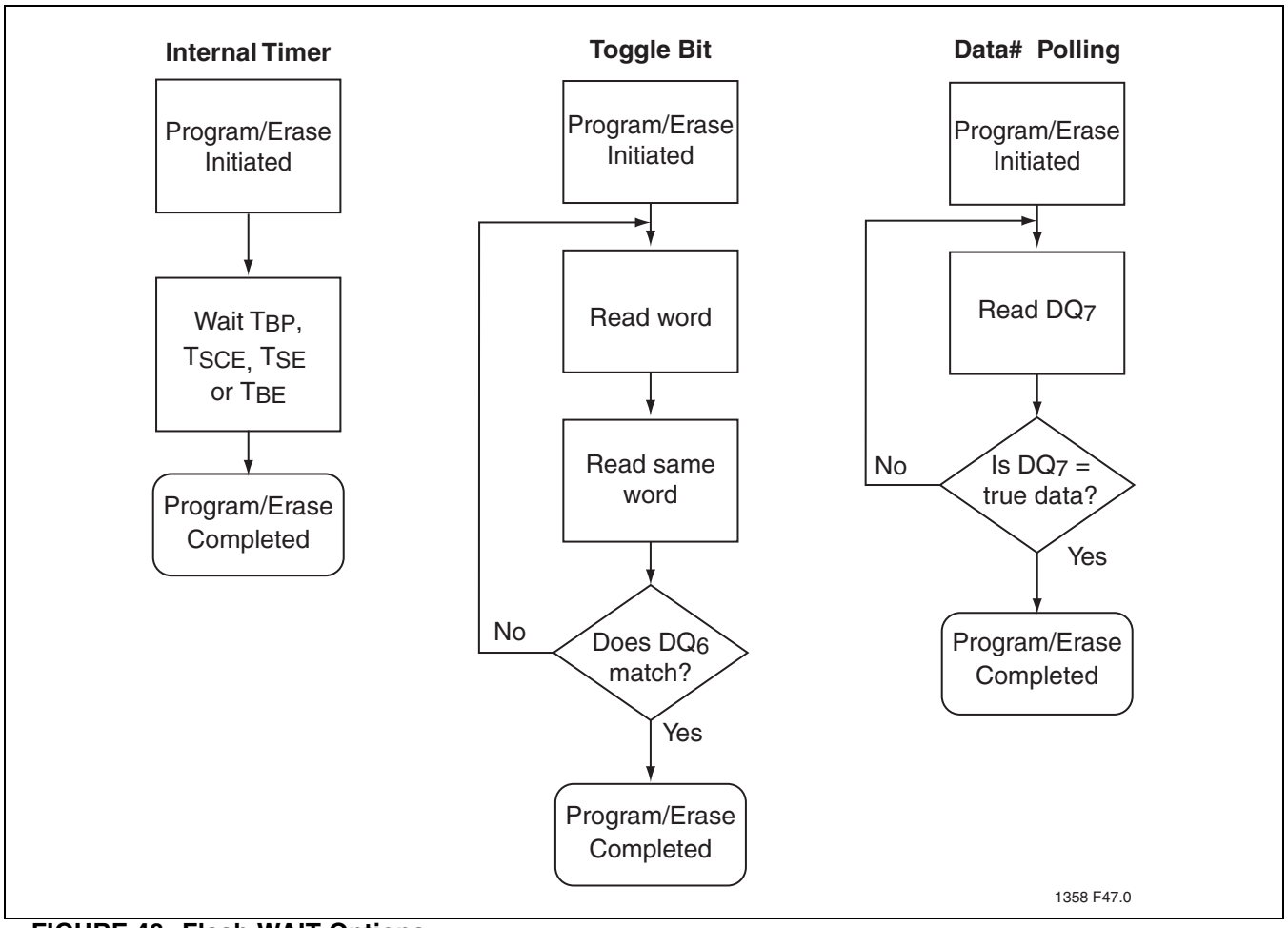
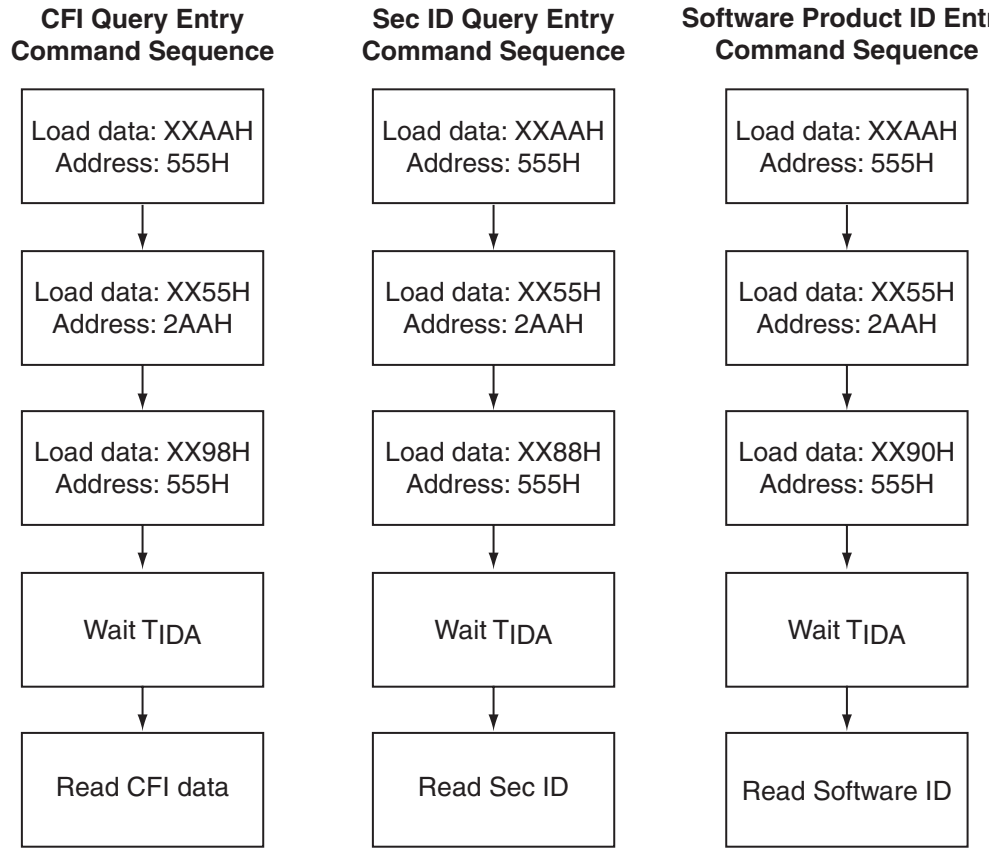
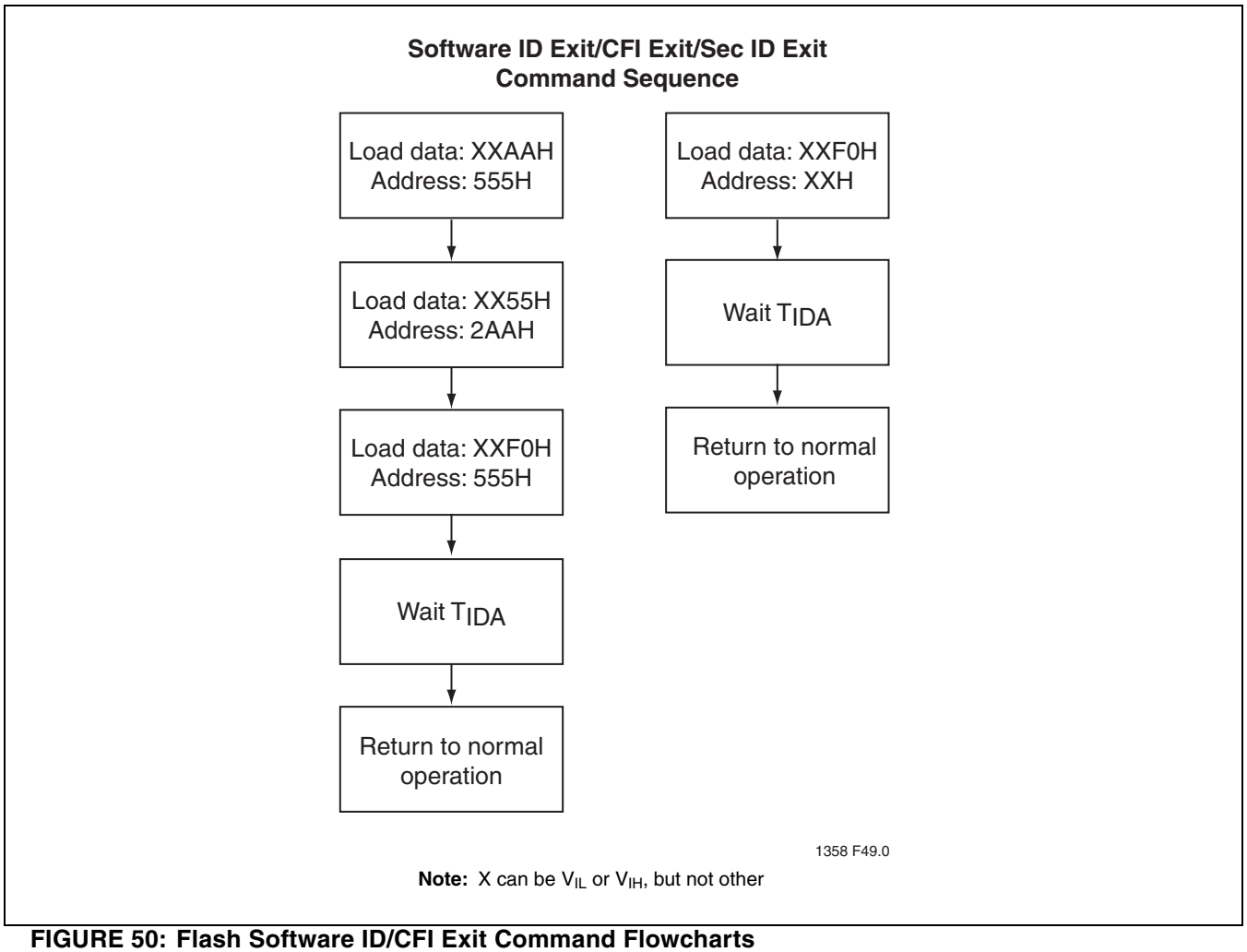


FIGURE 48: Flash WAIT Options



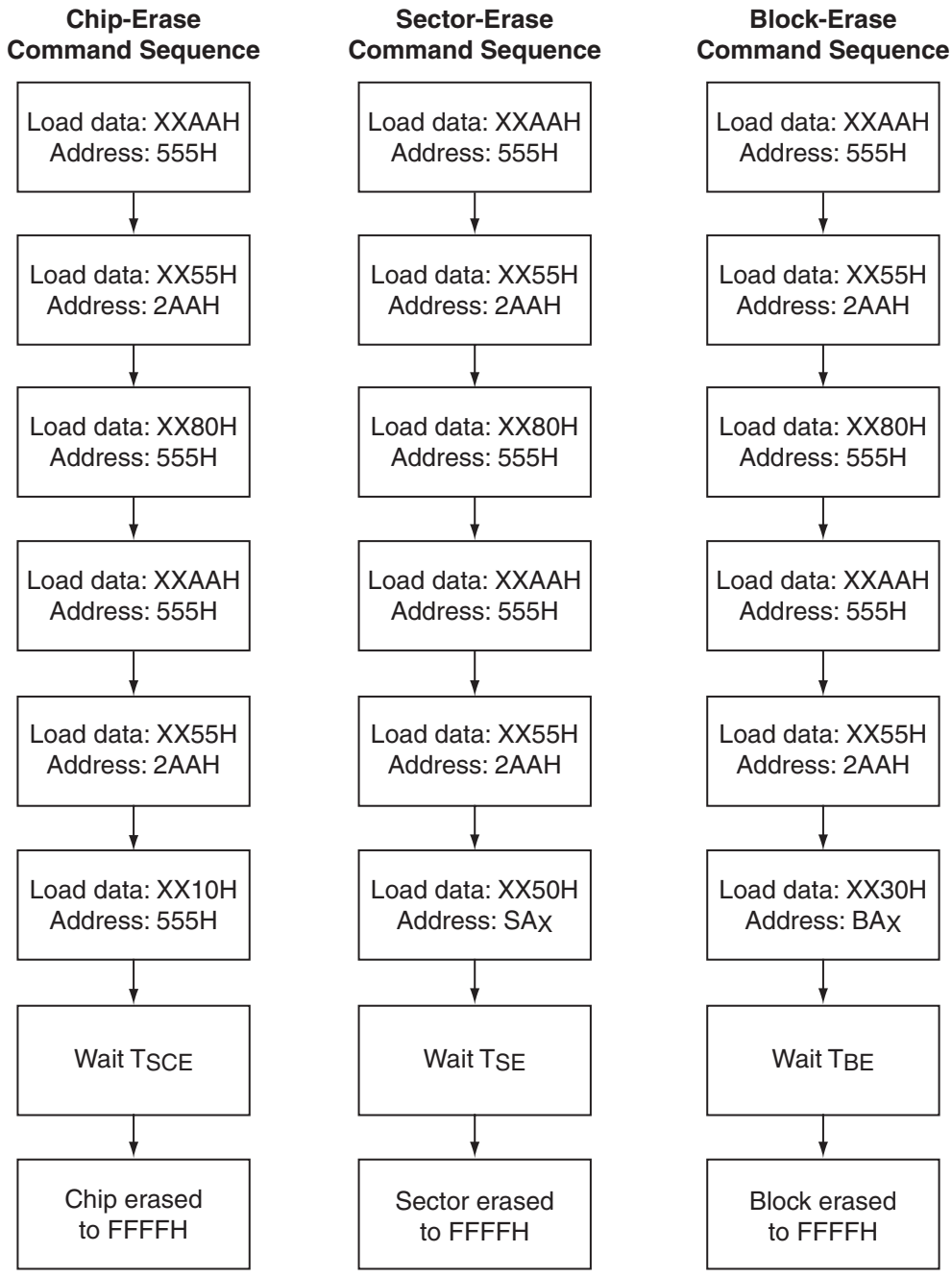
Note: X can be V_{IL} or V_{IH}, but not other value.

FIGURE 49: Flash Software ID/CFI Entry Command Flowcharts



Note: X can be V_{IL} or V_{IH}, but not other

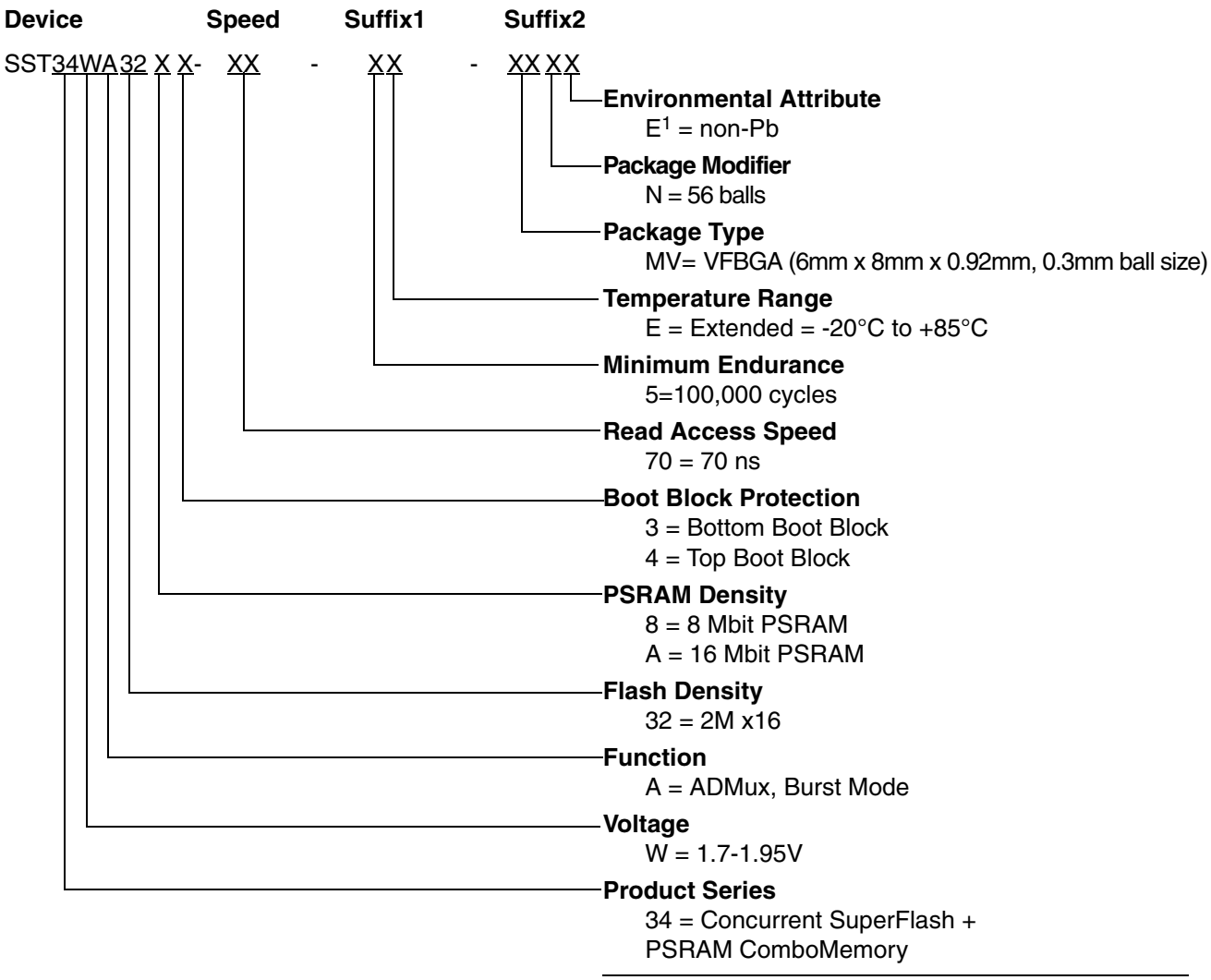
FIGURE 50: Flash Software ID/CFI Exit Command Flowcharts



Note: X can be V_{IL} or V_{IH}, but not other value.

FIGURE 51: Flash Erase Command Sequence

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST34WA32A3

SST34WA32A3-70-5E- MVNE

Valid combinations for SST34WA32A4

SST34WA32A4-70-5E- MVNE

Valid combinations for SST34WA3283

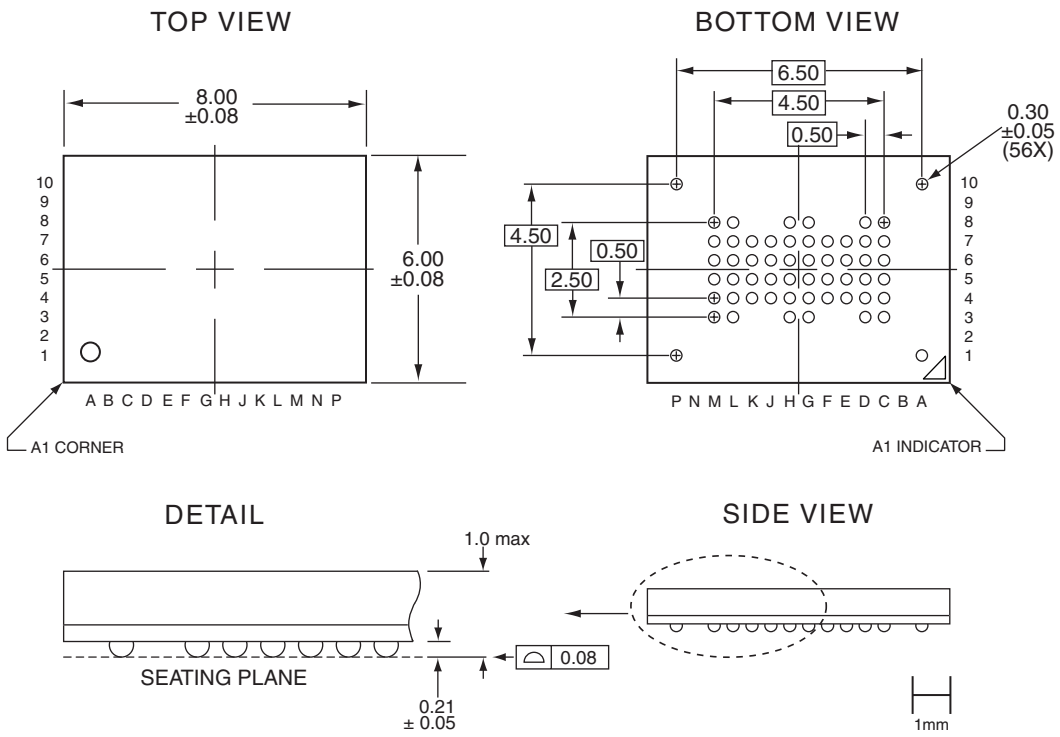
SST34WA3283-70-5E- MVNE

Valid combinations for SST34WA3284

SST34WA3284-70-5E- MVNE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGE DIAGRAMS



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-225, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.08 mm
4. Ball opening size is 0.25 mm (± 0.05 mm)

56-fbga-MVN-6x8-1.0

FIGURE 52: 56-Ball Very Fine-pitch Ball Grid Array (VFBGA) 6mm x 8mm
SST Package Code: MVN

TABLE 41: Revision History

Number	Description	Date
00	• Initial Release	Sep 2007
01	• Removed Partial Array Refresh section, page 20 • Edited Table 13, page 25	Nov 2007