

## ADSST-EM-3035

### FEATURES

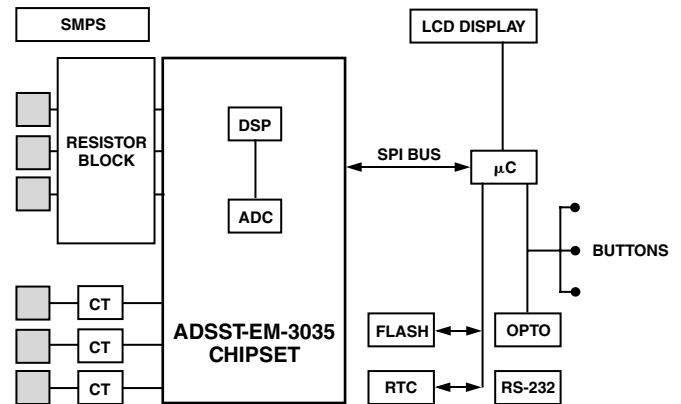
**IEC 687, Class 0.5 and Class 0.2 Accuracy**  
**ANSI C12.1**  
**IEC 1268, Requirements for Reactive Power**  
**Configurable as Import/Export or Import Only**  
**Simultaneous Measurement of:**  
 Active Power and Energy—Import and Export  
 Reactive Power and Energy  
 Apparent Power  
 Power Factor for Individual Phases and Total Frequency  
 RMS Voltage for All Phases  
 RMS Current for All Phases  
 Harmonic Analysis for Voltage and Current  
 All Odd Harmonics up to 21st Order  
**Interface with a General Purpose Microcontroller**  
**User-Friendly Calibration of Gain Offset and Phase and Nonlinearity Compensation on CTs (Patent Pending)**  
**Two Programmable Output E-Pulses**  
**Programmable E-Pulse Constant from 1,000 Pulses/kWh to 20,000 Pulses/kWh**  
**15 kHz Sampling Frequency**  
**Tamper-Proof Metering**  
**Single 5 V Supply**

### GENERAL DESCRIPTION

The ADSST-EM-3035 Chipset consists of a fast and accurate 6 channel, 16-bit sigma-delta analog-to-digital converter ADSST-73360AR (ADC), an efficient digital signal processor ADSST-2185KST-133 (DSP), and Metering Software. The ADC and DSP are interfaced together to simultaneously acquire voltage and current samples on all the three phases and perform mathematically intensive computations to accurately calculate the Powers, Energies, Instantaneous Quantities, and Harmonics. The chipset could be interfaced to any general-purpose microprocessor to develop state of the art polyphase or Tri-vector energy metering solution in accordance with IEC 1036, IEC 687, or ANSI C12.1.

All calibrations are done in digital domain and no trimming potentiometers are required.

### FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
 Tel: 781/329-4700 [www.analog.com](http://www.analog.com)  
 Fax: 781/326-8703 © Analog Devices, Inc., 2002

# ADSST-EM-3035

## ADSST-2185KST-133 (DSP) SPECIFICATION

### FEATURES

- 30 ns Instruction Cycle 33 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- Three-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 100 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode
- ADSP-2100 Family Code Compatible, with Instruction Set Extensions
- 40 kBytes of On-Chip RAM, Configured as 8 KWords On-Chip Program Memory RAM and 8 KWords On-Chip Data Memory RAM
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 100-Lead TQFP
- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)
- 4 MBytes Byte Memory Interface for Storage of Data Tables and Program Overlays
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
- Programmable Memory Strobe and Separate I/O Memory Space Permits Glueless System Design (Mode Selectable)
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or through Internal DMA Port
- Six External Interrupts
- 13 Programmable Flag Pins Provide Flexible System Signaling
- UART Emulation through Software SPORT Reconfiguration
- ICE-Port Emulator Interface Supports Debugging in Final Systems

### GENERAL DESCRIPTION

The ADSST-2185KST-133 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSST-2185KST-133 combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSST-2185KST-133 integrates 40 kBytes of on-chip memory configured as 8 Kwords (24-bit) of program RAM and 8 Kwords (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSST-2185KST-133 is available in a 100-lead TQFP package.

In addition, the ADSST-2185KST-133 supports instructions that include bit manipulations, bit set, bit clear, bit toggle, bit test new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers, and global interrupt masking for increased flexibility.

Fabricated in a high speed, double metal, low power, CMOS process, the ADSST-2185KST-133 operates with a 25 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSST-2185KST-133's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSST-2185KST-133 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation
- This takes place while the processor continues to:
  - Receive and transmit data through the two serial ports
  - Receive and/or transmit data through the internal DMA port
  - Receive and/or transmit data through the byte DMA port
  - Decrement timer

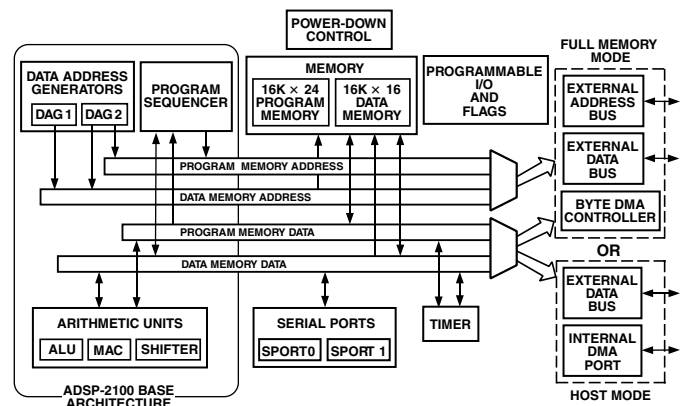


Figure 1. Functional Block Diagram

## ARCHITECTURE OVERVIEW

The ADSST-2185KST-133 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSST-2185KST-133 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSST-2185KST-133. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSST-2185KST-133 executes looped code with zero overhead. No explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from data memory and program memory. Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSST-2185KST-133 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSST-2185KST-133 can fetch an operand from program memory and the next instruction in the same cycle.

When configured in host mode, the ADSST-2185KST-133 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ( $\overline{BR}$ ,  $\overline{BGH}$ , and  $\overline{BG}$ ). One execution mode (Go Mode) allows the ADSST-2185KST-133 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSST-2185KST-133 can respond to 11 interrupts. There are up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master  $\overline{RESET}$  signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSST-2185KST-133 provides up to 13 general purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

### Serial Ports

The ADSST-2185KST-133 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSST-2185KST-133 SPORTs. For additional information on Serial Ports, refer to the *ADSP-2100 Family User's Manual*, Third Edition.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and M-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data-word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data-word. An interrupt is generated after a data buffer transfer.

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- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

## Pin Descriptions

The ADSST-2185KST-133 is available in a 100-lead TQFP package. To maintain maximum functionality and reduce package size and pin count, some serial ports, programmable flags, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during RESET only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Table I. Common-Mode Pins

Pin Name(s)	Number of Pins	Input/Output	Function	Pin Name(s)	Number of Pins	Input/Output	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input	PF0 (Mode A)	1	I	Mode Select Input-Checked only During RESET
$\overline{\text{BR}}$	1	I	Bus Request Input	CLKIN,	2	I	Clock or Quartz Crystal Input
$\overline{\text{BG}}$	1	O	Bus Grant Output	XTAL			
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output	CLKOUT	1	O	Processor Clock Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output	SPORT0	5	I/O	Serial Port I/O Pins
$\overline{\text{PMS}}$	1	O	Program Memory Select Output	SPORT1	5	I/O	Serial Port I/O Pins
$\overline{\text{IOMS}}$	1	O	Memory Select Output	$\overline{\text{IRQ1:0}}$			Edge- or Level-Sensitive Interrupts
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output	F1, F0			Flag In, Flag Out <sup>2</sup>
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output	$\overline{\text{PWD}}$	1	I	Power-Down Control Input
$\overline{\text{RD}}$	1	O	Memory Read Enable Output	PWDACK	1	O	Power-Down Control Output
$\overline{\text{WR}}$	1	O	Memory Read Enable Output	FL0, FL1,	3	O	Output Flags
IRQ2+PF7	1	I	Edge- or Level-Sensitive Interrupt Request <sup>1</sup>	FL2			
$\overline{\text{IRQL0}}$ +PF5	1	I	Level-Sensitive Interrupt Requests <sup>1</sup>	VDD	16	I	VDD and GND
$\overline{\text{IRQL1}}$ +PF6	1	I	Level-Sensitive Interrupt Requests <sup>1</sup>	AND			
$\overline{\text{IRQE}}$ +PF4	1	I	Edge-Sensitive Interrupt Requests <sup>1</sup>	GND			
PF3	1	I/O	Programmable I/O Pin	EX-Port	9	I/O	For Emulation Use
PF2 (Mode C)	1	I	Programmable I/O Pin Mode Select Input-Checked only During RESET				
PF1 (Mode B)	1	I	Mode Select Input-Checked only During RESET				

### NOTES

<sup>1</sup> Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.

<sup>2</sup> SPORT configuration determined by the DSP System Control Register. Software configurable.





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## System Interface

Figure 2 shows typical basic system configurations with the ADSST-2185KST-133, two serial devices, a byte-wide EPROM and optional external program and data overlay memories (mode selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSST-2185KST-133 also provides four external interrupts and two serial ports, or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Additional system peripherals can be added in this mode through the use of external hardware to generate and latch address signals.

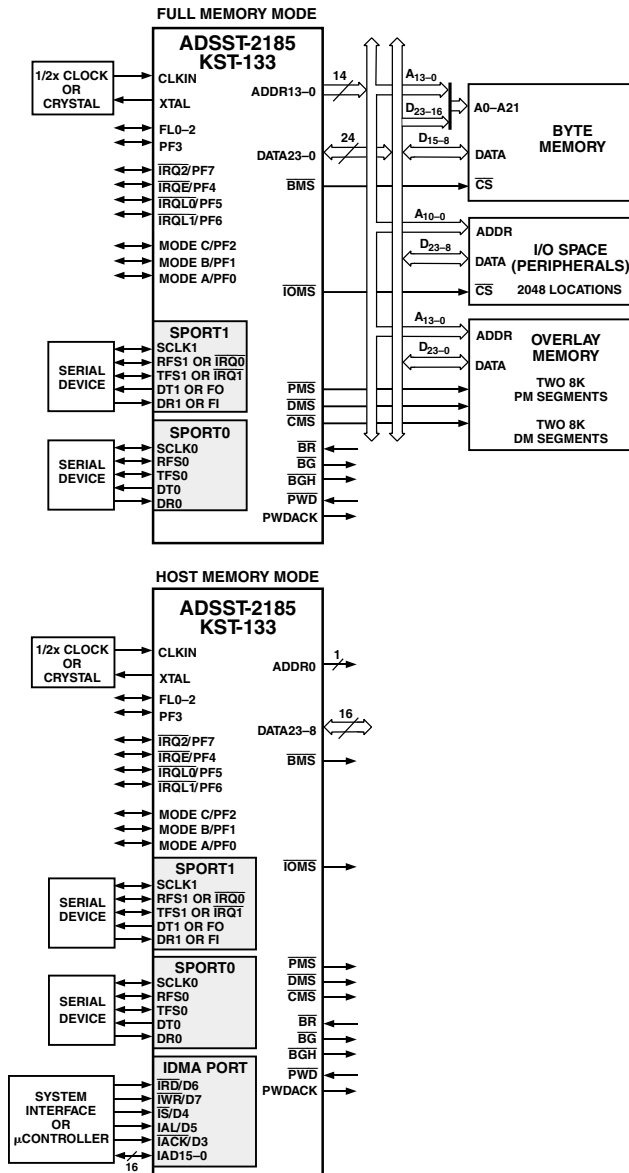


Figure 2. Basic System Interface

## Recommended Operating Conditions

Parameters	A Grade		B Grade		Unit
	Min	Max	Min	Max	
V <sub>DD</sub> Supply Voltage	4.5	5.5	4.5	5.5	V
T <sub>AMB</sub> Ambient Operating Temperature	0	+70	-40	+85	°C

## Clock Signals

Either a crystal or a TTL-compatible clock signal can clock the ADSST-2185KST-133.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual*, Third Edition, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The ADSST-2185KST-133 uses an input clock with a frequency equal to half the instruction rate; a 20.00 MHz input clock yields a 25 ns processor cycle (which is equivalent to 40 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSST-2185KST-133 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

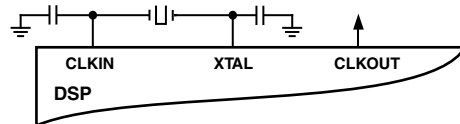


Figure 3. External Crystal Connections

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

## Reset

The  $\overline{\text{RESET}}$  signal initiates a master reset of the ADSST-2185KST-133. The  $\overline{\text{RESET}}$  signal must be asserted during the power-up sequence to assure proper initialization.  $\overline{\text{RESET}}$  during initial power-up must be held long enough to allow the internal clock to stabilize. If  $\overline{\text{RESET}}$  is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid VDD is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence, the  $\overline{\text{RESET}}$  signal should be held low. On any subsequent resets, the  $\overline{\text{RESET}}$  signal must meet the minimum pulsewidth specification,  $t_{\text{RSP}}$ .

The  $\overline{\text{RESET}}$  input contains some hysteresis; however, if you use an RC circuit to generate your  $\overline{\text{RESET}}$  signal, the use of an external Schmidt trigger is recommended. The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When  $\overline{\text{RESET}}$  is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

# ELECTRICAL CHARACTERISTICS

Parameters	Test Conditions	K/B Grade			Unit
		Min	Typ	Max	
V <sub>IH</sub>	High-Level Input Voltage <sup>1, 2</sup>	@ V <sub>DD</sub> = max	2.0		V
V <sub>IH</sub>	High-Level CLKIN Voltage	@ V <sub>DD</sub> = max	2.2		V
V <sub>IL</sub>	Low-Level Input Voltage <sup>1, 3</sup>	@ V <sub>DD</sub> = min		0.8	V
V <sub>OH</sub>	High-Level Output Voltage <sup>1, 4, 5</sup>	@ V <sub>DD</sub> = min I <sub>OH</sub> = -0.5 max @ V <sub>DD</sub> = min	2.4		V
V <sub>OL</sub>	Low-Level Output Voltage <sup>1, 4, 5</sup>	I <sub>OH</sub> = -100 μA <sup>6</sup> @ V <sub>DD</sub> = min I <sub>OL</sub> = 2 mA	V <sub>DD</sub> - 0.3	0.4	V
I <sub>IH</sub>	High-Level Input Current <sup>3</sup>	@ V <sub>DD</sub> = max V <sub>IN</sub> = V <sub>DD</sub> max		10	μA
I <sub>IL</sub>	Low-Level Input Current <sup>3</sup>	@ V <sub>DD</sub> = max V <sub>IN</sub> = 0 V		10	μA
I <sub>OZH</sub>	Three-State Leakage Current <sup>7</sup>	@ V <sub>DD</sub> = max V <sub>IN</sub> = V <sub>DD</sub> max		10	μA
I <sub>OZL</sub>	Three-State Leakage Current <sup>7</sup>	@ V <sub>DD</sub> = max V <sub>IN</sub> = 0 V <sup>8</sup>		10	μA
I <sub>DD</sub>	Supply Current (Idle) <sup>9</sup>	@ V <sub>DD</sub> = 5.0		12.4	mA
I <sub>DD</sub>	Supply Current (Dynamic) <sup>10, 11</sup>	@ V <sub>DDINT</sub> = 5.0 T <sub>AMB</sub> = 25°C t <sub>CK</sub> = 30 ns <sup>11</sup> t <sub>CK</sub> = 25 ns <sup>11</sup>		55 [65]	mA mA
C <sub>I</sub>	Input Pin Capacitance <sup>3, 6, 12</sup>	@ V <sub>IN</sub> = 2.5 V, f <sub>IN</sub> = 1.0 MHz, T <sub>AMB</sub> = 25°C		8	pF
C <sub>O</sub>	Output Pin Capacitance <sup>6, 7, 12, 13</sup>	@ V <sub>IN</sub> = 2.5 V, f <sub>IN</sub> = 1.0 MHz, T <sub>AMB</sub> = 25°C		8	pF

**NOTES**

- <sup>1</sup> Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.
- <sup>2</sup> Input only pins: RESET,  $\overline{\text{BR}}$ , DR0, DR1,  $\overline{\text{PWD}}$ .
- <sup>3</sup> Input only pins: CLKIN,  $\overline{\text{RESET}}$ ,  $\overline{\text{BR}}$ , DR0, DR1,  $\overline{\text{PWD}}$ .
- <sup>4</sup> Output pins: BG, PMS, DMS,  $\overline{\text{BMS}}$ , IOMS, CMS, RD,  $\overline{\text{WR}}$ , PWDACK, A0, DT0, DT1, CLKOUT, FL2-0,  $\overline{\text{BGH}}$ .
- <sup>5</sup> Although specified for TTL outputs, all ADSST-2185KST-133 outputs are CMOS-compatible and will drive to V<sub>DD</sub> and GND, assuming no dc loads.
- <sup>6</sup> Guaranteed but not tested.
- <sup>7</sup> Three-statable pins: A0–A13, D0, D23,  $\overline{\text{PMS}}$ ,  $\overline{\text{DMS}}$ ,  $\overline{\text{BMS}}$ , IOMS, CMS, RD,  $\overline{\text{WR}}$ , DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0, PF7.
- <sup>8</sup> 0 V on  $\overline{\text{BR}}$ , CLKIN inactive.
- <sup>9</sup> Idle refers to ADSST-2185KST-133 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V<sub>DD</sub> or GND.
- <sup>10</sup> I<sub>DD</sub> measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.
- <sup>11</sup> V<sub>IN</sub> = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.
- <sup>12</sup> Applies to TQFP package type
- <sup>13</sup> Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***

Supply Voltage . . . . . -0.3 V to +7.0 V  
 Input Voltage . . . . . -0.3 V to V<sub>DD</sub> + 0.3 V  
 Output Voltage Swing . . . . . -0.3 V to V<sub>DD</sub> + 0.3 V  
 Operating Temperature Range (Ambient) . . . -40°C to +85°C  
 Storage Temperature Range . . . . . -65°C to +150°C  
 Lead Temperature (5 sec) TQFP . . . . . 280°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ENVIRONMENTAL CONDITIONS**

Ambient Temperature Rating:  
 T<sub>AMB</sub> = T<sub>CASE</sub> - (PD × θ<sub>CA</sub>)  
 T<sub>CASE</sub> = Case Temperature in °C  
 PD = Power Dissipation in W  
 θ<sub>JA</sub> = Thermal Resistance (Junction-to-Ambient)  
 θ<sub>JC</sub> = Thermal Resistance (Junction-to-Case)  
 θ<sub>CA</sub> = Thermal Resistance (Case-to-Ambient)

Package	θ <sub>JA</sub>	θ <sub>JC</sub>	θ <sub>CA</sub>
TQFP	50°C/W	2°C/W	48°C/W

# ADSST-EM-3035

## ADSST-73360AR (ADC)

### FEATURES

- Six 16-Bit A/D Converters
- Programmable Input Sample Rate
- Simultaneous Sampling
- 76 dB SNR
- 64 kS/s Maximum Sample Rate
- 83 dB Crosstalk
- Low Group Delay (125  $\mu$ s Typ per ADC Channel)
- Programmable Input Gain
- Flexible Serial Port which Allows Multiple Devices to be Connected in Cascade
- Single (2.7 V to 5.5 V) Supply Operation
- 80 mW Max Power Consumption at 2.7 V
- On-Chip Reference
- 28-Lead SOIC

### GENERAL DESCRIPTION

The ADSST-73360AR is a six-input channel analog front-end processor for power metering. It features six 16-bit A/D conversion provide 76 dB signal-to-noise ratio over a dc to 4 kHz signal bandwidth. Each channel also features a programmable input gain amplifier (PGA) with gain settings in eight stages from 0 dB to 38 dB.

The ADSST-73360AR is particularly suitable for industrial power metering as each channel samples synchronously, ensuring that there is no (phase) delay between the conversions. The ADSST-73360AR also features low group delay conversions on all channels.

An on-chip reference voltage is included with a nominal value of 1.2 V.

The sampling rate of the device is programmable with four separate settings offering 64 kHz, 32 kHz, 16 kHz, and 8 kHz sampling rates (from a master clock of 16.384 MHz).

A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines. The SPORT transfer rate is programmable to allow interfacing to both fast and slow DSP engines.

The ADSST-73360AR is available in 28-lead SOIC.

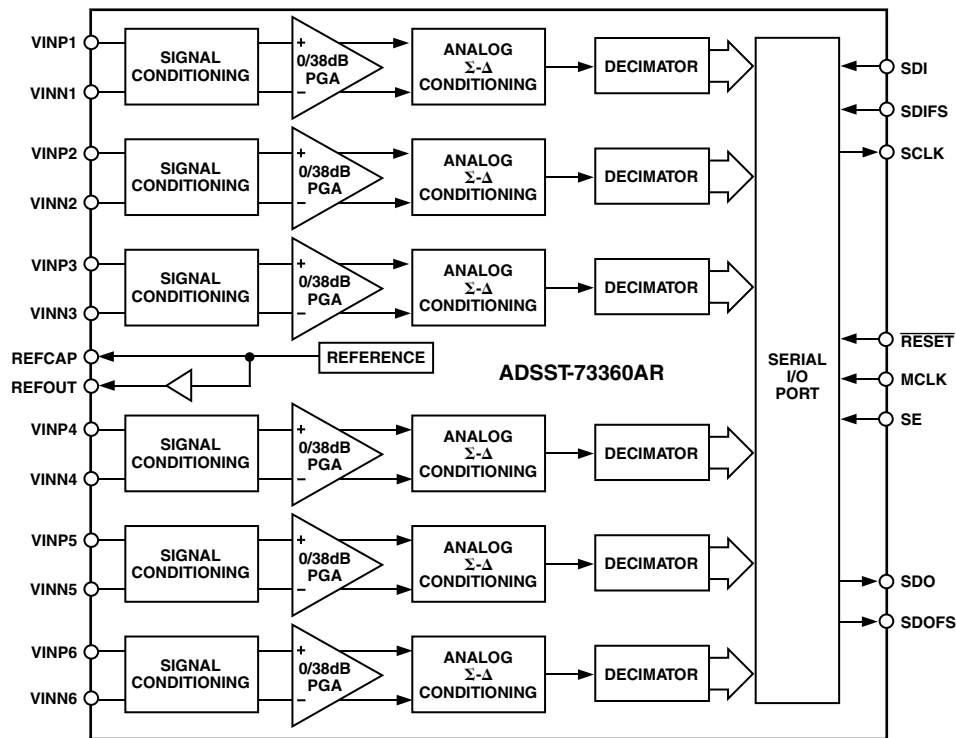


Figure 4. Functional Block Diagram



# SPECIFICATIONS

## ADSST-73360AR

(AVDD = 5 V ± 10%; DVDD = 5 V ± 10%; DGND = AGND = 0 V,  $f_{MCLK} = 16.384$  MHz,  $f_{SCLK} = 8.192$  MHz,  $f_s = 8$  kHz;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted<sup>1</sup>.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>REFERENCE</b>					
<b>REFCAP</b>					
Absolute Voltage, $V_{REFCAP}$		1.25		V	5 VEN = 0
		2.5		V	5 VEN = 1
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from, REFCAP to AGND2
<b>REFOUT</b>					
Typical Output Impedance		130		Ω	
Absolute Voltage, $V_{REFOUT}$		1.25		V	5 VEN = 0, Unloaded
		2.5		V	5 VEN = 1, Unloaded
Minimum Load Resistance	2			kΩ	5 VEN = 1
Maximum Load Capacitance			100	pF	
<b>ADC SPECIFICATIONS</b>					
Maximum Input Range at $V_{IN}^{2,3}$		3.156		V p-p	5 VEN = 1, Measured Differentially
		3.17		dBm	
Nominal Reference Level at $V_{IN}$ (0 dBm0)		2.1908		V p-p	5 VEN = 1, Measured Differentially
		0		dBm	
<b>Absolute Gain</b>					
PGA = 0 dB		+0.1		dB	1.0 kHz
PGA = 38 dB		-0.5		dB	1.0 kHz
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to -50 dBm0
<b>Signal to (Noise + Distortion)</b>					
PGA = 0 dB		76		dB	0 Hz to $f_s/2$ ; $f_s = 8$ kHz
PGA = 38 dB		70		dB	0 Hz to 4 kHz; $f_s = 64$ kHz
<b>Total Harmonic Distortion</b>					
PGA = 0 dB		-86		dB	
PGA = 38 dB		-80		dB	
<b>Intermodulation Distortion</b>					
Idle Channel Noise		-79		dB	PGA = 0 dB
Crosstalk ADC-to-ADC		-76		dB	PGA = 0 dB
		-85		dB	ADC1 Input Signal Level: 1 kHz, 0 dBm0 ADC2 Input at Idle
<b>DC Offset</b>					
DC Offset		20		mV	PGA = 0 dB
<b>Power Supply Rejection</b>					
Power Supply Rejection		-55		dB	Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine
<b>Wave Group Delay<sup>4,5</sup></b>					
		25		µs	64 kHz Output Sample Rate
		50		µs	32 kHz Output Sample Rate
		95		µs	16 kHz Output Sample Rate
		190		µs	8 kHz Output Sample Rate
Input Resistance at $V_{IN}^{2,4}$		25		kΩ <sup>6</sup>	DMCLK = 16.384 MHz
<b>FREQUENCY RESPONSE</b>					
<b>(ADC)<sup>7</sup> Typical Output Frequency (Normalized to <math>f_s</math>)</b>					
0		0		dB	
0.03125		-0.1		dB	
0.0625		-0.25		dB	
0.125		-0.6		dB	
0.1875		-1.4		dB	
0.25		-2.8		dB	
0.3125		-4.5		dB	
0.375		-7.0		dB	
0.4375		-9.5		dB	
> 0.5		< -12.5		dB	

# ADSST-EM-3035

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>LOGIC INPUTS</b>					
V <sub>INH</sub> , Input High Voltage	V <sub>DD</sub> - 0.8		V <sub>DD</sub>	V	
V <sub>INL</sub> , Input Low Voltage	0		0.8	V	
I <sub>IH</sub> , Input Current		-0.5		μA	
C <sub>IN</sub> , Input Capacitance		10		pF	
<b>LOGIC OUTPUT</b>					
V <sub>OH</sub> , Output High Voltage	V <sub>DD</sub> - 0.4		V <sub>DD</sub>	V	I <sub>OUT</sub>   ≤ 100 μA
V <sub>OL</sub> , Output Low Voltage	0		0.4	V	I <sub>OUT</sub>   ≤ 100 μA
Three-State Leakage Current		-0.3		μA	
<b>POWER SUPPLIES</b>					
AV <sub>DD1</sub> , AV <sub>DD2</sub>	4.5		5.5	V	
DV <sub>DD</sub>	4.5		5.5	V	
I <sub>DD</sub> <sup>8</sup>					See Table II

## NOTES

<sup>1</sup>Operating temperature range is as follows: -40°C to +85°C. Therefore, T<sub>MIN</sub> = -40°C and T<sub>MAX</sub> = +85°C.

<sup>2</sup>Test conditions: Input PGA set for 0 dB gain (unless otherwise noted).

<sup>3</sup>At input to sigma-delta modulator of ADC.

<sup>4</sup>Guaranteed by design.

<sup>5</sup>Overall group delay will be affected by the sample rate and the external digital filtering.

<sup>6</sup>The ADCs input impedance is inversely proportional to DMCLK and is approximated by: (4 ∞10<sup>20</sup>)/DMCLK.

<sup>7</sup>Frequency response of ADC measured with input at audio reference level (the input level that produces an output level of -10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.

<sup>8</sup>Test Conditions: no load on digital inputs, analog inputs ac coupled to ground.

Specifications subject to change without notice.

**Table II. Current Summary (AV<sub>DD</sub> = DV<sub>DD</sub> = 3.3 V)**

Conditions	Analog Current	Digital Current	Total Current (Max)	SE	MCLKON ON	Comments
ADCs Only On	16	16	32	1	YES	REFOUT Disabled
REFCAP Only On	0.8	0	0.8	0	NO	REFOUT Disabled
REFCAP and REFOUT Only On	3.5	0	3.5	0	NO	
All Sections Off	0.1	1.9	2.0	0	YES	MCLK Active Levels Equal to 0 V and DV <sub>DD</sub>
All Sections Off	0	0.05	0.06	0	NO	Digital Inputs Static and Equal to 0 V and DV <sub>DD</sub>

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C unless otherwise noted.)

AV<sub>DD</sub>, DV<sub>DD</sub> to GND ..... -0.3 V to +7 V

AGND to DGND ..... -0.3 V to +0.3 V

Digital I/O Voltage to DGND ..... -0.3 V to DV<sub>DD</sub> + 0.3 V

Analog I/O Voltage to AGND ..... -0.3 V to AV<sub>DD</sub> + 0.3 V

Operating Temperature Range Industrial (A Version)

..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

Maximum Junction Temperature ..... 150°C

SOIC, θ<sub>JA</sub> Thermal Impedance ..... 75°C/W

Lead Temperature, Soldering

Vapor Phase (60 sec) ..... 215°C

Infrared (15 sec) ..... 220°C

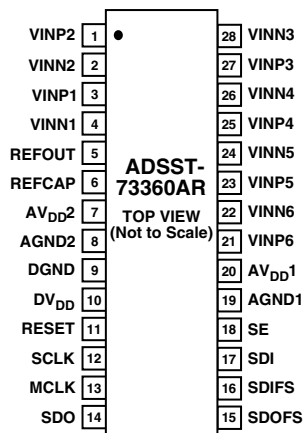
\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSST-EM-3035 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION



## PIN FUNCTION DESCRIPTIONS

Mnemonic	Function	Mnemonic	Function
VINP1	Analog Input to the Positive Terminal of Input Channel 1	<u>RESET</u>	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
VINN1	Analog Input to the Negative Terminal of Input Channel 1	SCLK	Output Serial Clock whose rate determines the serial transfer rate to/from the ADSST73360AR. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number. This integer number being the product of the external master clock rate divider and the serial clock rate divider.
VINP2	Analog Input to the Positive Terminal of Input Channel 2	MCLK	Master Clock Input. MCLK is driven from an external clock signal.
VINN2	Analog Input to the Negative Terminal of Input Channel 2	SDO	Serial Data Output of the ADSST-73360AR. Both data and control information may be output on this pin and are clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
VINP3	Analog Input to the Positive Terminal of Input Channel 3	SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one bit wide and it is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
VINN3	Analog Input to the Negative Terminal of Input Channel 3	SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one bit wide and it is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low.
VINP4	Analog Input to the Positive Terminal of Input Channel 4	SDI	Serial Data Input of the ADSST-73360AR. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.
VINN4	Analog Input to the Negative Terminal of Input Channel 4	SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low. However, the timing counters and other internal registers are at their reset values.
VINP5	Analog Input to the Positive Terminal of Input Channel 5	AGND1	Analog Ground Connection
VINN5	Analog Input to the Negative Terminal of Input Channel 5	AV <sub>DD</sub> 1	Analog Power Supply Connection
VINP6	Analog Input to the Positive Terminal of Input Channel 6		
VINN6	Analog Input to the Negative Terminal of Input Channel 6		
REFOUT	Buffered Reference Output, which has a nominal value of 1.2 V or 2.4 V, the value being dependent on the status of Bit 5 VEN (CRC:7). This pin can be overdriven by an external reference if required.		
REFCAP	A Bypass Capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin.		
AV <sub>DD</sub> 2	Analog Power Supply Connection		
AGND2	Analog Ground/Substrate Connection		
DGND	Digital Ground/Substrate Connection		
DV <sub>DD</sub>	Digital Power Supply Connection		

# ADSST-EM-3035

## Grounding and Layout

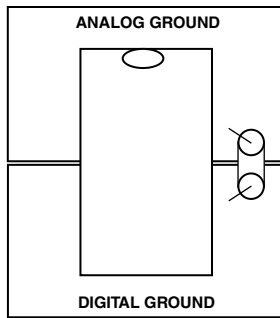


Figure 5. Grounding and Layout

Since the analog inputs to the ADSST-73360AR are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the ADSST-73360AR are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters on the encoder section will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the ADSST-73360LAR ADC is high, and the noise levels from the ADSST-73360AR are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the ADSST-73360AR should be designed so the analog and digital sections are separated and confined to certain sections of the board. The ADSST-73360AR pin configuration offers a major advantage in that its analog and digital interfaces are connected on opposite sides of the package. This facilitates the use of ground planes that can be easily separated, as shown in Figure 5. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place. If this connection is close to the device, it is recommended to use a ferrite bead inductor as shown in Figure 5.

Avoid running digital lines under the device for they will couple noise onto the die. The analog ground plane should be allowed to run under the ADSST-73360AR to avoid noise coupling. The power supply lines to the ADSST-73360AR should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A micro-strip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND

and DGND respectively, with 0.1  $\mu\text{F}$  ceramic capacitors in parallel with 10  $\mu\text{F}$  tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against it. In systems where a common supply voltage drives both the AVDD and DVDD of the ADSST-73360AR, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the ADSST-73360AR and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

NOTE: FOR MORE DETAILS ON ADSST-73360AR, PLEASE REFER TO DATA SHEET OF AD73360

### Interfaces between ADSST-EM-3035 and Microcontroller Overview

The following paragraphs describe the interface between the ADSST-EM-3035 chipset and the microcontroller. The sequence of operations is a critical issue for proper functioning of the two processors on the board. The DSP processor is primarily used to compute various parameters, provide the impulse outputs on the external LEDs and provide automatic gain switching inside the ADC. The microcontroller can collect the data from the chipset for data management for further processing. There are two basic functions that the microcontroller performs in a handshaking mode with the DSP processor:

- Boot loading the DSP with metering software on power up (for non-ROM coded version only)
- Communication with the DSP on SPI to:
  - Send Initialization data on power up after boot loading the DSP with metering software
  - Receive data from DSP during normal operation
  - Receive and send data during calibration

This section describes the Boot loading and SPI operations.

### BOOT LOADING THE DSP PROCESSOR FROM THE MICROCONTROLLER

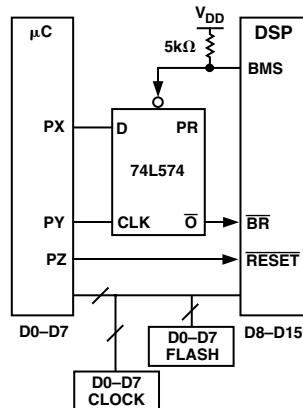
The DSP processor has an internal program memory RAM that supports boot loading. With boot loading, the processor reads instructions from a byte-wide data bus connected to the microcontroller and stores the instructions in the 24-bit wide internal program memory. The host microcontroller, is the source of bytes to be loaded into on-chip memory. The choice of which technique to use depends upon the I/O structure of the host microcontroller, availability of I/O port lines, and the amount of address decoding logic already available in the system. The description here is one of the many ways that this could be configured. However, the software on the microcontroller has been written in way to make optimum use of the configuration.

Figure 6 illustrates the system implementation to allow a microcontroller to boot the DSP processor. The only hardware required is a D-type flip-flop and a 5 k $\Omega$  resistor. The resistor is used to pull the DSP processor's BMS pin (Boot Memory Select) high.

The DSP processor boots using the BDMA option. The BDMA option can be used when pins Mode A, Mode B, and Mode C on the DSP are tied low. With these pins tied low the DSP automatically enters its boot sequence after the processor is reset.

In the sequence of booting the DSP, it has to be loaded with an object code into the internal program memory. The byte wide memory boot code file has the following structure:

- a) 32 words or 96 bytes of the initial header,
- b) 81 words or 243 bytes for initializing BDMA and associated registers,
- c) 6712 words or 20136 bytes of program code.



**Figure 6. System Architecture for Boot Loading DSP Processor From Microcontroller**

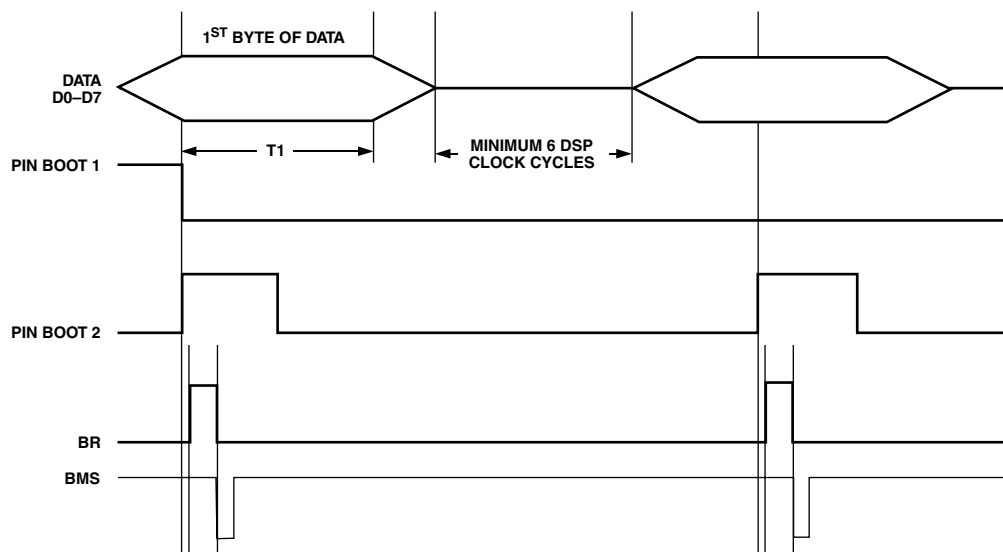
When the DSP is reset with the pins Mode A, Mode B, and Mode C tied low, it enters into the byte wide memory data access mode. The boot loading process will consist of the DSP reading the first 32 words, a small delay, say one millisecond for it execute these 32 words of program. The DSP will then read the next 81 words. After which a small delay, of say one millisecond, will be required for it to execute these 81 words. The DSP will now (with BDMA registers initialized) read the code length also initialized in the previous process. It should be noted that when the DSP reads the 20136 bytes from its port of the

program code, it will overwrite the first 113 words (i.e., 339 bytes). After reading 20136 bytes, it will start execution automatically.

The process of loading the code to the DSP is as follows:

- After the microcontroller is reset, hold DSP in reset by bringing reset pin low.
- Make PX high and clock PY (low to high transition). This will make BR low. In effect, the DSP will not read because it has granted its buses since BR is asserted.
- Put the first byte of the program code on the DSP bus D8 to D15 and deassert BR, which is done by taking PX low and clocking a transition on PY (low to high). Since the DSP buses have been released, it will read the byte and assert BMS. The assertion of BMS will cause the flip-flop to preset (PR on 74LS74) itself and therefore BR is again asserted.
- Continue this process byte by byte for 96 bytes and give a small delay.
- After the delay continue the byte loading process for the next 243 bytes and give a small delay again.
- Continue the byte loading process for 20136 bytes.
- Soon after the last program byte is loaded, the DSP starts execution of the code.

At the start of execution, the DSP waits for uploading of 154 bytes of data consisting of calibration constants (gain & dc offsets), E-pulse constants and filter coefficients. This data has to be sent to the DSP processor on the SPI port. Until the DSP receives the 154 bytes, the actual process of executing the metering code on the DSP does not start. Soon after receiving all the constants (i.e. 154 bytes) the metering process starts. Four dummy bytes have to be sent after the start of execution for the DSP to send back the check sum of its internal code. The microcontroller can use this to verify that the complete metering code has been loaded on the DSP processor properly. The DSP is now ready to provide the computed data on the SPI port.



**Figure 7. Timing Diagram for Boot Loading the DSP Processor**

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## SERIAL PERIPHERAL INTERFACE (SPI) AND CONTROL

The DSP and the microcontroller are interfaced through Serial Peripheral Interface (SPI). The microcontroller is always configured as a master and the DSP as a slave.

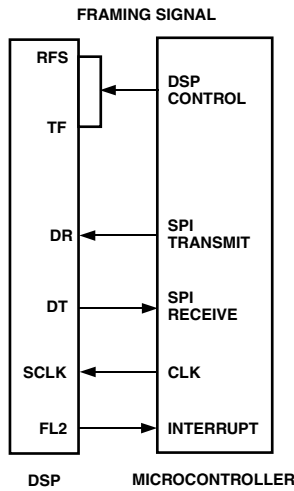


Figure 8. Serial Peripheral Interface and Control

## SPI OPERATION

There are two modes of communication between DSP and microcontroller.

- Microcontroller to DSP (while uploading the initial data of 154 bytes, including four bytes to read checksum of code from DSP, and sending a command)

Bring the DSP\_control pin low, i.e., give a high to low transition. This informs the DSP that the data after this transition is a valid data.

Send the data byte on the microcontroller's SPI port. Since the microcontroller is configured as a master, the clock signal will be generated by the microcontroller and the DSP being a slave will read the data byte in sync with the clock signal. Bring DSP\_control signal back to high state.

- DSP to Microcontroller (while transmitting computed data to the microcontroller)

The DSP during its metering code execution, is ready to give the computed parameters to the microcontroller after every 32 cycles of power line.

To request data from the DSP, the microcontroller sends a request code 45h on the SPI bus.

The DSP then sends a high to low transition on Pin FL2 soon after it completes the next 32 cycles of computation as an indication to the microcontroller that it is ready to transmit most recent data.

Since the microcontroller is a master, it has to now send clock signal to the DSP on the SPI to receive data. For the clock signal to be generated, the microcontroller has to send a dummy byte. The dummy byte (say, 0xFF) should be one that is not recognized by the DSP as a command. The microcontroller may send as many dummy bytes as it requires up to a maximum of 522 bytes for the complete

data train. The data received from the DSP will be in the same sequence as described in Table IV. If the microcontroller does not require all the parameters then it may stop sending dummy bytes at any time.

The diagram below shows the sequence of operation.

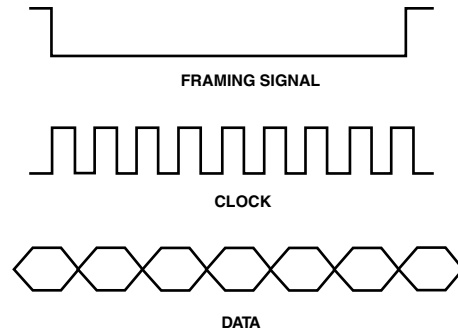


Figure 9. SPI Sequence of Operation

## Quadrant and Other Conventions

The data sent by the DSP is based on the following convention:

- Figure 10 gives the quadrant convention used by the chipset.
- Import means delivered from the utility to the user.
- Export means delivered by the user to the utility.
- Total means total of all three phases.

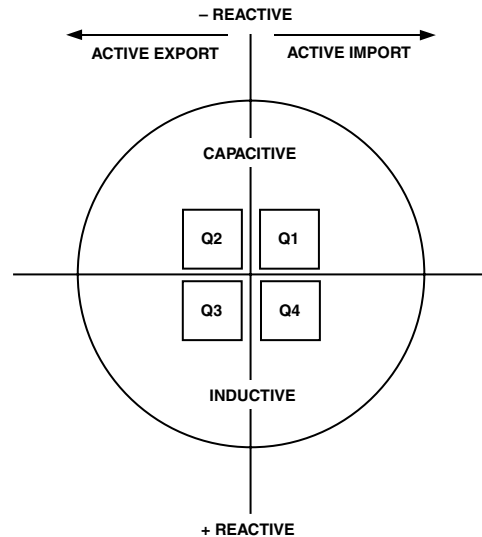


Figure 10.

## Power Up Initialization

To reduce the component count, cost and to give designer a greater flexibility in designing, ADSST-EM-3035 has not been provided with any Nonvolatile Memory to store the calibration constants and initialization data. On power up, after the boot loading of the DSP software, the microcontroller provides the DSP with all the initialization data. After receiving the initialization data the DSP starts the metering. The table below list outs the data that has to be transferred to the DSP on power up.



**Table III. Data Transfer to DSP on Power-Up**

Initialization Gain Constants and DC Offsets	Value	Defaults
R Phase Voltage Gain	2	4000h
Y Phase Voltage Gain	2	4000h
B Phase Voltage Gain	2	4000h
R Phase Current Low Gain	2	4000h
Y Phase Current Low Gain	2	4000h
B Phase Current Low Gain	2	4000h
R Phase Current High Gain	2	4000h
Y Phase Current High Gain	2	4000h
B Phase Current High Gain	2	4000h
R Phase Voltage DC Offset	2	0
Y Phase Voltage DC Offset	2	0
B Phase Voltage DC Offset	2	0
R Phase Current Low Gain DC Offset	2	0
Y Phase Current Low Gain DC Offset	2	0
B Phase Current Low Gain DC Offset	2	0
R Phase Current High Gain DC Offset	2	0
Y Phase Current High Gain DC Offset	2	0
B Phase Current High Gain DC Offset	2	0
E-pulse (Type)*		
Energy Pulse $e\phi = \text{active}$		
$e1 = \text{Apparent}$	1	1
Pulse E-pulse Constant		
Range from 1,000–20,000 Impulse Constant 1 (pulses/kWh)	2	2000
Pulse E-pulse Constant Range from 1,000–20,000	2	2000
<b>PHASE COMPENSATION VARIABLES</b>		
R Phase Coeff for High Current Range	12	0000, 0000, 7FFF, 0000, 0000, 0000
R Phase Coeff for Middle Current Range	12	-Do-
R Phase Coeff for Low Current Range	12	-Do-
Y Phase Coeff for High Current Range	12	-Do-
Y Phase Coeff for Middle Current Range	12	-Do-
Y Phase Coeff for Low Current Range	12	-Do-
B Phase Coeff for High Current Range	12	-Do-
B Phase Coeff for Middle Current Range	12	-Do-
B Phase Coeff for Low Current Range	12	-Do-

\*The first byte to be sent for initialization is 45h followed by all the above tabled parameters in the same sequence.

**Phase Compensation Coefficients**

Three sets of filter coefficients have been provided which will be automatically selected by the DSP during execution based on the maximum current (Imax). In the ADSST-EM-3035, the Imax is fixed at 20 Amps. Therefore the current ranges have been grouped as:

- High current range: From 20 Amps to 7 Amps
- Middle current range: 7 Amps to 1.5 Amps
- Low current range: 1.5 Amps to 0 Amps

**Data from DSP to Microcontroller**

To facilitate easy of operation, the data transfer from DSP to microcontroller has been segregated into multiple blocks. Table IV lists the various data blocks:

**Table IV. Data Transfer Sequence from DSP to Microcontroller**

DATA from DSP on SPI BUS	Byte(s)
REQUEST CODE 45h	1
R Phase Voltage	2
R Phase Current	2
R Phase Active Power	4
R Phase Apparent Power	4
R Phase Inductive Power	4
R Phase Capacitive Power	4
R Phase Power Factor	2
R Phase Active Energy Import	4
R Phase Apparent Energy	4
R Phase Inductive Energy	4
R Phase Active Energy Export	4
R Phase Capacitive Energy	4
Y Phase Voltage	2
Y Phase Current	2
Y Phase Active Power	4
Y Phase Apparent Power	4
Y Phase Inductive Power	4
Y Phase Capacitive Power	4
Y Phase Power Factor	2
Y Phase Active Energy Import	4
Y Phase Apparent Energy	4
Y Phase Inductive Energy	4
Y Phase Active Energy Export	4
Y Phase Capacitive Energy	4
B Phase Voltage	2
B Phase Current	2
B Phase Active Power	4
B Phase Apparent Power	4
B Phase Inductive Power	4
B Phase Capacitive Power	4
B Phase Power Factor	2
B Phase Active Energy Import	4
B Phase Apparent Energy	4
B Phase Inductive Energy	4
B Phase Active Energy Export	4
B Phase Capacitive Energy	4
Total Active Power	4
Total Apparent Power	4
Total Inductive Power	4
Total Capacitive Power	4
Average Power Factor	2
Total Active Energy Import	4
Total Apparent Energy	4
Total Inductive Energy	4
Total Active Energy Export	4
Total Capacitive Energy	4
Frequency	2
R Phase Channel_Present	1
Y Phase Channel_Present	1

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DATA from DSP on SPI BUS	Byte(s)
B Phase Channel_Present	1
R Phase Current Division FlagUnits_flag_R	1
Y Phase Current Division FlagUnits_flag_Y	1
B Phase Current Division FlagUnits_flag_B	1
R Phase Negative Power Flag	1
Y Phase Negative Power Flag	1
B Phase Negative Power Flag	1
R Phase (INDUC/CAP POWER Flag)	1
Y Phase (INDUC/CAP POWER Flag)	1
B Phase (INDUC/CAP POWER Flag)	1

GAIN CONTRASTS AND DC OFFSETS	
R Phase Voltage Gain	2
Y Phase Voltage Gain	2
B Phase Voltage Gain	2
R Phase Current Low Gain	2
Y Phase Current Low Gain	2
B Phase Current Low Gain	2
R Phase Current High Gain	2
Y Phase Current High Gain	2
B Phase Current High Gain	2
R Phase Voltage DC Offset	2
Y Phase Voltage DC Offset	2
B Phase Voltage DC Offset	2
R Phase Current Low Gain DC Offset	2
Y Phase Current Low Gain DC Offset	2
B Phase Current Low Gain DC Offset	2
R Phase Current High Gain DC Offset	2
Y Phase Current High Gain DC Offset	2
B Phase Current High Gain DC Offset	2
DC_Offset Calibration Done (EFh)	1
Total Negative Power Flag	1
Total Inductive Capacitive Flag	1

HARMONIC ANALYSIS DATA	
(All odd harmonics sequenced from fundamental to 21st order, total 11 harmonics of 2 bytes each)	
R Phase Voltage Components Magnitude	$2 \times 11 = 22$
R Phase Current Components Magnitude	22
R Phase Voltage Components Phase	22
R Phase Current Components Phase	22
Y Phase Voltage Components Magnitude	22
Y Phase Current Components Magnitude	22
Y Phase Voltage Components Phase	22
Y Phase Current Components Phase	22
B Phase Voltage Components Magnitude	22
B Phase Current Components Magnitude	22
B Phase Voltage Components Phase	22
B Phase Current Components Phase	22

**Table V. Interpretation of the Voltage Data**

Phase Voltage Data from DSP		
Hex (2 byte)	Decimal	Voltage
5A10h	23056	230.56 V

**Table VI. Interpretation of the Current Data**

Line Current Data from DSP		Unit flag_X (X = R/Y/B)	Current
Hex (2 Byte)	Decimal		
278Bh	10123	1	1.0123 A
278Bh	10123	0	10.123 A

**Frequency Data from DSP**

The frequency data is with two decimal places. This means that the value has to be divided by 100 to get the frequency. For example, if DSP data = 139Fh (decimal value = 5023), then the frequency is 50.23 Hz

**Interpretation of the Power Data**

As in the case of current and voltages, described above, all the power data supplied by DSP has to be interpreted, as shown in Table VII.

The data received from the DSP is in a 4-byte format. The least significant word comes first and the most significant word comes last, e.g., 000D1C4A will come as 1C4A000D and this word reversal has to be performed by the controller.

**Table VII. Interpretation of the Power Data**

Power Data from DSP		
Hex (4-Byte)	Decimal	Power
000D1C4A	859210	859.210 W

**Interpretation of the Power Factor Data**

The DSP data for power factor has a resolution up to four decimal places. To get the value of Power Factor the DSP data has to be divided by 10,000.

**Table VIII. Interpretation of the Power Factor Data**

Power Factor Data from DSP		
Hex (2-Byte)	Decimal	Power Factor
1388h	5000	0.5

**Interpretation of the Energy Data**

The DSP data for energy has a resolution up to four decimal places. To get the value of Energy the DSP data has to be divided by 10,000.

**Table IX. Interpretation of the Energy Data**

Energy Data from DSP		
Hex (4-Byte)	Decimal	Energy
000D1C4Ah	859210	85.9210 kWh

## Interpretation of Harmonics Data

Each harmonic data from DSP is two byte wide. The voltage and phase angle values have a resolution of up to second decimal place and the current has up to third decimal place.

## INPUT SECTION

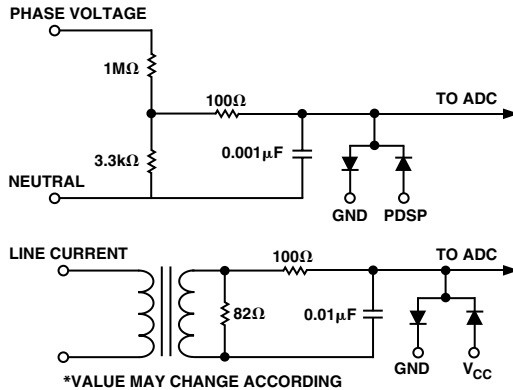


Figure 11. Input Section

ADSST-73360AR has an input range of  $V_{REF} + (V_{REF} \times 0.6525)$  to  $V_{REF} - (V_{REF} \times 0.6525)$  V p-p (0.856 V to 4.14 V for 2.5 V  $V_{REF}$ ). This limit defines the resistance network on the potential circuits and the burden resistance on the secondary side of the CT. ADSST-73360AR being a unipolar ADC the ac, potential, and current have to be offset by a desired dc level. The reference design has a dc offset of 2.5 V. This limits the p-p signal range of potential and current to  $\pm 1.64$  V peak or 1.16 V rms.

For details please refer to the data sheet of AD73360.

### Potential Section

The selection of potential divider circuit should be such that it can:

- Handle high surge voltages
- Should have minimum VA burden
- Give approximately 0.656 V rms output at nominal voltage such that it sufficiently takes care of over voltage.
- The reference design has 1 MΩ and 3.3 kΩ resistance network.

### Current Section

The selection of CT ratio and burden resistance should be such that it can

- Handle the complete dynamic range for the current signal input.
- Give around 1 V(0-pk) output at maximum current such that it sufficiently takes of loads with low crest factors and current surges.

The reference design has a CT with turn ratio of 1:2500 and burden resistance of 82 Ω. This generates 0.656 V rms or 0.928 V (0-pk) at 20 amps current. This leaves enough margins for current pulses or low crest factor loads, such as electronic loads such as SMPS.

The maximum current can be up to 32.767 amps.

## CALIBRATION

ADSST-EM-3035 Chipset has a highly advance calibration routines embedded into the software. Easy of calibration is the philosophy in ADSST-EM-3035 Chipset. ADSST-EM-3035 chipset enables dc offset and gain computation on the voltage and current channels and also performs phase and nonlinearity compensation on the current transformer. Calibrations for power is done internally and no extra procedure is required for it. This section describes the calibration procedure required.

### Voltage Gain Calibration

To calibrate voltage channel:

- Inject a known voltage ( $V_I$ ) to the meter based on ADSST-EM-3035
- Note the voltage read by meter say VM
- Voltage gain coefficient =  $(V_I/V_M) \times 0x4000$ .
- The calculated coefficients are to be communicated to the microcontroller for storage.
- Repeat the same procedure for all the three channels
- Note: Where 0x4000 is default coefficient in hex

### Current Gain Calibration

The Current Gain calibration is performed at two current settings to compute two current gain coefficients, namely current high gain and current low gain coefficients. In all six current gain coefficients are calculated for all the three phase currents. The gains are calculated at:

- $I_1 = 20$  A
- $I_2 = 5$  A

Inject the meter with current value  $I_1$

Note the value of the current sent by meter ( $I_M$ )

Current low gain coefficient =  $(I_1/I_M) \times 0x4000$

Inject the meter with  $I_2$  current

Note the value of the current sent by meter ( $I_M$ )

Current high gain coefficient =  $(I_2/I_M) \times 0x4000$

The calculated coefficients are to be communicated to the microcontroller for storage

Repeat the procedure for other Phases

### DC Offset Calibration for Voltage and Current

Writing EFh to DSP on SPI initiates the dc offset calibration in the DSP. After 32 cycles the DSP returns back the offset values and sends FEh as a mark of completion on the SPI. The microcontroller has to store the dc offset constants for uploading during power up.

# ADSST-EM-3035

**Table X. DC Offset Calibration Data**

DC-Offset Calibration	Command from Microcontrolled in Hex	Setup Input Voltage and Current
Offset Calibration (All Three Phases)	0xEF	V = Nominal Voltage I = 0

The microcontroller now issues 0x45H command on SPI to the DSP. The DSP sends back Table IV. This table will contain new dc-offset coefficients. The microcontroller should store these coefficients.

### Procedure

- Power up the meter with nominal voltage
- Give command for calculation of the coefficient (EFh) to DSP on SPI.
- Receive the coefficient by sending 0x45 on SPI after waiting at least 1s.
- Store the coefficient

### Phase Compensation

The ADSST-EM-3035 employs a patent pending algorithm for phase compensation and non-linearity. This also reduces the cost of the end product by reducing the cost of the sensing elements i.e., CT. To compensate for the phase non-linearity in CTs, the compensation is performed at three current ranges. The three current ranges for calibration are:

- $20\text{ A} > I_1 > 7\text{ A}$
- $7\text{ A} > I_2 > 1.5\text{ A}$
- $1.5\text{ A} > I_3 > 0\text{ A}$

### Procedure

- The ADSSTCOMP.EXE supplied with the chipset is an executable file for calculation of the phase compensation coefficients.
- Set the voltage equal to 230 V which is the nominal voltage at all phases.
- Inject  $I_1$  current at 0.5 inductive ( $60^\circ$  lagging) in all phases.
- The chipset performs the harmonic analysis by providing information about the magnitude and phase angle for all odd harmonics sequenced from fundamental to 21st order. The DSP sends the phase angle information along with other data as described in Table IV after sending the command 0x45.
- The value of the phase angle for line current A, B, and C is available at the locations 283, 371, and 459 respectively (say  $P_A, P_B, P_C$ ) in the data stream sent by the DSP.

- Calculate the normalized lag value ( $L_A, L_B, L_C$ ) for each phase as under :

$$L_A = \frac{60^\circ - P_A}{1.20} + 2 \quad (1)$$

$$L_B = \frac{60^\circ - P_B}{1.20} + 2 \quad (2)$$

$$L_C = \frac{60^\circ - P_C}{1.20} + 2 \quad (3)$$

- Run ADSSTCOMP.EXE on PC
- Feed the normalized lag value during the execution of ADSSTCOMP.EXE.
- The ADSSTCOMP.EXE will provide six coefficients for each phase and the size of each coefficient is 2 bytes.
- The phase compensation should be performed for the three currents on each phase. These coefficients must be stored in a suitable location such that DSP can get these coefficients on power up in the same sequence as shown in Table III.

### Configuration of Output E-pulses

The ADSST-EM-3035 Chipset provides two pulse outputs

- Configurable for Active energy or Apparent energy
- Reactive energy
- Table III gives the default conditions and configuration for first E-pulse.
- The E-pulse constant is variable from 1,000 pulses/kWh to 20,000 pulses/kWh.
- Example: To set 1,500 pulses/kWh, the new E-pulse constant will be 1,500

### Inaccuracy of the E-pulse

Higher E-pulse constant is always desirable as it reduces the testing time. However, increase in pulses/kWh may increase the error at higher power. The error can be calculated by the given formula.

### General Note About Calibration

- It should be noted that ADSST-EM-3035 does not have any permanent memory and hence all the calibration data are to be stored by the microcontroller and provided to the DSP at the time of power up.
- Before starting the calibration the meter should be supplied with the default calibration constants as specified in the Table III.

- The whole calibration can be done in very few steps as shown in the example below.

Start meter with nominal voltage and calculate dc offset

Set current at 20 A and calculate voltage gain and low current gain for all channels

Set current at 5 A and calculate low current gain for all channels

Set current at  $20\text{ A} < I < 7\text{ A}$  and perform phase compensation for all channels

Set current at  $1.5\text{ A} < I < 7\text{ A}$  and perform phase compensation for all channels

Set current at  $1.5\text{ A} < I < 0\text{ A}$  and perform phase compensation for all channels

## MEASUREMENT ACCURACY

### Overall Accuracy, Power and Energy Measurement

The accuracy figures are measured in nominal conditions unless otherwise indicated. The measurement are taken on the reference design with the given below nominal values.

### Reference Design with $\mu$ Metal CT (0.5 Class)

**Table XI. Nominal Value: Reference Design Parameters**

Parameters	Nominal Value
Nominal Voltage (Neutral to Line) $V_N$	$V_N = 230\text{ V} \pm 1\%$
Max Voltage (Neutral to Line)	300 V
Max Current $I_{MAX}$	$I_{MAX} = 20\text{ A}$
Base Current	$I_n = 5\text{ A}$
Frequency	$F_N = 50\text{ Hz}/60\text{ Hz} \pm 10\%$
Power Factor	1
THD of Voltage	$< 2\%$
Temperature	$23 \pm 2^\circ\text{C}$

**Table XII. Maximum Error (Power and Energies)**

Current	Voltage	PF	Min	Typ	Max	Unit
$0.01\text{ I}_n \leq I < 0.05\text{ I}_n$	$V_N$	1.0		$\pm 0.1$	$\pm 0.2$	%
$0.05\text{ I}_n \leq I < I_{MAX}$	$V_N$	1.0		$\pm 0.1$	$\pm 0.2$	%
$0.02\text{ I}_n \leq I < 0.1\text{ I}_n$	$V_N$	0.5 Lagging		$\pm 0.15$	$\pm 0.35$	%
		0.8 Leading		$\pm 0.15$	$\pm 0.35$	%
$0.1\text{ I}_n \leq I \leq I_{MAX}$	$V_N$	0.5 Lagging		$\pm 0.1$	$\pm 0.2$	%
		0.8 Leading		$\pm 0.1$	$\pm 0.2$	%

**Table XIII. Unbalanced Load Error**

Current	Voltage	PF	Min	Typ	Max	Unit
$0.05\text{ I}_n \leq I \leq I_{MAX}$	$V_N$	1.0		$\pm 0.15$	$\pm 0.2$	%
$0.1\text{ I}_n \leq I \leq I_{MAX}$	$V_N$	0.5 Lagging		$\pm 0.15$	$\pm 0.2$	%

**Table XIV. Voltage Variation Error**

Voltage	Current	PF	Min	Typ	Max	Unit
$V_N \pm 10\%$	$0.05\text{ I}_n \leq I \leq I_{MAX}$	1.0		$\pm 0.05$	$\pm 0.1$	%
$V_N \pm 10\%$	$0.1\text{ I}_n \leq I \leq I_{MAX}$	0.5 Lagging		$\pm 0.05$	$\pm 0.1$	%

**Table XV. Frequency Variation Errors**

Frequency	Current	PF	Min	Typ	Max	Unit
$V_N \pm 10\%$	$0.05\text{ I}_n \leq I \leq I_{MAX}$	1.0		$\pm 0.05$	$\pm 0.1$	%
$V_N \pm 10\%$	$0.1\text{ I}_n \leq I \leq I_{MAX}$	0.5 Lagging		$\pm 0.05$	$\pm 0.1$	%

# ADSST-EM-3035

**Table XVI. Harmonic Distortion Error**

Current	Current	Min	Typ	Max	Unit
10% of Third Harmonic	$0.05 I_n < I < I_{MAX}$		$\pm 0.05$	$\pm 0.1$	%

**Table XVII. Reverse Phase Sequence Error**

Current	Voltage	Min	Typ	Max	Unit
0.1 $I_n$	$V_N$			$\pm 0.05$	%

**Table XVIII. Voltage Unbalance Error**

Current	Voltage	Min	Typ	Max	Unit
$I_n$	$V_N \pm 15$		$\pm 0.1$	$\pm 0.2$	%

**Table XIX. Starting Current**

Voltage	Min	Typ	Max	Unit
$V_N$		0.0007	0.001	$I_n$

**RECOMMENDED OPERATING CONDITIONS**

Parameters	A Grade		B Grade		Unit
	Min	Max	Min	Max	
$V_{DD}$		7	0	7	V
Temperature	0	+70	-40	+85	°C

**ELECTRICAL CHARACTERISTICS OF ADSST-EM-3035  
ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	0.3 V to 7 V
Input Voltage	-0.3 V to $V_{DD} + 0.3$ V
Output Voltage Swing	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

**Ordering Codes**

A Grade: ADSST-EM-3035-BST  
B Grade: ADSST-EM-3035-KST

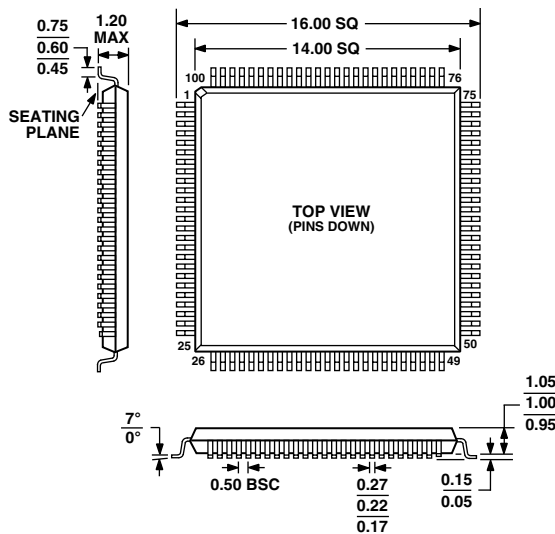
**ORDERING GUIDE**

Model	Temperature Range	Model Included	Package Option
ADSST-EM-3035K	0 to +70°C	ADSST-2185KST-133 ADSST-73360AR	SU-100 RW-28

**OUTLINE DIMENSIONS**

**100-Lead Thin Plastic Quad Flat Package [TQFP]  
(SU-100)**

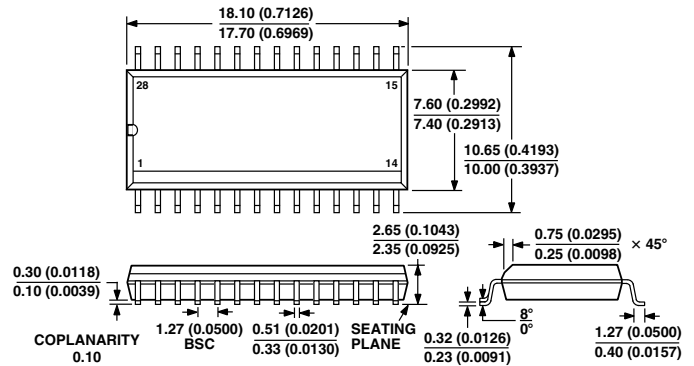
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026AED-HD  
CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED

**28-Lead Standard Small Outline Package [SOIC]  
Wide Body  
(RW-28)**

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN