LDS8865

IXYS Display

6-Channel Ultra Low Dropout LED Driver

FEATURES

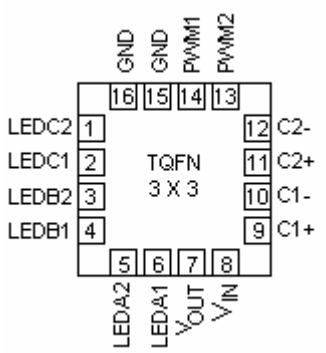
- **Ultra low dropout PowerLite Current Regulator**
- **Multi-mode charge pump: 1x, 1.5x, 2x**
- **Drives up to 6 LEDs at 32mA each**
- **Factory preset current value at each LED bank**
- **PWM brightness control with up to 25,000:1 dimming range at 200 Hz**
- **Power efficiency up to 94%**
- **Low noise input ripple in all charge pump modes**
- **Low current shutdown mode**
- **Soft start and current limiting**
- **Short circuit protection**
- **Thermal shutdown protection**
- **Available in 3 x 3 x 0.8 mm 16-pin TQFN package**

APPLICATION

- **LCD Display Backlight**
- **Cellular Phones**
- **Digital Still Cameras**
- **Handheld Devices**

DESCRIPTION

The LDS8865 is a high efficiency multi-mode fractional charge pump with ultra low feedback



voltage that can drive up to six LEDs. The ultra low dropout PowerLite Current Regulator increases device's efficiency up to 94%.

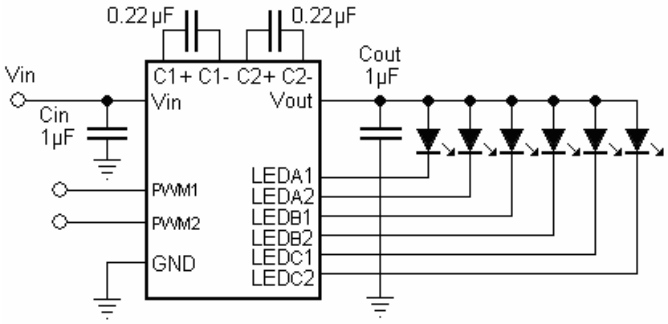
The PWM1/PWM2 logic inputs function as a chip enable and a PWM mode LED brightness control. PWM1 pin contorls LEDA and LEDB banks with four LEDs, while PWM2 controls bank with two LEDs.

The maximum LEDs current is factory preset Every LED bank with two LEDs each is programmable separately in the range from 0.5 to 32mA in 0.5mA steps.

Low noise input ripple is achieved by operating at a constant switching frequency which allows the use of small external ceramic capacitors. The multi-fractional charge pump supports a wide range of input voltages from 2.7V to 5.5V.

The device is available in in 16-lead TQFN 3mm x 3mm package with a max height of 0.8mm.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Vin, LEDx, C1±, C2± voltage	6	V
Vout voltage	6	V
PWM1, PWM2 voltage	Vin + 0.7V	V
Storage Temperature Range	-65 to +160	°C
Junction Temperature Range	-40 to +125	°C
Lead Temperature	300	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Vin	2.7 to 5.5	V
Ambient Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS

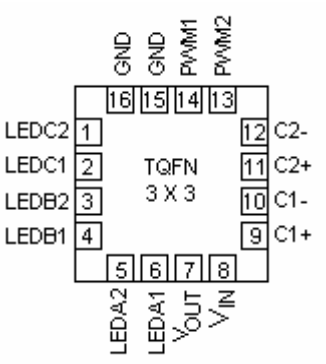
(Over recommended operating conditions unless specified otherwise) Vin = 3.6V, C1 = C2 = 0.22 µF, C_{IN} = C_{OUT} = 1 µF, EN = High, T_{AMB} = 25°C

Name	Conditions	Min	Typ	Max	Units
Quiescent Current	1x mode, no load		1.7	2.5	mA
Shutdown Current	V_{PWM} = 0V			1	µA
LED Current Accuracy	To factory preset value	-5	±3	+5	%
LED Channel Matching	(I_{LED} - I_{LEDAVG}) / I_{LEDAVG}	-5	±1	+5	%
Output Resistance (open loop)	1x mode		0.8		Ω
	1.5x mode		5.5		
	2x mode		6.5		
Charge Pump Frequency	1.5x mode and 2x mode		1.1		MHz
Output short circuit Current Limit	Vout < 0.5V		35		mA
Input Current Limit	Vout > 1V		450		mA
1x to 1.5x, or 1.5x to 2x Transition Thresholds at any LED pin			75	130	mV
1.5x to 1x Mode Transition Hysteresis			600		mV
Transition Filter Delay[1]			800		µs
PWM1, PWM2 pins — Input Leakage			-1		1	µA
PWM1, PWM2 pins — Logic Level — High			1.3			V
PWM1, PWM2 pins — Logic Level — Low					0.4	V
PWM frequency [1]			100		100000	Hz
PWM Pulse HIGH/LOW state			200			ns
PWM Low Time to Shutdown			30			ms
Thermal Shutdown[1]			150			°C
Thermal Hysteresis[1]			20			°C
Under Voltage Lockout (UVLO)			2.2			V
Over Voltage Protection[1]				6.2		V

[1] Sample test only

PIN DESCRIPTION

Pin #	Name	Function
1	LEDC2	LEDC2 cathode terminal
2	LEDC1	LEDC1 cathode terminal
3	LEDB2	LEDB2 cathode terminal
4	LEDB1	LEDB1 cathode terminal
5	LEDA2	LEDA2 cathode terminal
6	LEDA1	LEDA1 cathode terminal
7	V_{OUT}	Charge pump output connected to the LED anodes
8	V_{IN}	Charge pump input, connect to battery or supply
9	C1+	Bucket capacitor 1 Positive terminal
10	C1-	Bucket capacitor 1 Negative terminal
11	C2+	Bucket capacitor 2 Positive terminal
12	C2-	Bucket capacitor 2 Negative terminal
13	PWM2	LEDC bank PWM brightness control
14	PWM1	LEDA and LEDB banks PWM brightness control
15, 16	GND	Ground Reference
TAB	TAB	Bottom Thermal Pad; connect to GND on the PCB



Top view: TQFN 16-lead 3 X 3 mm

PIN FUNCTION

V_{IN} is the supply pin for the charge pump. A small 1µF ceramic bypass capacitor is required between the V_{IN} pin and ground near the device. The operating input voltage range is from 2.5V to 5.5V. Whenever the input supply falls below the under-voltage threshold (2.2 V), all the LED channels are disabled and the device enters shutdown mode.

PWM1, PWM2 are the enable and PWM LED brightness control logic inputs.. Guaranteed levels of logic high and logic low are set at 1.3V and 0.4V respectively. When any of PWM pins is taken high, the device becomes enabled with maximum LED current at associated bank. To place the device into zero current mode, both PWM pins must be held low for more than 30 ms.

V_{OUT} is the charge pump output that is connected to the LED anodes. A small 1µF ceramic bypass capacitor is required between the V_{OUT} pin and ground near the device.

GND is the ground reference for the charge pump. The pin must be connected to the ground plane on the PCB.

C1+, C1- are connected to each side of the ceramic bucket capacitor C1

C2+, C2- are connected to each side of the ceramic bucket capacitor C2

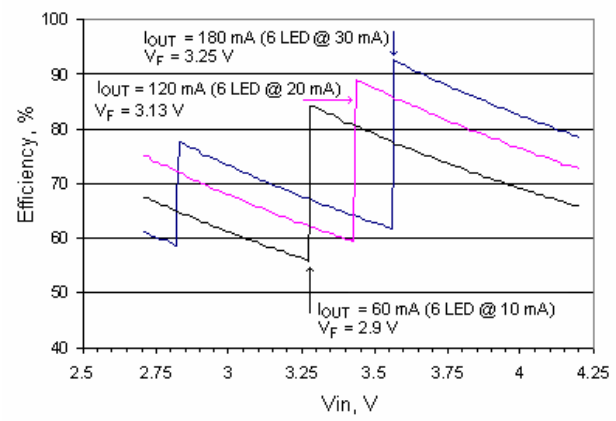
LEDA1 – LEDC2 provide the internal regulated current source for each of the LED cathodes. These pins enter high-impedance zero current state whenever the device is in shutdown mode.

TAB is the exposed pad underneath the package. For best thermal performance, the tab should be soldered to the PCB and connected to the ground plane

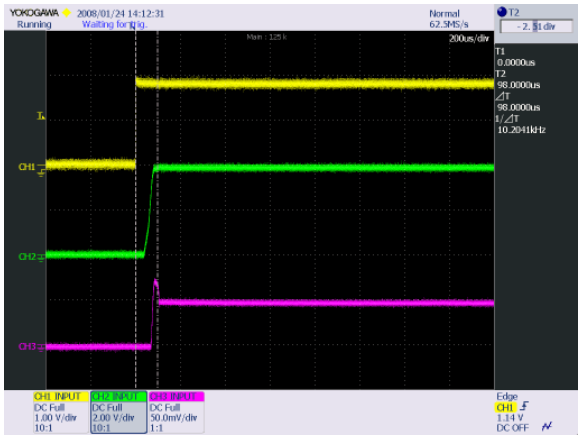
TYPICAL CHARACTERISTICS

Vin = 3.6V, I_{OUT} = 120mA (6 LEDs at 20mA), $C_1 = C_2 = 0.22\ \mu F$, $C_{IN} = C_{OUT} = 1\ \mu F$, T_{AMB} = 25°C unless otherwise specified

Efficiency vs. Input Voltage

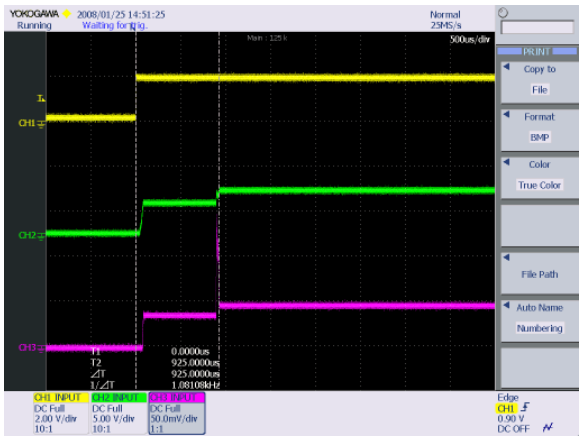


Power-Up in 1x mode



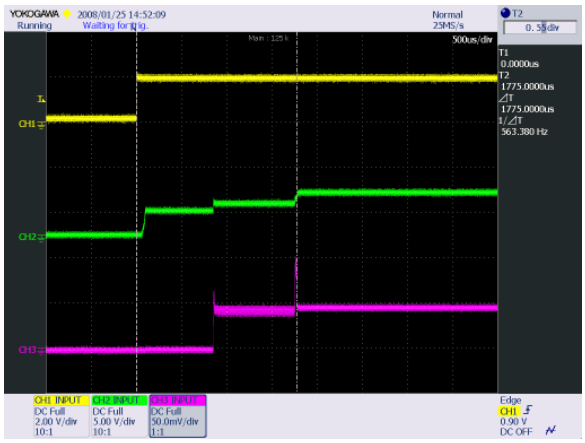
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Up in 1.5x Mode



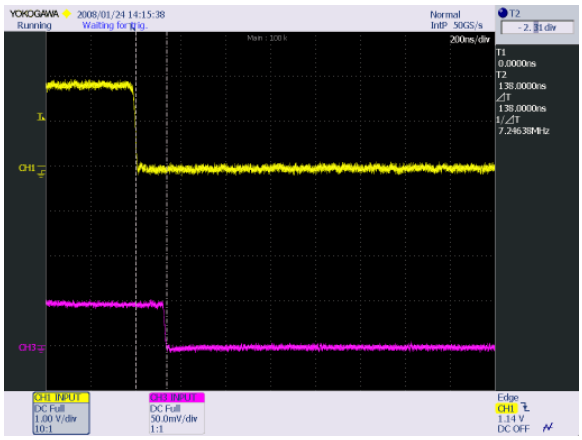
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Up in 2x Mode



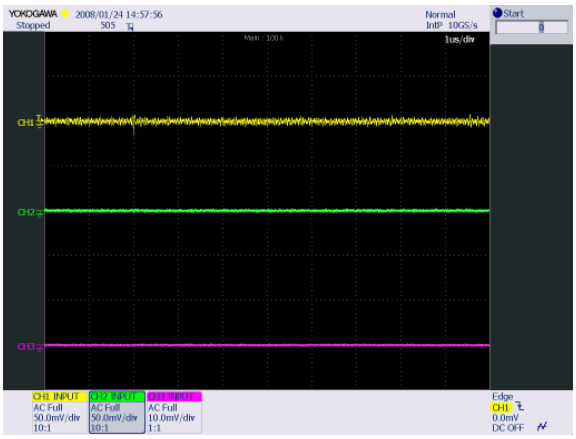
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Down Delay (1x Mode)



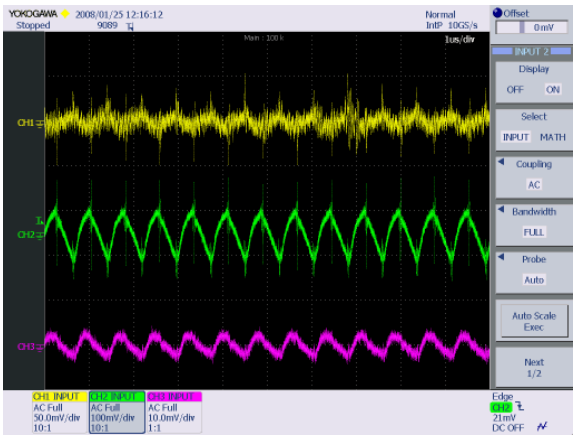
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Operating Waveforms in 1x Mode)



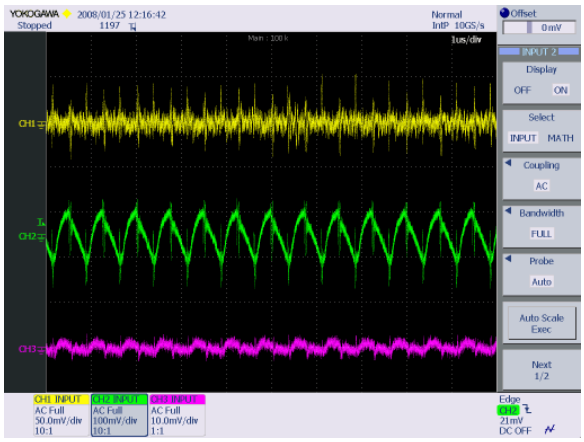
Ch1 – Vin (AC coupled), Ch2 – Vout (AC coupled),
Ch3 – Output current (AC coupled 20mA/div)

Switching Waveforms in 1.5x Mode



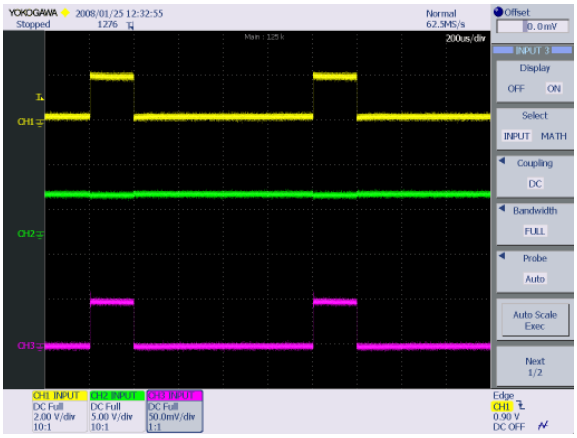
Ch1 – Vin (AC coupled), Ch2 – Vout (AC coupled),
Ch3 – Output current (AC coupled 20mA/div)

Switching Waveforms in 2x Mode



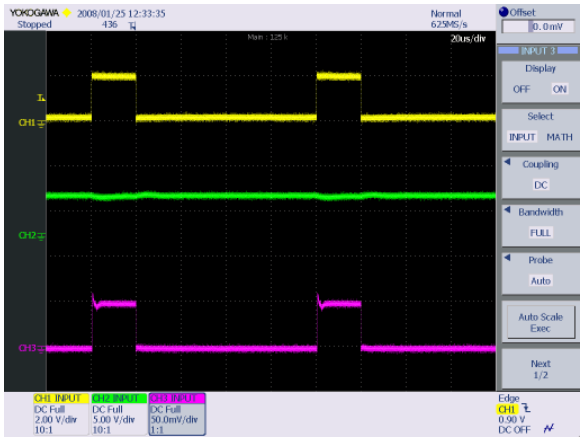
Ch1 – Vin (AC coupled), Ch2 – Vout (AC coupled),
Ch3 – Output current (AC coupled 20mA/div)

Switching Waveforms at 1kHz PWM mode



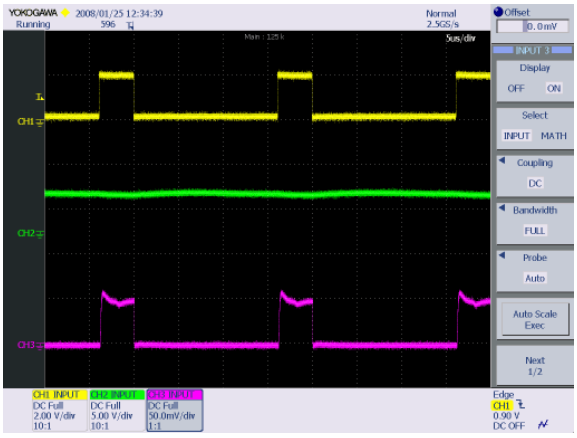
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Switching Waveforms at 10kHz PWM mode



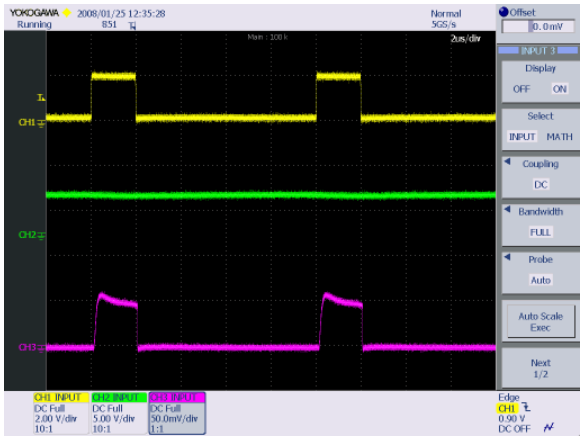
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Switching Waveforms at 50kHz PWM mode



Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Switching Waveforms at 100kHz PWM mode



Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

BLOCK DIAGRAM

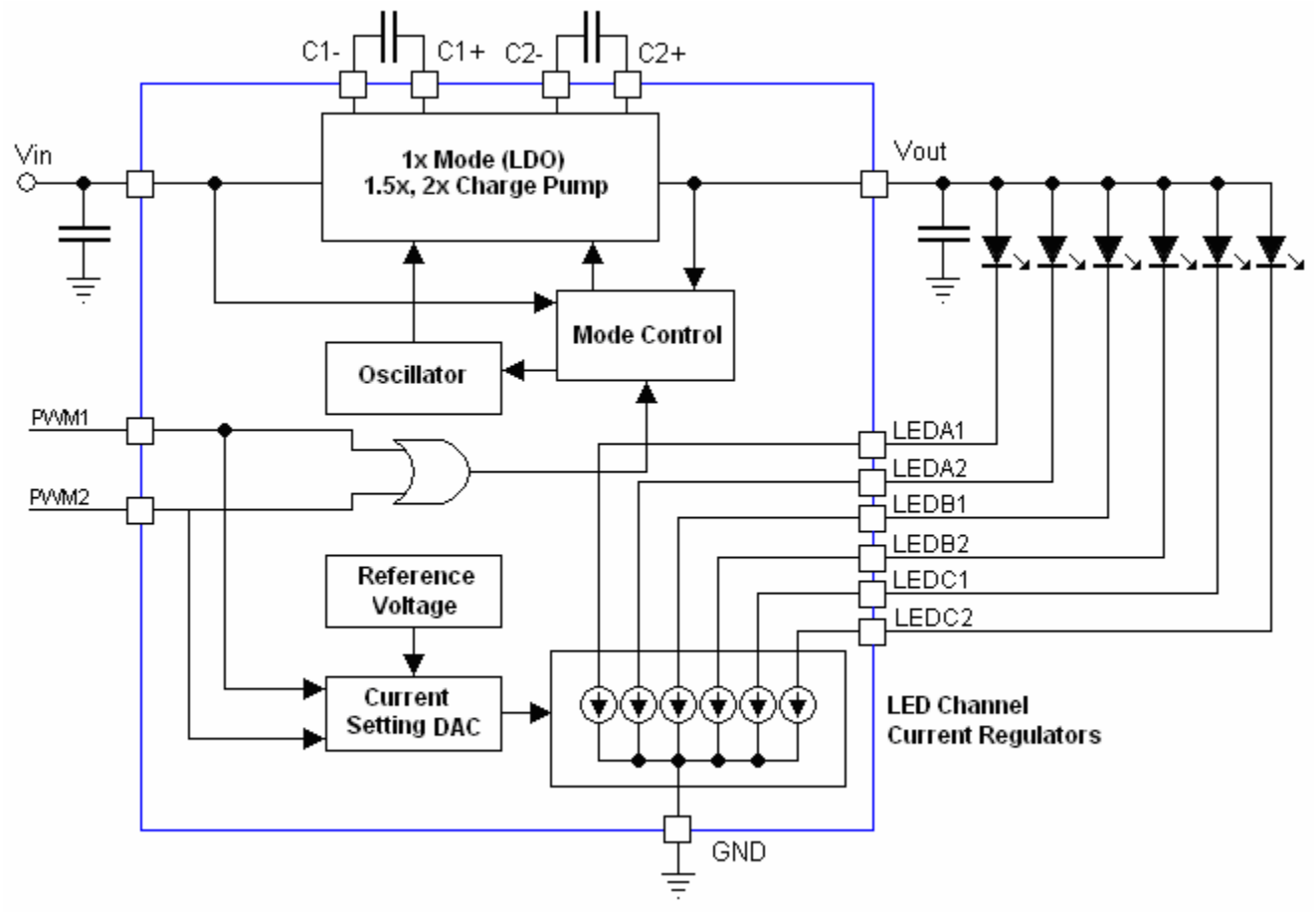


Figure 2. LDS8865 Functional Block Diagram

BASIC OPERATION

At power-up, PWM1 and PWM2 pins should be logic LOW. During power-up device performs internal circuits reset that requires less than 10µs. To start device either PWM1 or PWM2 pin should be set logic HIGH 10µs after than input voltage applied. Device starts operating at 1x mode at which the output is approximately equal to the input supply voltage (less any internal voltage losses). If the output voltage is sufficient to regulate all LED currents, the device remains in 1x operating mode.

The low dropout PowerLite™ Current regulator (PCR) performs well at input voltages Vin up to 75mV above LED forward voltage V_F significantly increasing driver's efficiency. The LDS8865 monitors voltage drop Vd across PCR at every channel in ON state. If this voltage falls below 75 mV (typical) at any one channel, (channel with LED with highest forward voltage), the Mode Control Block changes charge pump mode to the next multiplication ratio.

$Vd = V_{IN} \times M - V_F - Rcp \times Iout$, where Rcp is a Charge Pump Output Resistance at given mode, Iout is sum of all LED currents, and M is a charge pump' multiplication ratio.

If the input voltage is insufficient or falls to a level where Vd ≤ 75 mV, and the regulated currents cannot be maintained, the low dropout PowerLite™ Current Regulator switches the charge pump into 1.5x mode (after a fixed delay time of about 800 µs). In 1.5x mode, the charge pump' output voltage is approximately equal to 1.5 times the input supply voltage (less any internal voltage losses).

This sequence repeats until driver enters the 2x mode.

If the device detects a sufficient input voltage is present to drive all LED currents in 1x mode, it will change automatically back to 1x mode. This only applies for changing back to the 1x mode. The difference between the input voltage when exiting 1x mode and returning to 1x mode is called the 1x mode transition hysteresis (about 600 mV).

Operation of PWM-based LED Current Control

The maximum current value in each of the LDS8865's three LED banks is factory preset; to set each ILED below this value, a PWM (a duty cycle based) control signal can be applied at the PWM1/PWM2 pins.

Using a PWM control technique guarantees stable WLED color temperature over a wide range of LED currents. The LED color temperature set at the factory preset maximum LED current does not vary with respect to the average LED current unlike conventional 1-wire LED current control methods.

The LDS8865's PWM logic control circuits have been designed to operate from 100 Hz to 100 kHz with duty cycles higher than (0.02*F)% and lower than (100 – 0.02*F)%, where F is the PWM control frequency in kHz. The brightness dynamic dimming range at 200 Hz is 25,000 : 1. PWM control frequencies lower than 100 Hz are not recommended (especially with short duty cycles) because LED flicker may become visible.

When PWM current control is enabled, the LED current is modulated from zero to 100% over a single PWM period. For example, when PWM1/PWM2 is logic high, the LED current is set equal to the maximum factory preset value. When PWM1/PWM2 is logic low, the LED current is zero. The average LED current level is then determined by the PWM duty cycle that may be adjusted as described above.

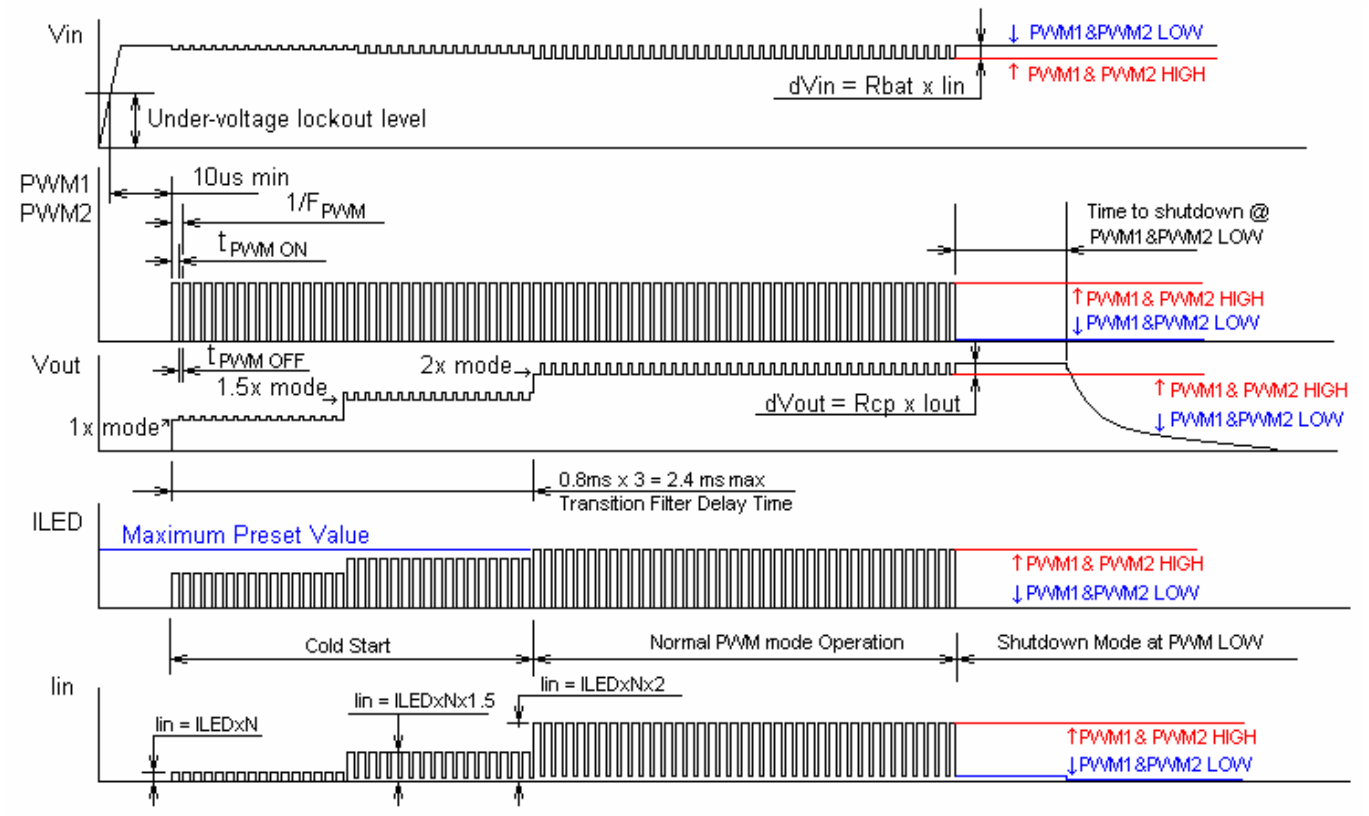


Figure 3 LDS8865 Timing Diagram

Note:
1. Timing diagram represents condition when LED forward voltage Vf is higher than Charge Pump Mode times(1.5) input voltage minus voltage drop on current regulator VPCR and minus voltage drop on charge pump output resistance Rcp at Iled current through N LEDs.
Vf > CPM X Vin – Vd – Rcp x Iled x N; PWM duty Cycle = $T_{PWM\ ON}$ / ($T_{PWM\ ON}$ + $T_{PWM\ OFF}$)
2. Timing Diagram is not to scale

When LED current control is enabled at the PWM1/PWM2 inputs, the LDS8865's maximum input current is determined by the factory preset maximum LED current multiplied by number of LED used, the charge pump operating mode (1x, 1.5x, or 2x), and divided by charge-pump driver's efficiency. For example, if six LEDs are used and the charge pump is operating in 2x mode, the maximum pulse current at V_{IN} would then be 400 mA (= 30 mA/LED x 6LEDs x 2/0.9), assuming that charge pump's efficiency alone at 2x mode is 90% and maximum factory preset current is 30 mA per LED.

When PWM LED current control is first enabled (at cold start, for example), the LDS8865's V_{IN}, V_{OUT}, and V_{PCR} monitors cause the LDS8865's charge pump to cycle through all operating modes (if necessary) so that V_{OUT} is high enough to maintain regulated LED current. To prevent nuisance switching of the charge pump during this initial start-up sequence, a 0.8ms transition filter is applied at each charge-pump mode. Depending on V_{IN} and the V_F of the LEDs chosen, the maximum cold-start delay to regulated LED current operation can be up to 1.6 ms. (See Timing Diagram Figure 3)

Once the LDS8865 reaches steady-state operation, its charge pump remains in operation even when the LED current is turned off (t_{OFF}). As shown in Figure 3, V_{OUT} increases slightly by an amount proportional to the voltage drop generated by charge pump's R_{OUT} and the total LED current load. The LDS8865's efficiency and LED current regulation are not affected because the LEDs are off during this time.

If the PWM1/PWM2 pins are held high or low longer than 30ms (Time to Shutdown), the LDS8865 turns LEDs off. If PWM1/PWM2 pins are low, shutdown mode is enabled and the supply current drops to 1 µA or less. If PWM1/PWM2 pins are logic high, the LDS8865 charge pump remains active with an overall quiescent current ~ 1 mA.

Unused LED Channels

For applications with only four or two LEDs, unused LED banks can be disabled via the appropriate PWM pin connected to the ground.

For applications requiring 1, 3, or 5 channels, the unused LED pins should be tied to Vout (see Figure 4). If LED pin voltage is within 1V of V_{OUT}, then the channel is switched off and a 250µA test current is placed in the channel to sense when the channel moves below V_{OUT} – 1.5 V.

Protection Mode

The LDS8865has follow protection modes:

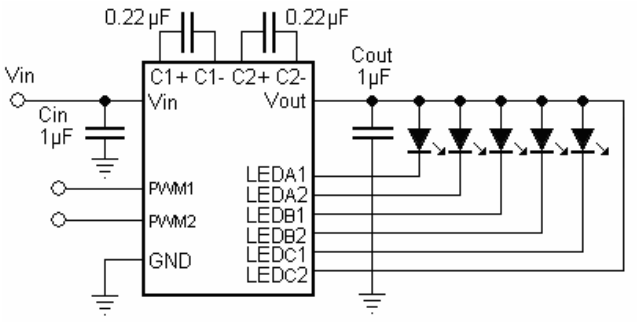


Figure 4. Application circuit with 5 LEDs

1. LED short to V_{OUT} protection

If LED pin is shorted to V_{OUT}, LED burned out becomes as short circuit, or LED pin voltage is within from V_{OUT} to (V_{OUT} - 1.5V) range, LDS8865 recognizes this condition as "LED Short" and disables this channel. If LED pin voltage is less than (Vout – 1.5V), LDS8865 restores LED current at this particular channel to programmed value.

2. V_{OUT} Over-Voltage Protection

The charge pump' output voltage V_{OUT} automatically limits at about 6.2 V maximum. This is to prevent the output pin from exceeding its absolute maximum rating.

3. V_{OUT} Short Circuit Protection

If V_{OUT} is shorted to ground before LDS8865 is enabled, input current may increase up to 200 – 300 mA within 20 µs after enable and is limited to 35 – 40 mA after that.

4. Over-Temperature Protection

If the die temperature exceeds +150°C, the driver will enter shutdown mode. The LDS8865 requires restart after die temperature falls below 130°C.

5. Input Voltage Under-Voltage Lockout

If V_{IN} falls below 2.2 V (typical value), LDS8865 enters shutdown mode Device restarts when input voltage rises above 2.3 V and PWM signal is applied.

6. Low V_{IN} or High LED V_F Voltage Detection

If, in 2x mode, V_{IN} is too low to maintain regulated LED current for given LED V_F, or LED becomes an open circuit, or if any LED at active channels is disconnected, LDS8865 starts subsequently changing modes (2x – 1x –1.5x – 2x -…) in an attempt to compensate insufficient voltage. As a result, average current at all other channels that are ON may fall below regulated level.

LED Selection

LEDs with forward voltages (V_F) ranging from 1.6 V to 3.6 V may be used. Charge pumps operate in highest efficiency when V_F voltage is close to V_{IN} voltage multiplied by switching mode, i.e. V_{IN} x 1, V_{IN} x 1.5, and so on. If the power source is a Li-ion battery, LEDs with VF = 2.7V - 3.3V are recommended to achieve highest efficiency performance and extended operation on a single battery charge.

External Components

The driver requires two external 1 µF ceramic capacitors (C_{IN} and C_{OUT}) and two 0.22 µF ceramic capacitors (C1 and C2) X5R or X7R type. Capacitors C1 and C2 may be increased up to 1 µF to improve charge pump efficiency by 3%. In all charge pump modes, the input current ripple is very low, and an input bypass capacitor of 1µF is sufficient.

In 1x mode, the device operates in linear mode and does not introduce switching noise back onto the supply.

Recommended Layout

In charge pump mode, the driver switches internally at a high frequency. It is recommended to minimize trace length to all four capacitors. A ground plane should cover the area under the driver IC as well as the bypass capacitors. Short connection to ground on capacitors C_{IN} and C_{OUT} can be implemented with the use of multiple via. A copper area matching the TQFN exposed pad (TAB) must be connected to the ground plane underneath. The use of multiple via improves the package heat dissipation.

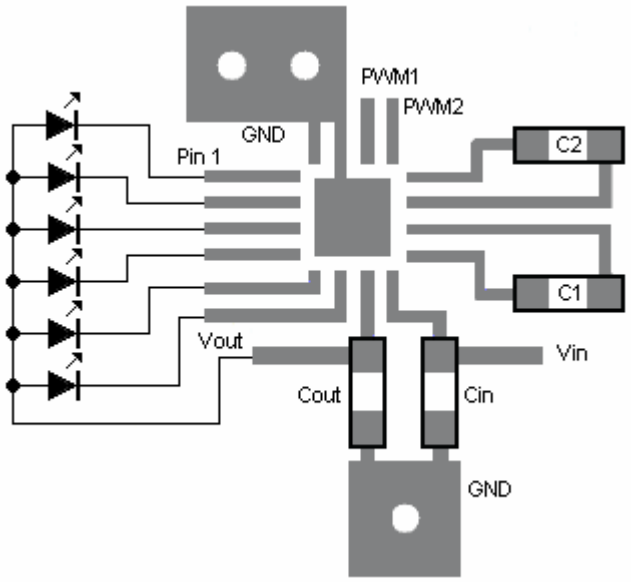
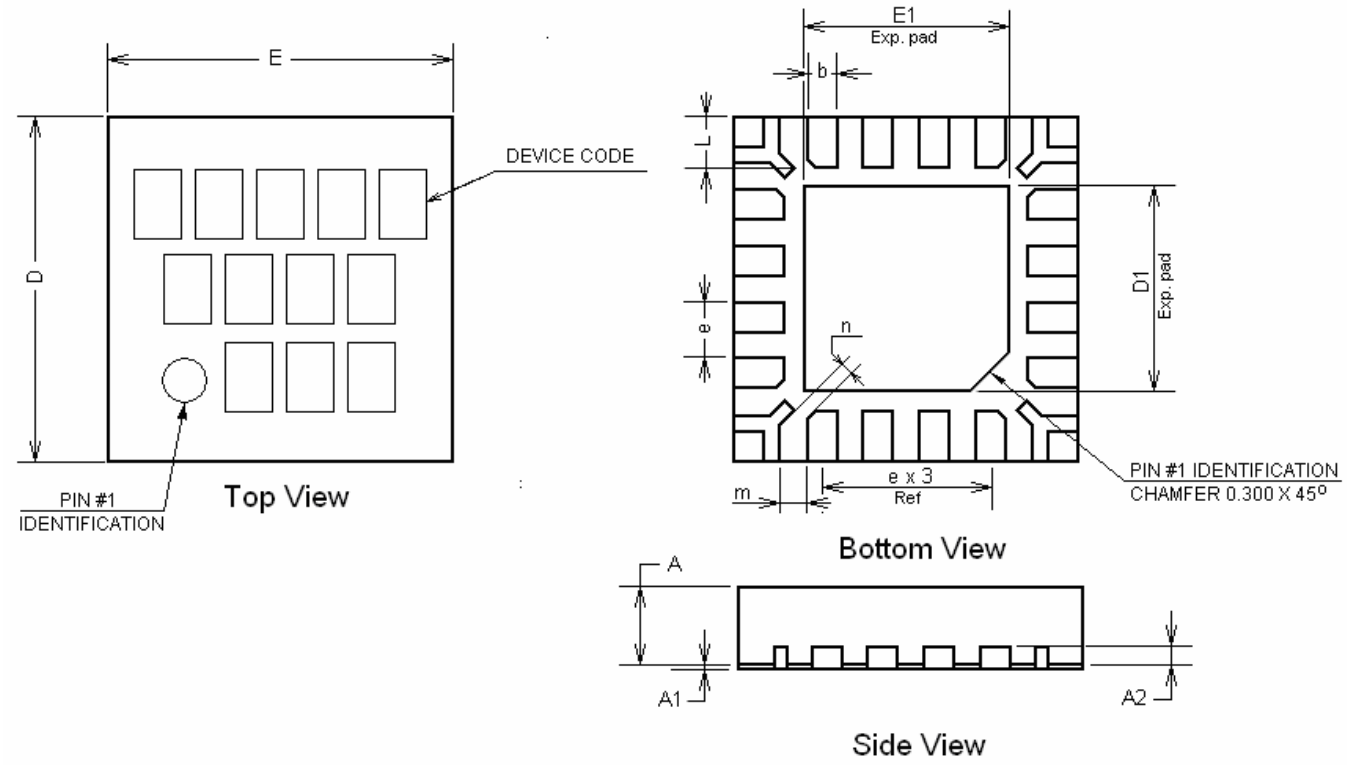


Figure 5. Recommended layout

PACKAGE DRAWING AND DIMENSIONS

16-PIN TQFN (HV3), 3mm x 3mm, 0.5mm PITCH



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.178	0.203	0.228
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D1	1.65	1.70	1.75
E	2.95	3.00	3.05
E1	1.65	1.70	1.75
e		0.50 typ	
L	0.325	0.375	0.425
m		0.150 typ	
n		0.225 typ	

Note:

1. All dimensions are in millimeters
2. Complies with JEDEC Standard MO-220

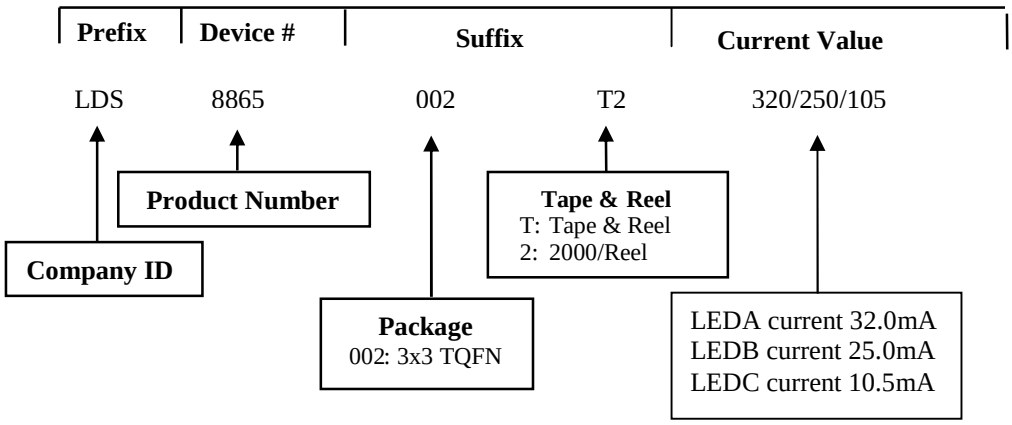
ORDERING INFORMATION

Part Number	Package	Package Marking
LDS8865 002 -T2 XXX/YYY/ZZZ	TQFN-16 3 x 3mm	8865

Notes:

1. XXX – LEDA bank maximum current value
2. YYY – LEDB bank maximum current value
3. ZZZ – LEDC bank maximum current value
4. Current value is in the range from 0.5mA to 32.0mA in 0.5mA steps and it should be shown as XXX = 320 =32.0mA, XXX = 255 = 25.5mA, XXX=050 = 5.0mA
5. Matte-Tin Plated Finish (RoHS-compliant)
6. Quantity per reel is 2000

EXAMPLE OF ORDERING INFORMATION



Notes:

1) All packages are RoHS-compliant (Lead-free, Halogen-free).
2) The standard lead finish is Matte-Tin.
3) The device used in the above example is a LDS8865 002–T2 (3x3 TQFN, Tape & Reel, 32/25/10.5 mA maximum current per LED bank
4) For additional package and temperature options, please contact your nearest IXYS Corp. Sales office.

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