A701/2

6 CHANNELS ADJUSTABLE CONSTANT CURRENT LED DRIVER

ADDtek
www.addmtek.com

DESCRIPTION

A701/2 are adjustable constant current drivers for LED applications. Six regulated current ports are designed to provide uniform and pure DC constant current sinks for driving LEDs within a large range VF variation.

A701/2 provide users 6-channel constant current ports to match LEDs with equal current. Users may program the output current from 5mA to 40mA through an external resistor, R_{SET}, which gives user flexibility in controlling the light intensity of LEDs.

Two kinds of control logic, active high and active low, for Output Enable pin ($\overline{OE}$/OE pin) are provided for user's varies applications. It could precisely adjust LED brightness from 0% to 100% via OE/$\overline{OE}$ pin with Pulse Width Modulation signal.

The thermal protection function protects IC from over temperature (150°C) damage. Also, the thermal pad enhances the package power dissipation.

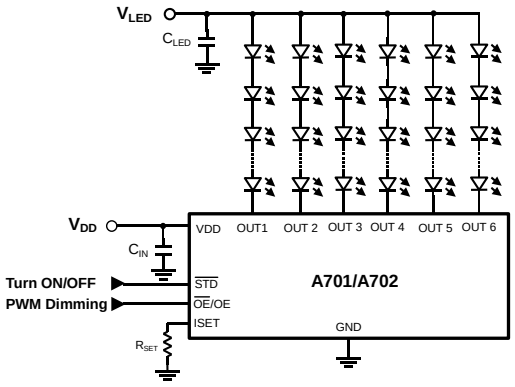
FEATURES

- **6 constant-current output channels**
- **Output current deviations: ±3% between channels, ±7% between ICs.**
- **Output current programmable through external resistor.**
- **Constant output current range: 5mA~40mA**
- **Wide supply voltage range: 6V~50V (A702)**
- **75V output sustaining voltage**
- **2 kinds of control logic for Output Enable pin**

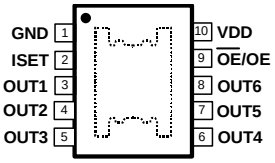
APPLICATIONS

- **Automotive Interior Lighting**
- **Channel Letter, Indoor Lighting**
- **LED Backlight Driver for MP3, MP4, Mobile Phone, Portable DVD, NB, and LCD TV.**

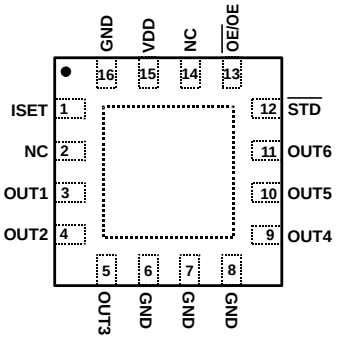
TYPICAL APPLICATION CIRCUIT



PACKAGE PIN OUT



MSOP-EP-10 Pin
(Top View)



QFN 3mm x 3mm
(Top View)

ORDER INFORMATION

V_{DD} Range	$\overline{OE}$/OE Pin Logic	G	MSOP-EP 10 pin		J	QFN 3x3 16 pin
2.9V~ 6V	Low Enable	A701GFT		A701GGT		A701JGT
6V~ 50V	High Enable	A702GFT-HE		A702GGT-HE		A702JGT-HE
	Low Enable	A702GFT		A702GGT		A702JGT

Note: **Part Number**: A 7 0 1 □ □ □
A 7 0 2 □ □ □ – HE

Package Type. G: MSOP-EP; J: QFN-3x3
Package Process. F: Lead Free; G: Green
EN Pin Logic. HE: High Enable
Packing. T: Tape & Reel

PIN DESCRIPTION

Pin Name	Pin Descriptions
GND	Ground terminal for control logic and current sink.
OUT1~OUT6	Constant current output terminals
$\overline{OE}$	Output Enable terminal, "Low" active. "Low level voltage" enables all the six output pins while "high level voltage" disables all the six output pins (blanked). It can be left floating for normally on.
OE	Output Enable terminal, "High" active. "High level voltage" enables all the six output pins while "low level voltage" disables all the six output pins (blanked). It can be left floating for normally on.
ISET	Output current setting input. Connect a resistor (R_{SET}) between ISET pin and GND pin to setup the output current for all output channels following: $I_{OUTn} = (1.2V / R_{SET}) \times 60$ **Don't leave this pin open as shutdown control**.
$\overline{STD}$	Chip shutdown pin, Low active. The supply current less than 1uA when shutdown. Internal pull-high.
V_{DD}	6V/50V supply voltage terminal

Note: The thermal pad is suggested connect to GND on PCB. And thermal conductivity will be improved, if a copper foil on PCB is soldered with thermal pad.

THERMAL RESISTANCE

Package		Thermal Resistance (°C /W)	
		θ_{JA}	θ_{JT}
G	MSOP-EP	107	9.63
J	QFN 3x3	51	29.62

Note:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A = P_D \times \theta_{JA} + T_A$$

Where, T_J: Junction Temperature.

T_A: Ambient Temperature.

P_D: Dissipated power.

θ_{JC}: Thermal Resistance – Junction to Case (Tab).

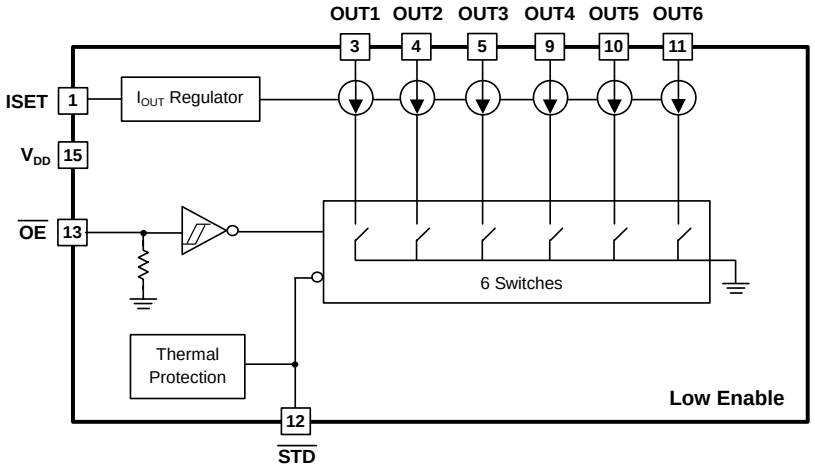
θ_{CS}: Thermal Resistance – Case (Tab) to Mounting Surface

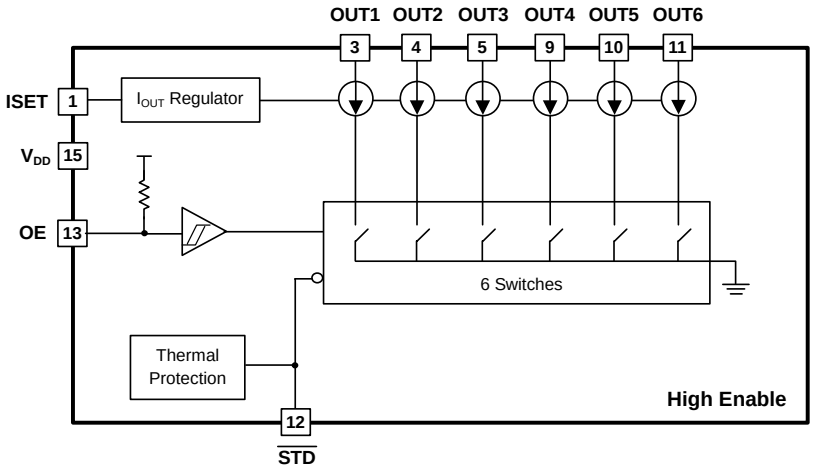
θ_{SA}: Thermal Resistance – Mounting Surface to Ambient (thermal resistance of the heat sink)

ABSOLUTE MAXIMUM RATINGS (Note)	
Supply Voltage, V_{DD}	50V
$\overline{OE}$/OE, $\overline{STD}$ Pin Input Voltage	12V
Output Current, I_{OUTn}	40mA
Sustaining Voltage (OUT1 ~ OUT6), V_{DS}	-0.4V to 75V
Maximum Operating Junction Temperature, T_J	125°C
Operating Temperature, T_{opr}	-40°C to 85°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground.
Currents are positive into, negative out of the specified terminal.

BLOCK DIAGRAM





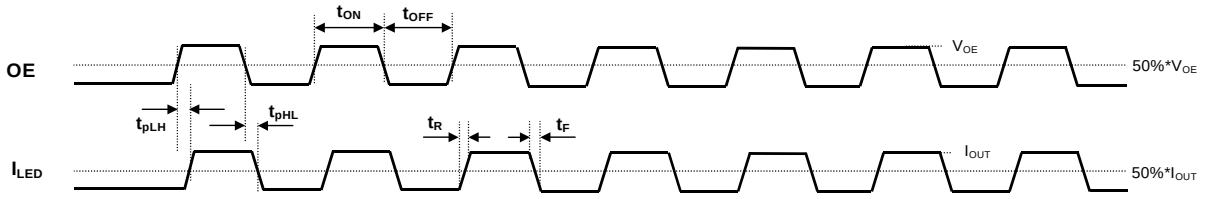
ELECTRICAL CHARACTERISTICS

V_{DD}=5V for A701 and V_{DD}=12V for A702, T_A=25°C. (Unless otherwise noted)

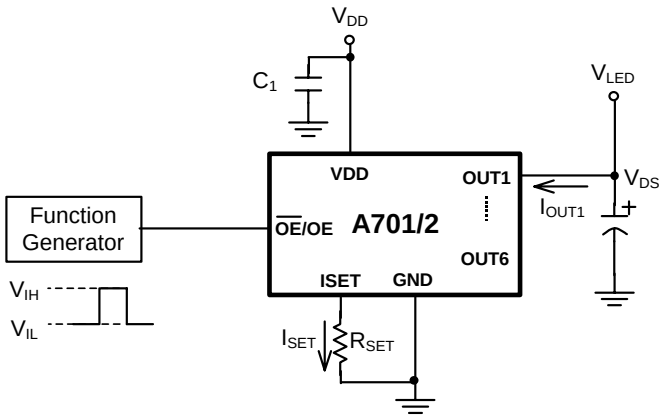
Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	A701	2.9	5	6	V
			A702	6	12	50	
Sustaining Voltage		V_{DS}	OUT1 ~ OUT 6			75	V
Output Current		I_{OUTn}	DC Test Circuit	5		40	mA
$\overline{OE}$/OE/$\overline{STD}$ Input Voltage	"H" level	V_{IH}	A701. Should not higher than V_{DD}.	2		6	V
			A702. Should not higher than V_{DD}.	2		12	
	"L" level	V_{IL}		GND		0.8	V
$\overline{OE}$/OE Input Hysteresis				200			mV
Output Leakage Current		I_{OH}	V_{OH}=40V			0.5	uA
Output Current (Between ICs)		I_{OUT}	V_{DS}=0.6V, R_{SET}=2.4 KΩ	27.9	30.0	32.1	mA
			V_{DS}=0.6V, R_{SET}=3.6 KΩ	18.6	20.0	21.4	
Output Current Skew (Between Channels)		$\triangle I_{OUTn}$	V_{DS}=0.6V, R_{SET}=2.4 KΩ		±1	±3	%
			V_{DS}=0.6V, R_{SET}=3.6 KΩ		±1	±3	
Regulation of Output Current vs. Sustaining Voltage		%/$\triangle V_{DS}$	V_{DS} =0.5V ~ 3.0V		±0.1	-	%/V
Regulation of Output Current vs. Supply Voltage		%/$\triangle V_{DD}$	A701, V_{DD} = 2.9V ~ 6V		±1	-	%
			A702, V_{DD} = 6V ~ 40V		±1		
Pull-up Resistor, $\overline{OE}$, $\overline{STD}$		R_{IN} (up)		0.5	1	1.5	MΩ
Thermal Protection Temperature		T_X	When T_J approaches T_X and OUT is shut off		160		°C
Thermal Protection Temperature Hysteresis					25		
Supply Current	"ON"	$I_{DD(ON)}$	R_{SET}=2.4KΩ; $\overline{OE}$/OE="Active"		4	7	mA
	"OFF"	$I_{DD(OFF)}$	R_{SET}=Open; $\overline{OE}$/OE="Inactive"		6	9	
			R_{SET}=2.4KΩ; $\overline{OE}$/OE="Inactive"		4	7	
	Shutdown	$I_{DD(SD)}$	A701, $\overline{STD}$ = "Low"		4	7	uA
			A702, $\overline{STD}$= "Low"		40	70	

TIMING CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Propagation Delay Time (Output Current from "L" to "H")	t_{pLH}	V_{DD}=5.0V(A701) V_{DD}=12.0V(A702) V_{DS}=1.0V V_{IH}=5.0V V_{IL}=GND R_{SET}=2.4 KΩ	0.1	0.3	0.6	us
Propagation Delay Time (Output Current from "H" to "L")	t_{pHL}		0.05	0.1	0.4	us
Shutdown Recover Delay Time				50		us
$\overline{OE}$/OE Minimum Pulse Width	$t_{W(OE)}$		5	-	-	us
Output Current Rising Time (Turn ON, rising from 10% to 90%)	t_{ON}		0.5	1	2	us
Output Current falling Time (Turn OFF, falling from 90% to 10%)	t_{OFF}		0.5	1	2	us



TEST CIRCUIT FOR SWITCHING CHARACTERISTICS



APPLICATION INFORMATION

The Maximum Power Dissipation on Regulator:

$$P_D = \sum_{n=1}^{6}(V_{OUTn} \cdot I_{OUTn}) + V_{DD(MAX)} \cdot I_{DD}$$

V_{OUTn} = the maximum voltage on output pin OUTn;
I_{OUTn} = the nominal output current through output pin OUTn;
$V_{DD(MAX)}$ = the maximum input voltage;
I_{DD} = the supply current to the regulator at I_{OUTn};
n = 1 ~ 6.

Thermal Consideration:

The A701/2 has internal power and thermal limiting circuitry designed to protect the device under overload conditions. However, maximum junction temperature ratings should not be exceeded under continuous normal load conditions. The thermal protection circuit of A701/2 prevents the device from damage due to excessive power dissipation. When the device temperature rises to approximately 150°C, the regulator will be turned off. When power consumption is over about 467mW (MSOP-10 package, at T_A=70°C) or 980mW (QFN 3x3 package, at T_A=70°C), additional heat sink is required to control the junction temperature below 120°C.

The junction temperature is:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

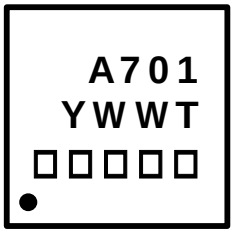
P_D : Dissipated power.
θ_{JC} : Thermal resistance from the junction to the mounting tab (case) of the package.
θ_{CS} : Thermal resistance through the interface between the IC and the surface on which it is mounted.
(typically, θ_{CS} < 1.0°C /W)
θ_{SA} : Thermal resistance from the mounting surface to ambient (thermal resistance of the heat sink).

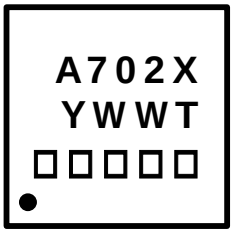
If PC Board copper is going to be used as a heat sink, below table can be used to determine the appropriate size of copper foil required. For multi-layered PCB, these layers can also be used as a heat sink. They can be connected with several through-hole vias.

PCB θ_{SA} (°C /W)	59	45	38	33	27	24	21
PCB heat sink size (mm^2)	500	1000	1500	2000	3000	4000	5000

PACKAGE

Top Marking for QFN 3mm x 3mm





X : OE Pin Control Logic

H – HE (High Enable)

N/A – LE (Low Enable)

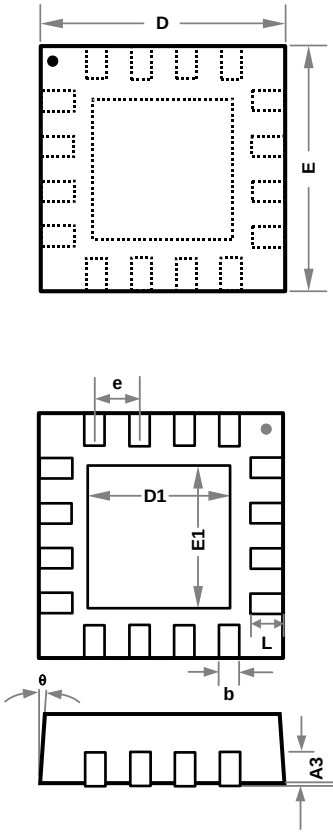
Y : Year Code

WW : Week Code

T : Trace Code

□□□□□ : Lot Number

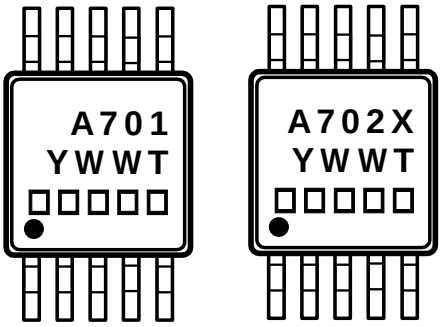
16-Pin QFN 3mmx3mm



SYMBOLS	MIN.	TYP.	MAX.
A	0.80	0.85	0.90
A1	0	0.010	0.030
A3	-	0.20REF.	-
b	0.18	0.23	0.28
D	2.95	3.00	3.03
D1	-	1.60BSC	-
E	2.95	3.00	3.03
E1	-	1.60BSC	-
e	-	0.50BSC	-
L	0.35	0.40	0.45
θ°	-12	-	0

UNIT: MILLIMETERS

Top Marking for MSOP-EP 10 Pin



X : OE Pin Control Logic

H – HE (High Enable)

N/A – LE (Low Enable)

Y : Year Code

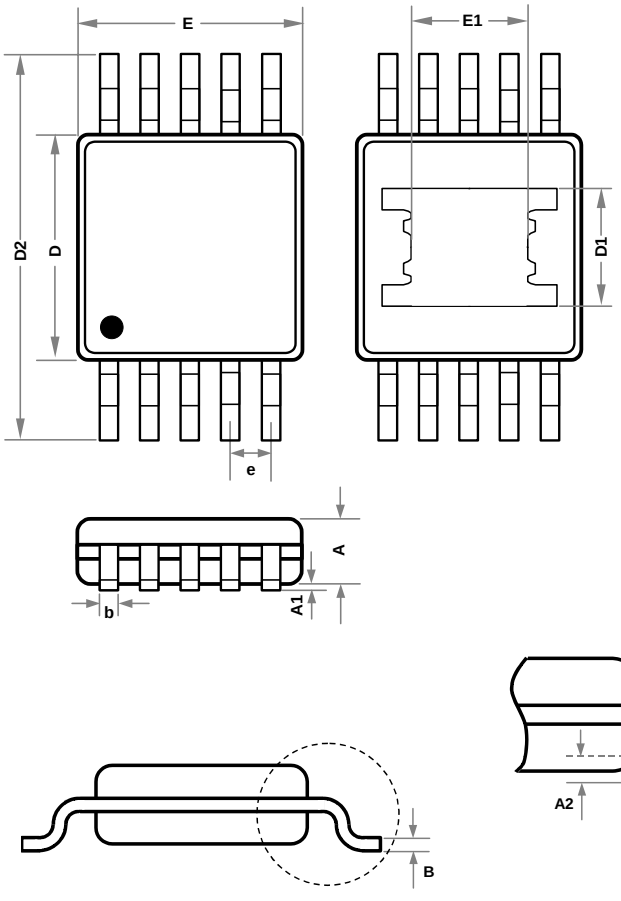
WW : Week Code

T : Trace Code

□□□□□ : Lot Number 《A701G**F**T/A702G**F**T-HE/A702G**F**T》

□□□□□ : Lot Number 《A701G**G**T/A702G**G**T-HE/A702G**G**T》

MSOP-EP 10 Pin



SYMBOLS	MIN.	TYP.	MAX.
A	0.81	0.86	0.91
A1	-	0.07	-
A2	-	0.25	-
B	0.10	0.15	0.20
b	0.17	-	0.27
D	2.90	3.00	3.10
D1	-	1.73	-
D2	4.68	4.88	5.08
E	2.90	3.00	3.10
E1	-	1.70	-
e	-	0.50	-
L	0.43	0.53	0.63
θ°	0	-	6

UNIT: MILLIMETERS

IMPORTANT NOTICE

ADDtek reserves the right to make changes to its products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage. ADDtek integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications. Use of ADDtek products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

ADDtek assumes to no liability to customer product design or application support. ADDtek warrants the performance of its products to the specifications applicable at the time of sale.

ADDtek Corp.
9F, No. 20, Sec. 3, Bade Rd., Taipei, Taiwan, 105
TEL: 2-25700299
FAX: 2-25700196