Low Voltage ORing FET Controller

ISL6146

The ISL6146 represents a family of ORing MOSFET controllers capable of ORing voltages from 1V to 18V. Together with suitably sized N-channel power MOSFETs, the ISL6146 increases power distribution efficiency when replacing a power ORing diode in high current applications. It provides gate drive voltage for the MOSFET(s) with a fully integrated charge pump.

The ISL6146 allows users to adjust with external resistor(s) the V_{OUT} - V_{IN} trip point, which adjusts the control sensitivity to system power supply noise. An open drain FAULT pin will indicate if a conditional or FET fault has occurred.

The ISL6146A and ISL6146B are optimized for very low voltage operation, down to 1V with an additional independent bias of 3V or greater.

The ISL6146C provides a voltage compliant mode of operation down to 3V with programmable Undervoltage Lock Out and Overvoltage Protection threshold levels.

TABLE 1. KEY DIFFERENCES BETWEEN PARTS IN FAMILY

PART NUMBER	KEY DIFFERENCES
ISL6146A	Separate BIAS and VIN with Active High Enable
ISL6146B	Separate BIAS and VIN with Active Low Enable
ISL6146C	VIN with OVP/UVLO Inputs

Features

- ORing Down to 1V and Up to 20V with ISL6146A, ISL6146B
- Programmable Voltage Compliant Operation with ISL6146C
- VIN Hot Swap Transient Protection Rating to +24V
- High Speed Comparator Provides Fast <0.3µs Turn-off in Response to Shorts on Sourcing Supply.
- Fastest Reverse Current Fault Isolation with 6A Turn-off Current
- Very Smooth Switching Transition
- Internal Charge Pump to Drive N-channel MOSFET
- User Programmable V_{IN} - V_{OUT} Vth for Noise Immunity
- Open Drain $\overline{FAULT}$ Output with Delay
  - Short between any two of the ORing FET Terminals
  - GATE Voltage and Excessive FET V_{DS}
  - Power-Good Indicator (ISL6146C)
- MSOP and DFN Package Options

Applications

- N+1 Industrial and Telecom Power Distribution Systems
- Uninterruptable Power Supplies
- Low Voltage Processor and Memory
- Storage and Datacom Systems

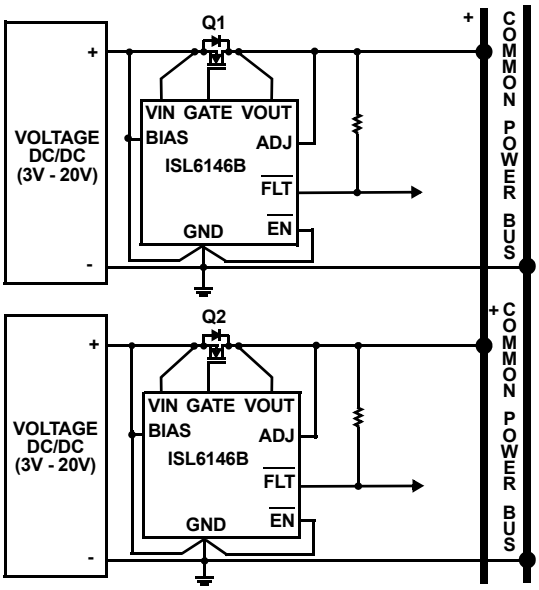


FIGURE 1. TYPICAL APPLICATION

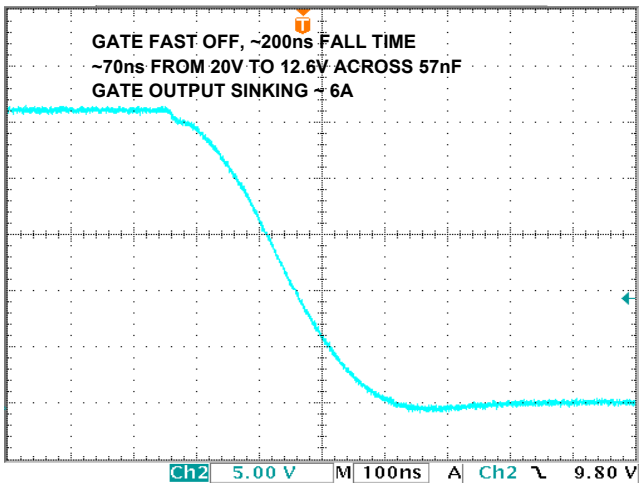
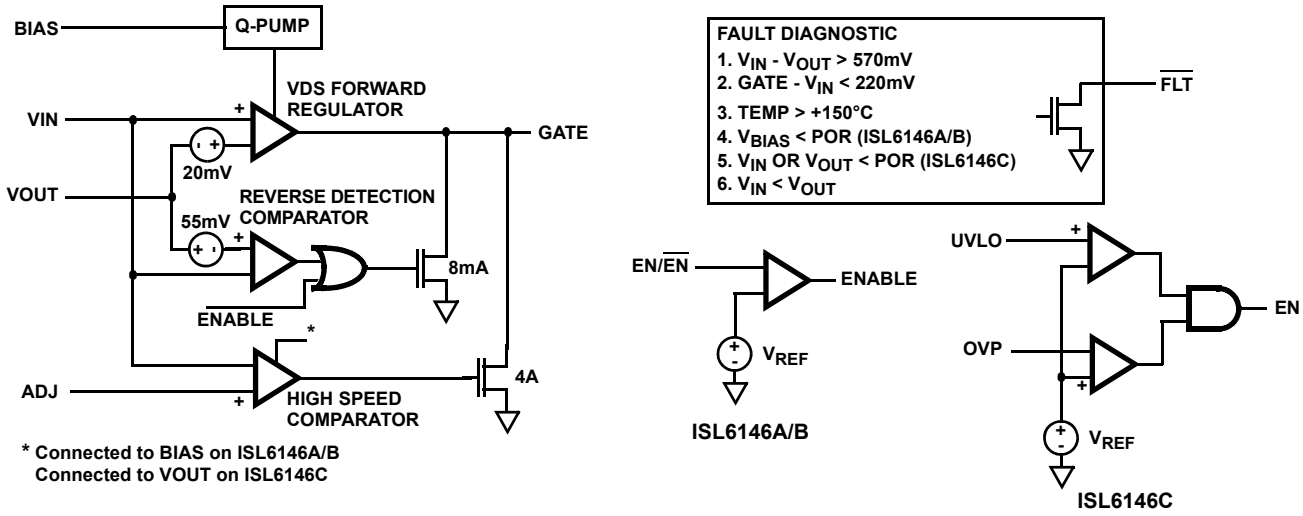


FIGURE 2. ISL6146 GATE HIGH CURRENT PULL-DOWN

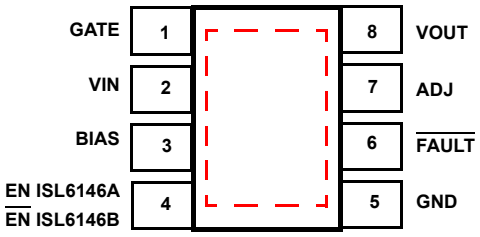
Block Diagram



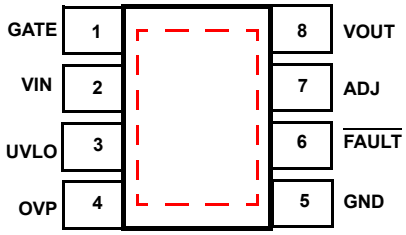
Pin Configuration

ISL6146
(8 LD MSOP/DFN)
TOP VIEW

ISL6146A, ISL6146B



ISL6146C



EPAD on DFN only, connect to GND

Pin Descriptions

MSOP/ DFN	SYMBOL	DESCRIPTION
1	GATE	Gate Drive output to the external N-Channel MOSFET generated by the IC internal charge pump. Gate turn-on time is typically <1ms. Allows active control of external N-Channel FET gate to perform ORing function. The GATE drive is between V_{IN} + 7V at V_{IN} = 3.3V and V_{IN} +12V at V_{IN} = 18V.
2	VIN	Connected to the sourcing supply side (ORing MOSFET Source), this pin serves as the sense pin to determine the OR'd supply voltage. The ORing MOSFET will be turned off when V_{IN} becomes lower than V_{OUT} by a value more than the externally set threshold or the defaulted internal threshold. Range: 0 to 24V
3 ISL6146A ISL6146B	BIAS	Primary bias pin. Connected to an independent voltage supply greater than or equal to 3V and greater than V_{IN}. Range: 3.0 to 24V
3 ISL6146C	UVLO	Programmable UVLO protection to prevent premature turn-on prior to VIN being adequately biased. Range: 0 to 24V
4 ISL6146A	EN	Active high enable input to turn on the FET. Internally pulled low to GND through 2MΩ Range: 0 to 24V
4 ISL6146B	$\overline{EN}$	Active low enable input to turn on the FET. Internally pulled high to BIAS through 2MΩ. Range: 0 to 24V

Pin Descriptions (Continued)

MSOP/ DFN	SYMBOL	DESCRIPTION
4 ISL6146C	OVP	Programmable OV protection to prevent continued operation when the monitored voltage is too high. A back-to-back FET configuration must be employed to implement the OVP capability. Range: 0 to 24V
5	GND	Chip ground reference.
6	$\overline{\text{FAULT}}$	Open-Drain pull-down fault indicating output with internal on chip filtering (T_{FLT}). The ISL6146 fault detection circuitry will pull-down this pin to GND as it detects a fault or to a disable input. Different types of faults and their detection mechanisms are discussed in more detail on page 16, these faults include: a. GATE is OFF (GATE < V_{IN}+0.2V) or b. V_{IN}-V_{OUT} > 0.57V when ON. c. FET G-D or G-S or D-S shorts. d. V_{IN} < POR_{L2H} e. V_{IN} < V_{OUT} f. Over-Temperature Range: 0 to V_{OUT}
7	ADJ	Resistor programmable V_{IN} - V_{OUT} Voltage Threshold (Vth) of the High Speed Comparator. This pin is either directly connected to VOUT or can be connected through a 5kΩ to 100kΩ resistor to GND. Allows for adjusting the voltage difference threshold to prevent unintended turn-off of the pass FET due to normal system voltage fluctuations. Range: 0.4 to V_{OUT}
8	VOUT	The second sensing node for external FET control and connected to the Load side (ORing MOSFET Drain). This is the common connection point for multiple paralleled supplies. V_{OUT} is compared to V_{IN} to determine when the ORing FET has to be turned off. Range: 0 to 24V
PAD	Thermal Pad	Connect to GND

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6146AFUZ (Note 4)	6146A	-40 to +125	8 Ld MSOP	M8.118
ISL6146AFRZ	46AF	-40 to +125	8 Ld 3x3 DFN	L8.3x3J
ISL6146BFUZ (Note 4)	6146B	-40 to +125	8 Ld MSOP	M8.118
ISL6146BFRZ	46BF	-40 to +125	8 Ld 3x3 DFN	L8.3x3J
ISL6146CFUZ (Note 4)	6146C	-40 to +125	8 Ld MSOP	M8.118
ISL6146CFRZ	46CF	-40 to +125	8 Ld 3x3 DFN	L8.3x3J
ISL6146AEVAL1Z	ISL6146A Evaluation Board			
ISL6146BEVAL1Z	ISL6146B Evaluation Board			
ISL6146CEVAL1Z	ISL6146B Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6146. For more information on MSL please see techbrief TB363.
4. MSOP packaged parts to be released soon.

Table of Contents

Absolute Maximum Ratings

BIAS, VIN, VOUT. . . . . -0.3V to +24V
GATE . . . . . -0.3V to 40V
EN, $\overline{EN}$, UVLO, OVP . . . . . -0.3V to +24V
ADJ . . . . . -0.3V to V_{OUT}
$\overline{FAULT}$ . . . . . -0.3V to V_{OUT}
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2.5kV
Machine Model (Tested per JESD22-A115-A). 250V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
MSOP Package (Notes 5, 8)	140	41
DFN Package (Notes 6, 7).	46	5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pb free/Pb-FreeReflow.asp

Recommended Operating Conditions

Bias Supply Voltage Range . . . . . +3V to +20V
OR'd Supply Voltage Range. . . . . +1V to BIAS
Temperature Range (T_A) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
8. For θ_{JC}, the "case temp" location is taken at the package top center

Electrical Specifications

V_{CC} = BIAS = 12V, unless otherwise stated. T_A = +25°C to +85°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
BIAS						
POR_{L2H}	POR Rising	BIAS Rising, GATE Rising	**1.9**	2.5	**2.95**	V
POR_{HYS}	POR Hysteresis			189		mV
IBIAS_en_18	ISL6146A/B BIAS Current	BIAS, V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, enabled		3.6	5	mA
IVIN_en_18	ISL6146A/B V_{IN} Current	BIAS, V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, enabled		25	40	µA
IVIN_en_18	ISL6146C V_{IN} Current	V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, enabled		3	4.5	mA
IVOUT_en_18	ISL6146A/B V_{OUT} Current	BIAS, V_{IN} = 18V, V_{OUT} = 16.98V, enabled		14	20	µA
VOUT_en_18	ISL6146C V_{OUT} Current	V_{IN} = 18V, V_{OUT} = 16.98V, enabled		400	500	µA
IBIAS_den_18	ISL6146A/B BIAS Current	BIAS, V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, disabled		1.7	3	mA
IVIN_den_18	ISL6146A/B V_{IN} Current	BIAS, V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, disabled		27	37	µA
IVIN_den_18	ISL6146C V_{IN} Current	V_{IN} = 18V, ADJ, V_{OUT} = 16.98V, disabled		1.3	1.5	mA
IVOUT_den_18	ISL6146A/B V_{OUT} Current	BIAS, V_{IN} = 18V, V_{OUT} = 16.98V, disabled		14	20	µA
IVOUT_den_18	ISL6146C V_{OUT} Current	V_{IN} = 18V, V_{OUT} = 16.98V, disabled		385	500	µA
$t_{BIAS2GTE}$	BIAS to GATE Delay	BIAS > POR_{L2H} to GATE Rising		150	210	µs
GATE						
V_{GH_3}	Charge Pump Voltage	V_{IN}, BIAS = 3V V_{IN} - V_{OUT} > V_{FWD_HR}	**V_{IN}+5V**	V_{IN} +7V	**V_{IN}+10.5V**	V
V_{GH_12}	Charge Pump Voltage	V_{IN}, BIAS = 12V V_{IN} - V_{OUT} > V_{FWD_HR}	**V_{IN}+9V**	V_{IN} +10V	**V_{IN}+17.5V**	V
V_{GH_18}	Charge Pump Voltage	V_{IN}, BIAS = 18V V_{IN} - V_{OUT} > V_{FWD_HR}	**V_{IN}+9V**	V_{IN} +10V	**V_{IN}+18V**	V
V_{GL}	Low Voltage Level	V_{IN} - V_{OUT} < 0V		0	**0.1**	V
I_{PDL}	Low Pull-Down Current	V_{IN} = 12V, V_{OUT} = 12.2V ADJ = 11V	**5**	8.4	**13**	mA
I_{PDH}	High Pull-Down Current	V_{IN} falling from 12V to 10V in 2µs	**3.5**	6.5		A

Electrical Specifications V_{CC} = BIAS = 12V, unless otherwise stated. T_A = +25°C to +85°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
t_{toff}	Fast Turn-off Time	V_{IN} = V_{BIAS} = 12V, V_{GATE} = 18V to 10V, C_{GATE} = 57nF		65	**130**	ns
t_{toffs}	Slow Turn-off Time	V_{IN} = V_{BIAS} = 12V, V_{GATE} = 18V to 10V, C_{GATE} = 57nF		58	**80**	µs
I_{ON}	Turn-On Current	BIAS = 12V, VG = 0V		1		mA
		BIAS = 12V, VG = 20V		0.15		mA
V_{VG_FLTr}	GATE to V_{IN} Rising Fault Voltage	GATE > V_{IN}, enabled, fault is asserted	**320**	440	**560**	mV
V_{VG_FLTf}	GATE to V_{IN} Falling Fault Voltage	GATE > V_{IN}, enabled, fault is asserted	**140**	220	**300**	mV
CONTROL AND REGULATION I/O						
V_{Rr}	Reverse Voltage Detection Rising V_{OUT} Threshold	V_{OUT} rising	**35**	57	**79**	mV
V_{Rf}	Reverse Voltage Detection Falling V_{OUT} Threshold	V_{OUT} falling	**10**	30	**51**	mV
t_{Rs}	Reverse Voltage Detection Response Time			10		µs
VFWD_VR	Amplifier Forward Voltage Regulation	ISL6146 controls voltage across FET V_{DS} to V_{FWD_VR} during static forward operation at loads resulting in Id*$r_{DS(ON)}$ < V_{FWD_VR}	**11**	19	**28**	mV
V_{OS_HS}	HS Comparator Input Offset Voltage		**-14**	0.7	**14**	mV
$V_{TH(HS5k)}$	ADJ Adjust Threshold with 5k to GND	R_{ADJ} = 5kΩ to GND	**0.57**	0.8	**1.1**	V
$V_{TH(HS100k)}$	ADJ Adjust Threshold with 100k to GND	R_{ADJ} = 100kΩ to GND	**10**	40	**95**	mV
t_{HSpd}	HS Comparator Response Time	V_{OUT} > V_{IN}, 1ns transition, 5V differential		170		ns
V_{FWD_FLT}	V_{IN} to V_{OUT} Forward Fault Voltage	V_{IN} > V_{OUT}, GATE is fully on, fault is asserted	330	450	570	mV
$V_{FWD\_FLT\_HYS}$	V_{IN} to V_{OUT} Forward Fault Voltage Hysteresis	V_{IN} > V_{OUT}, GATE is fully on, fault is deasserted		44		mV
FAULT OUTPUT						
I_{FLT_SINK}	$\overline{FAULT}$ Sink Current	BIAS = 18V $\overline{FAULT}$ = 0.5V, V_{IN} < V_{OUT}, V_{GATE} = V_{GL}	**5**	9		mA
I_{FLT_LEAK}	$\overline{FAULT}$ Leakage Current	$\overline{FAULT}$ = "V_{FLT_H}", V_{IN} > V_{OUT}, V_{GATE} = V_{IN} + V_{GQP}		0.04	**10**	µA
t_{FLT_L2H}	$\overline{FAULT}$ Low to High Delay	GATE = V_{GQP} to $\overline{FAULT}$ = HIGH		10	**23**	µs
t_{FLT_H2L}	$\overline{FAULT}$ High to Low Delay	GATE = V_{IN} to $\overline{FAULT}$ = LOW		1.7	**3**	µs
ENABLE UVLO/OVP/ADJ INPUTS						
VthRa	ISL6146A EN Rising Vth		**580**	606	**631**	mV
VthR_hysa	ISL6146A EN Vth Hysteresis			-90		mV
VthFb	ISL6146B $\overline{EN}$ Falling Vth		**580**	606	**631**	mV
VthF_hysb	ISL6146B $\overline{EN}$ Vth Hysteresis			+90		mV
VthFc	ISL6146C OVP Falling Vth		**580**	606	**631**	mV
VthF_hysc	ISL6146C OVP Vth Hysteresis			+90		mV
VthRc	ISL6146C UVLO Rising Vth		**580**	606	**631**	mV
VthR_hysc	ISL6146C UVLO Vth Hysteresis			-90		mV
$t_{EN2GTER}$	EN/UVLO Rising to GATE Rising Delay			10	**12**	µs
	$\overline{EN}$/OVP Falling to GATE Rising Delay			9	**12**	µs

Electrical Specifications V_{CC} = BIAS = 12V, unless otherwise stated. T_A = +25°C to +85°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
$t_{EN2GTEF}$	EN/UVLO Falling to GATE Falling Delay			2	4	µs
	$\overline{EN}$/OVP Rising to GATE Falling Delay			2	4	µs
Ren_h	ENABLE Pull-Down Resistor	ISL6146A		2		MΩ
Ren_l	$\overline{ENABLE}$ Pull-Up Resistor	ISL6146B		2		MΩ
Vadj	ADJ Pin Voltage	R_{ADJ} 5kΩ to 100kΩ		0.4		V
Radj	ADJ Pull-Up Resistor	Internal ADJ Pull-up Resistor to V_{OUT}		3.85		MΩ
OTS	Over-Temperature Sense	Fault signals in operation		140		°C
OTS_{HYS}	Over-Temperature Sense Hysteresis			20		°C
HTS	High Temperature Sense	Fault signals upon enabling		125		°C

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

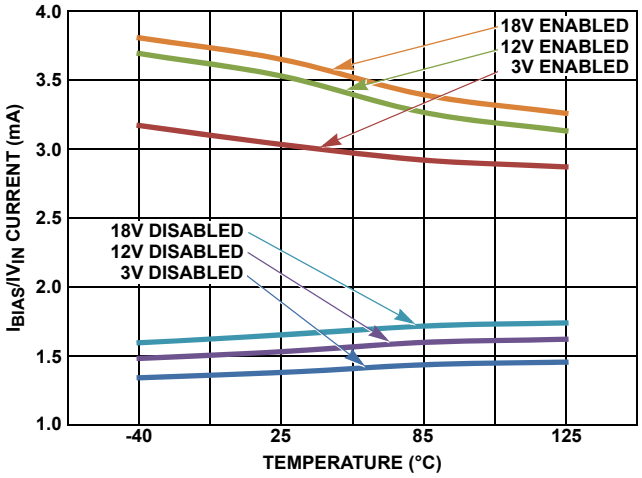


FIGURE 3. ISL6146A/B BIAS AND ISL6146C V_{IN} CURRENT vs TEMPERATURE

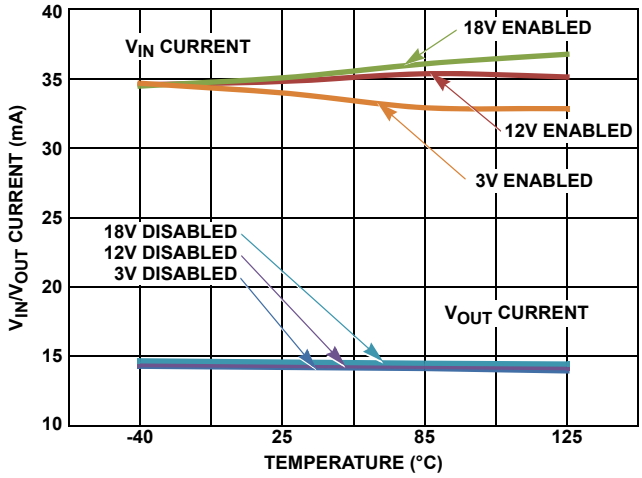


FIGURE 4. ISL6146A/B/C V_{IN} AND V_{OUT} CURRENT vs TEMPERATURE

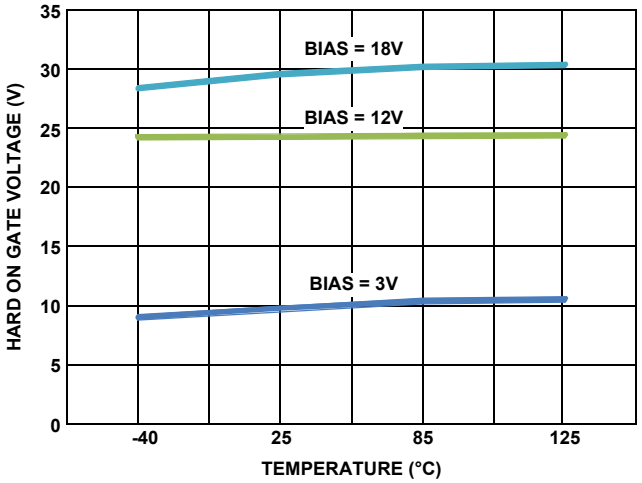


FIGURE 5. GATE VOLTAGE vs TEMPERATURE

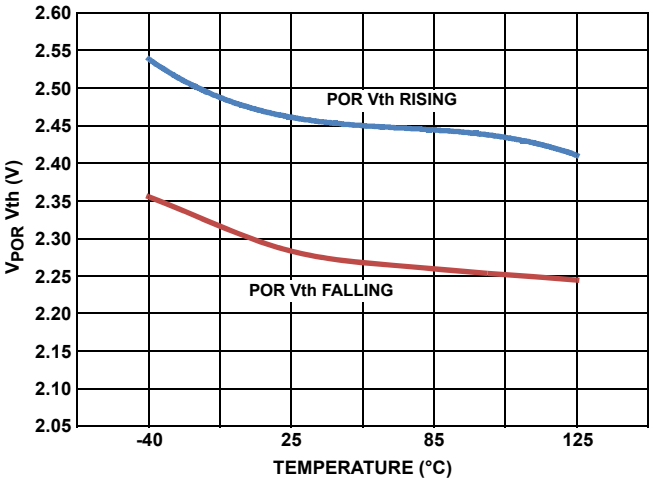


FIGURE 6. POR Vth RISING AND FALLING VOLTAGE

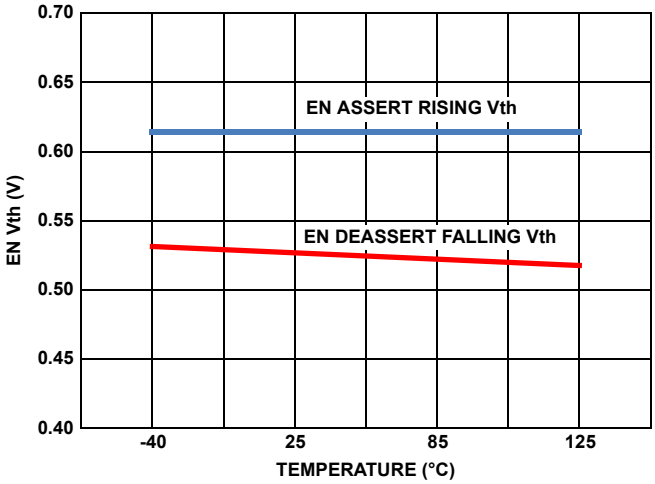


FIGURE 7. ISL6146A EN Vth vs TEMPERATURE

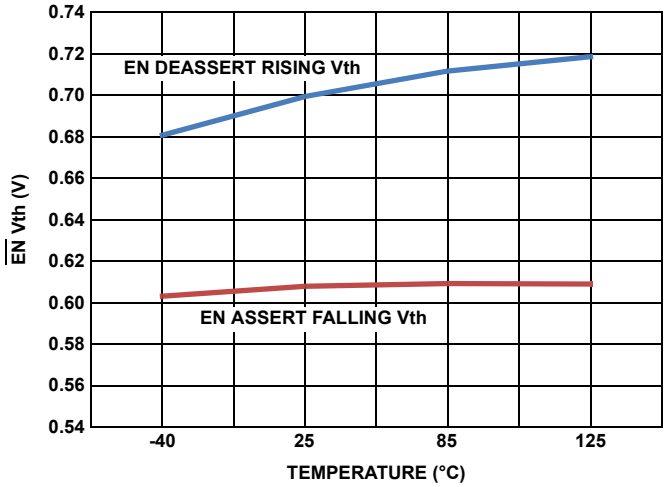


FIGURE 8. ISL6146B EN Vth vs TEMPERATURE

Typical Performance Curves (Continued)

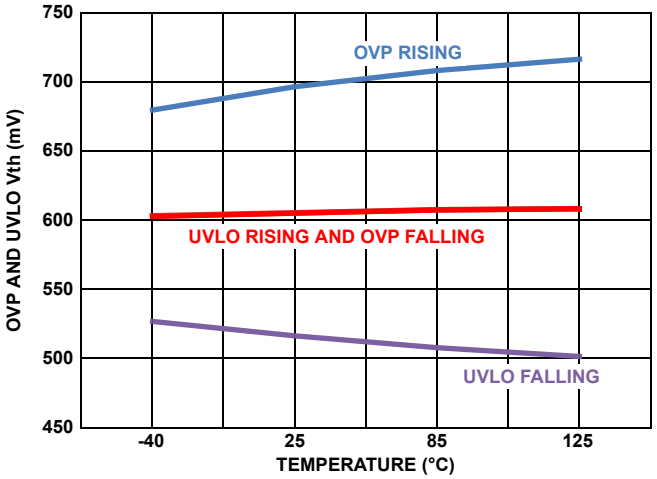


FIGURE 9. ISL6146C UVLO/OVP Vth vs TEMPERATURE

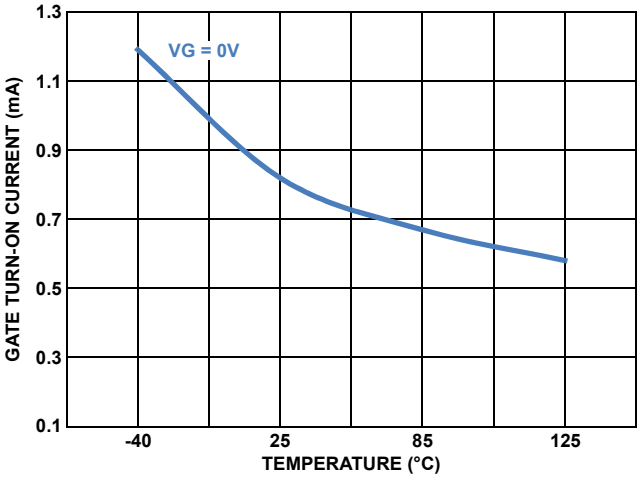


FIGURE 10. GATE TURN-ON CURRENT V_{IN} = 12V

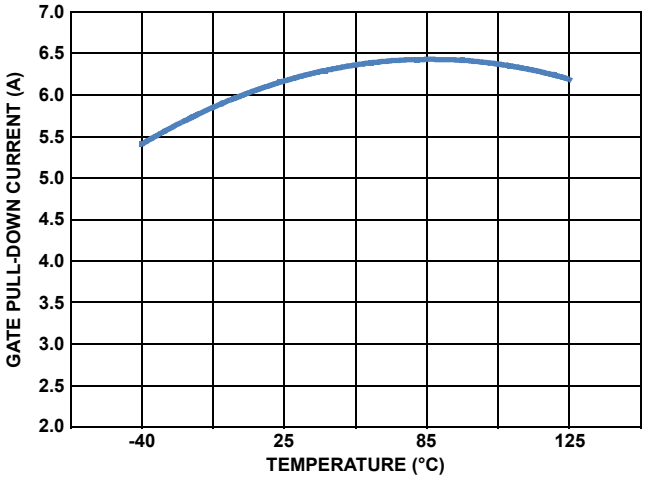


FIGURE 11. GATE HARD TURN-OFF CURRENT

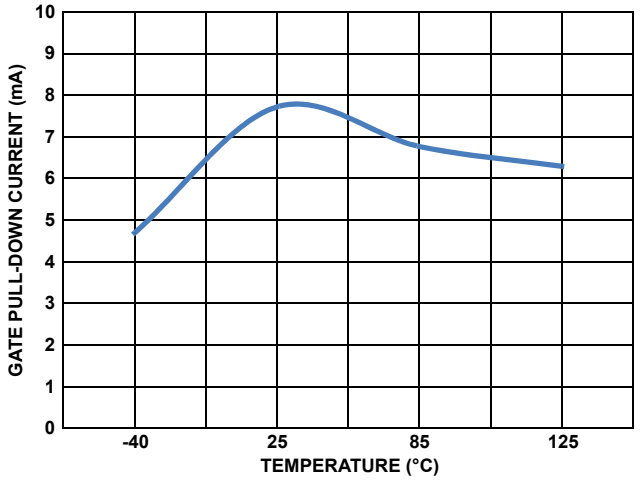


FIGURE 12. GATE SLOW TURN-OFF CURRENT

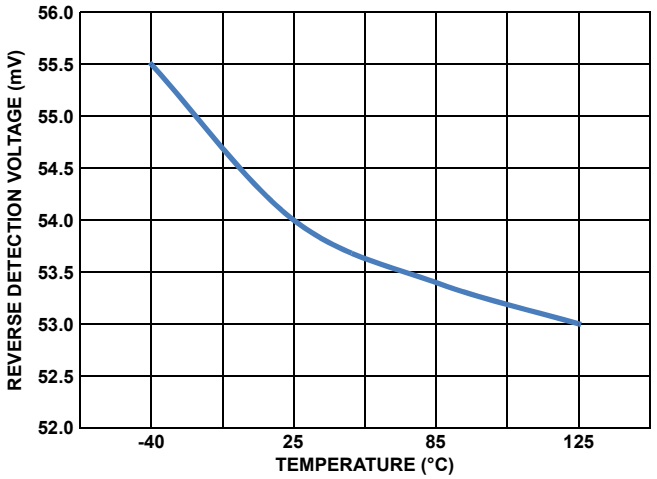


FIGURE 13. INCREASING REVERSE VOLTAGE DETECTION Vth

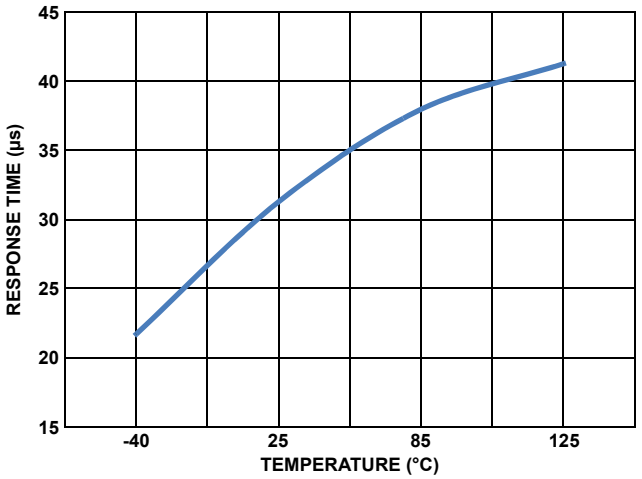


FIGURE 14. REVERSE VOLTAGE RESPONSE TIME

Typical Performance Curves (Continued)

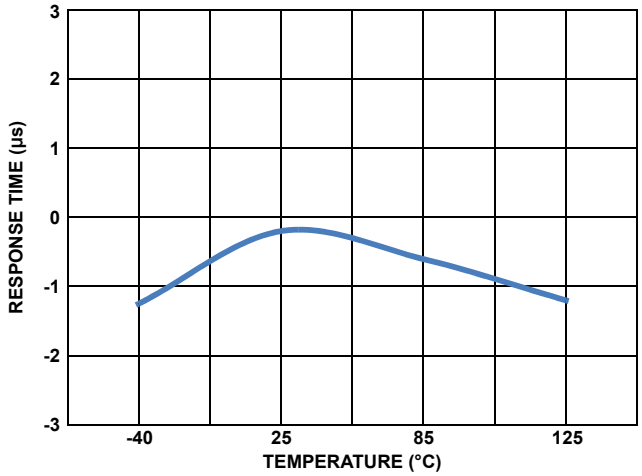


FIGURE 15. HIGH SPEED COMPARATOR OFFSET VOLTAGE

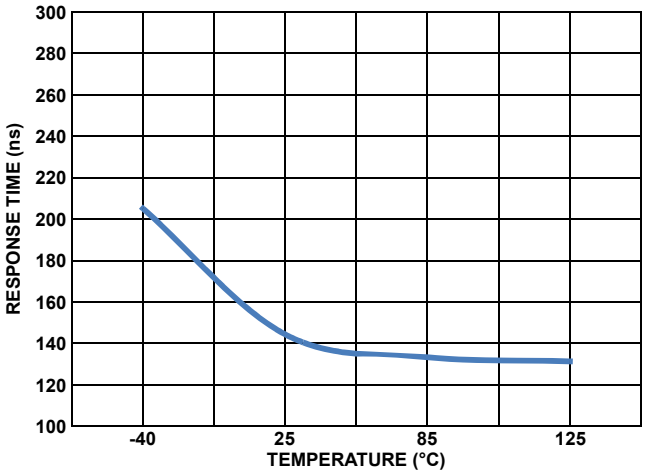


FIGURE 16. VHIGH SPEED COMPARATOR RESPONSE TIME

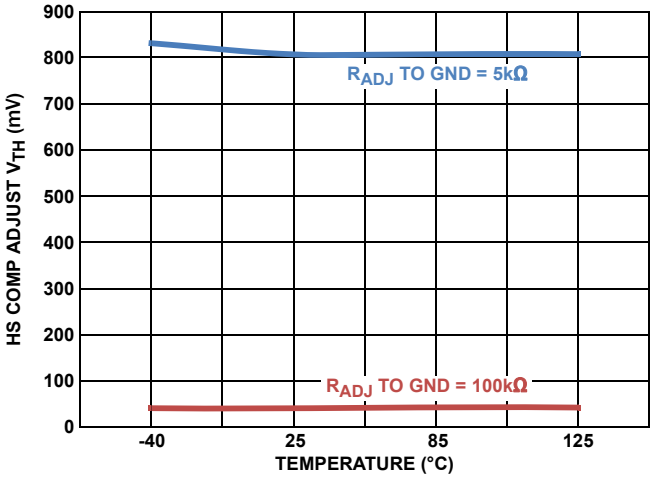


FIGURE 17. HS COMPARATOR ADJUSTABLE Vth

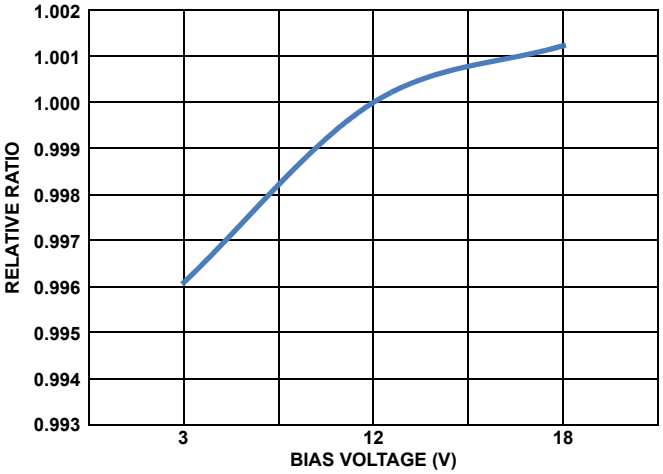


FIGURE 18. EN/EN/OVP/UVLO Vth DELTA vs BIAS VOLTAGE NORMALIZED TO BIAS = 12V

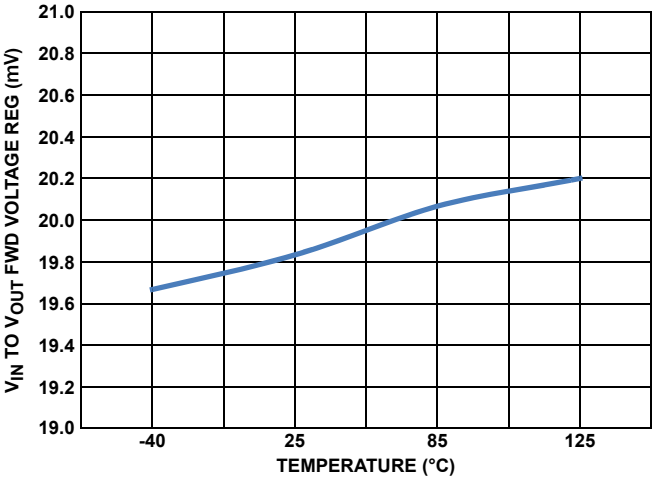


FIGURE 19. FORWARD VOLTAGE REGULATION

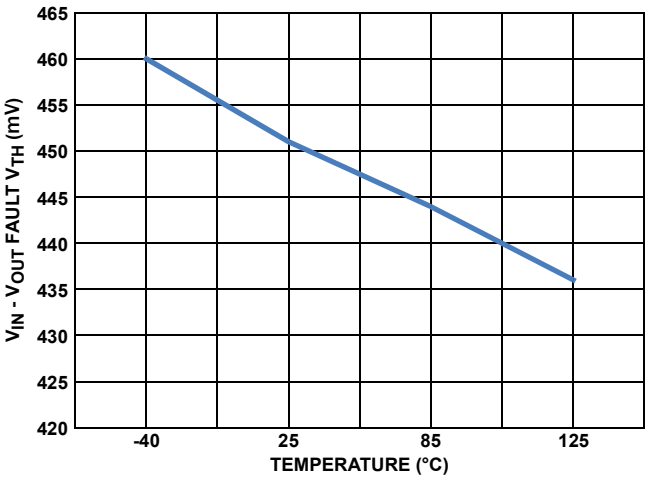


FIGURE 20. V_{IN} TO V_{OUT} FORWARD FAULT VOLTAGE

Typical Performance Curves (Continued)

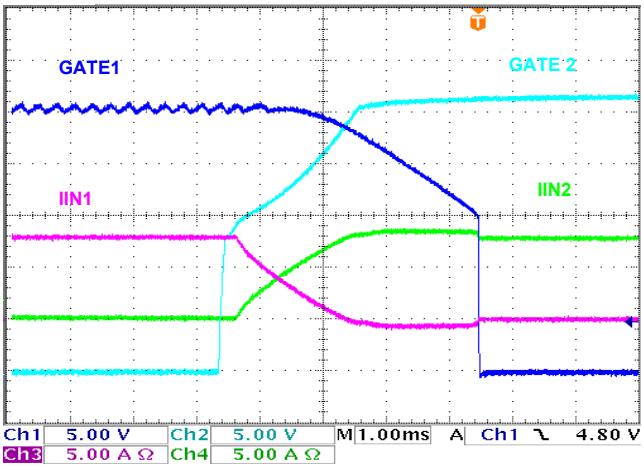


FIGURE 21. ISL6146C SLOW RAMP CONNECT 12V ORing

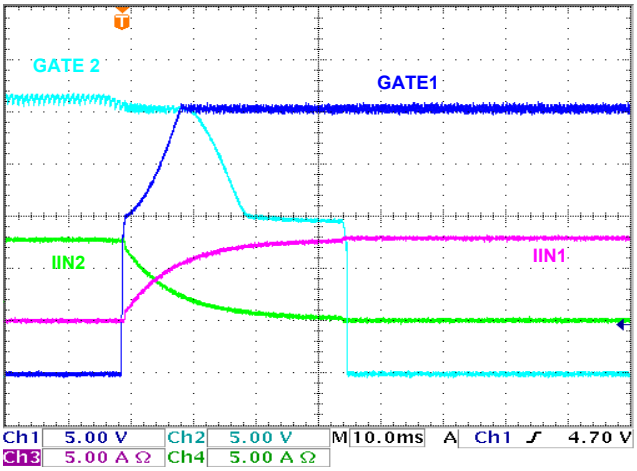


FIGURE 22. ISL6146C SLOW RAMP DISCONNECT 12V ORing

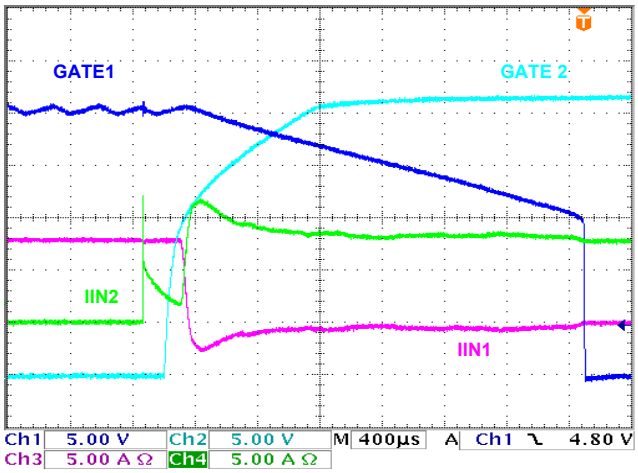


FIGURE 23. ISL6146C HOT SWAP CONNECT 12V ORing

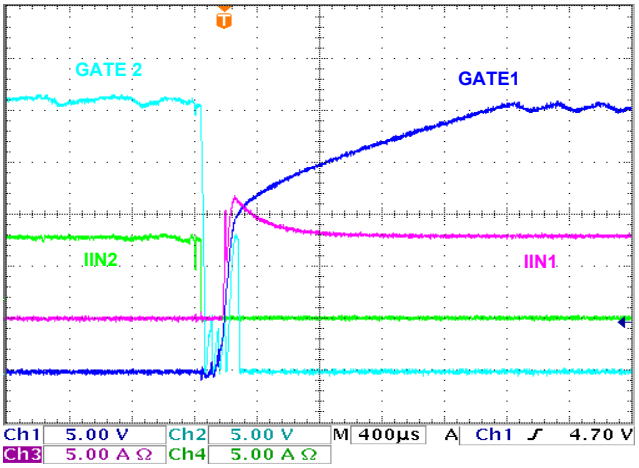


FIGURE 24. ISL6146C HOT DISCONNECT 12V ORing

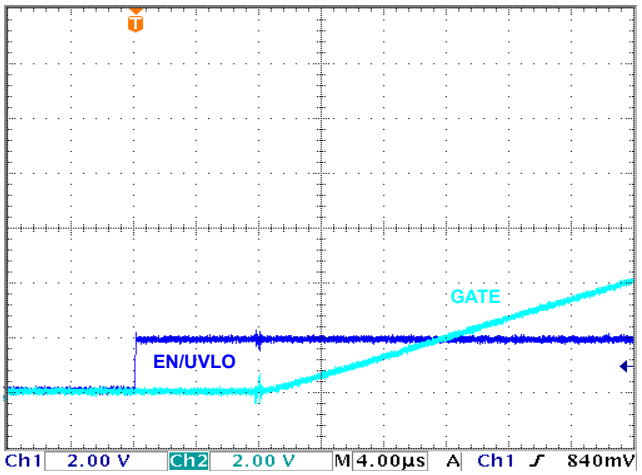


FIGURE 25. ISL6146A EN/ISL6146C UVLO TO GATE ON DELAY

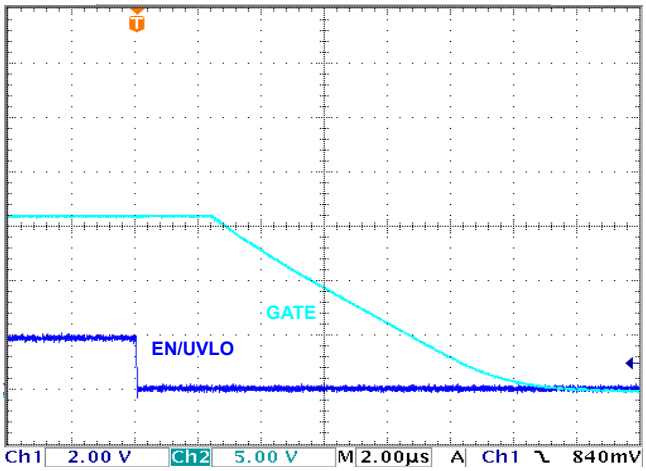


FIGURE 26. ISL6146A EN/ISL6146C UVLO TO GATE OFF DELAY

Typical Performance Curves (Continued)

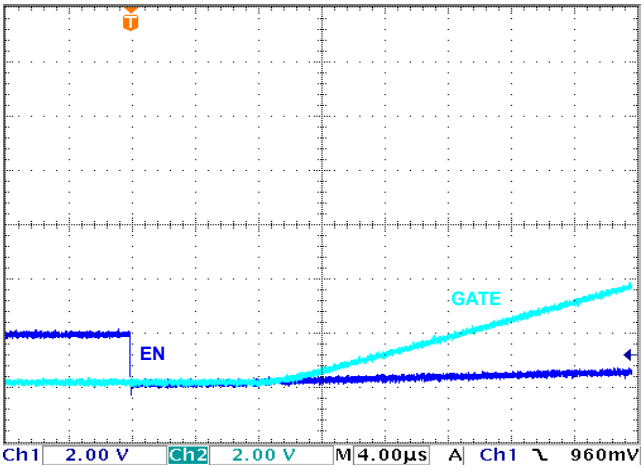


FIGURE 27. ISL6146B EN TO GATE ON DELAY

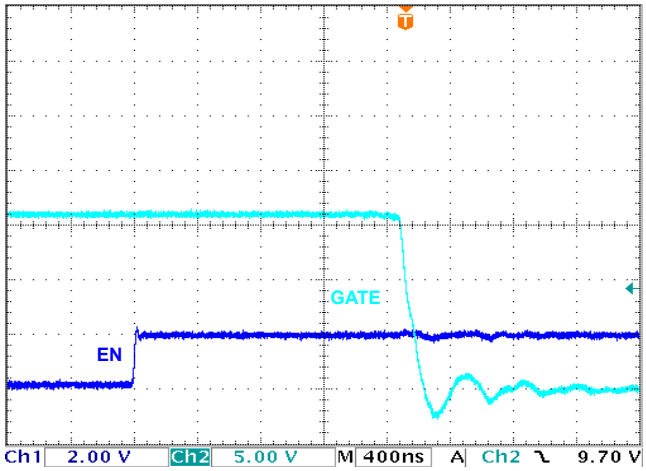


FIGURE 28. ISL6146B EN TO GATE OFF DELAY

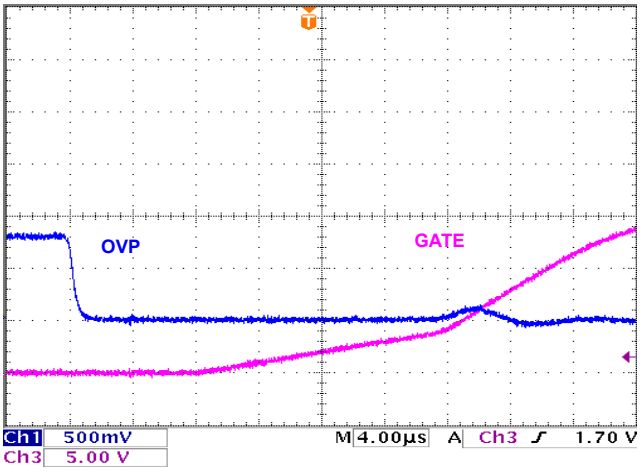


FIGURE 29. ISL6146C OVP TO GATE ON DELAY

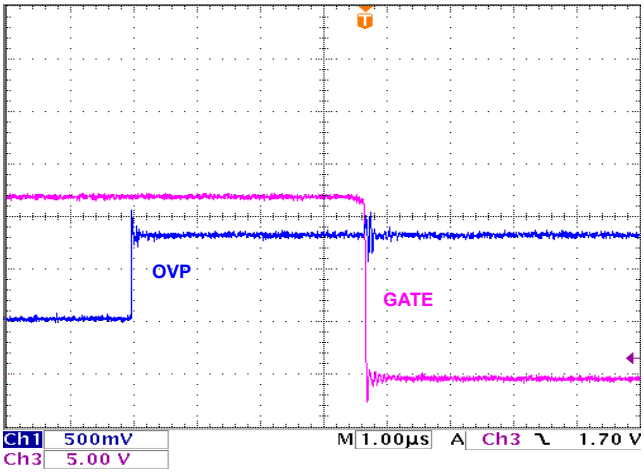


FIGURE 30. ISL6146C OVP TO GATE OFF DELAY

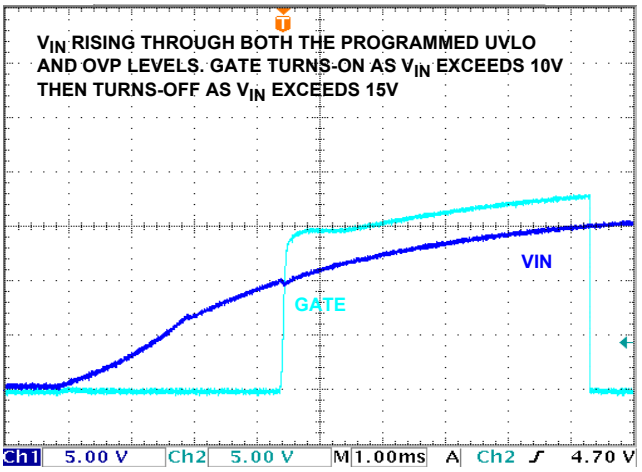


FIGURE 31. ISL6146C RISING V_{IN}, UVLO AND OVP FUNCTION

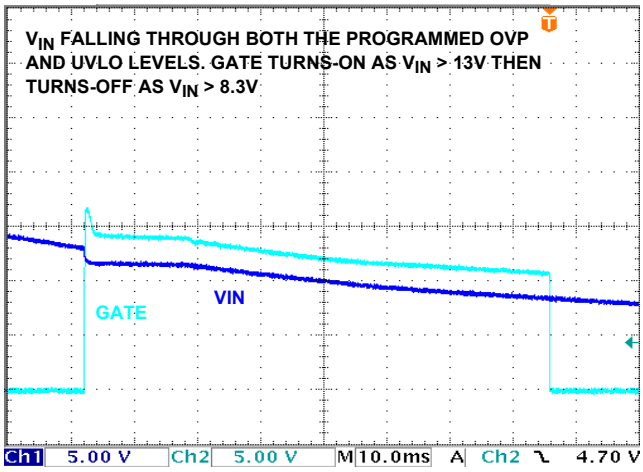


FIGURE 32. ISL6146C FALLING, V_{IN} OVP AND UVLO FUNCTION

Typical Performance Curves (Continued)

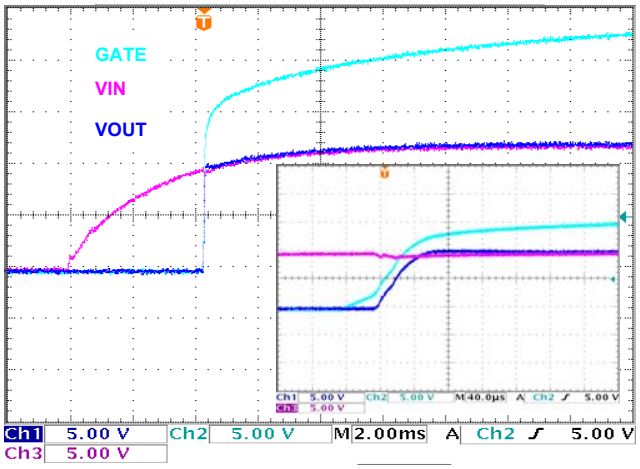


FIGURE 33. BACK-TO-BACK FET TURN_ON DETAIL

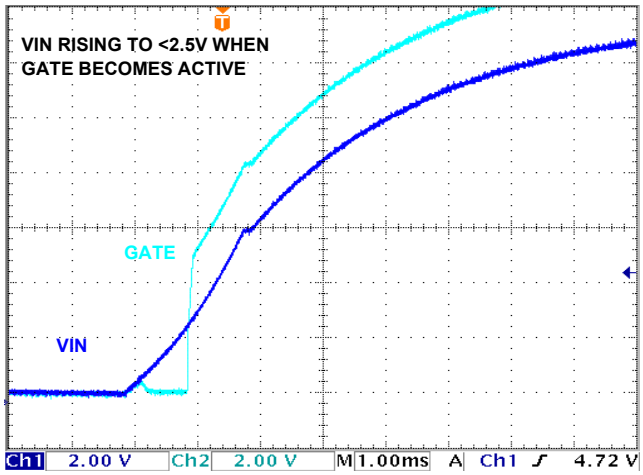


FIGURE 34. ISL6146 RISING POR Vth

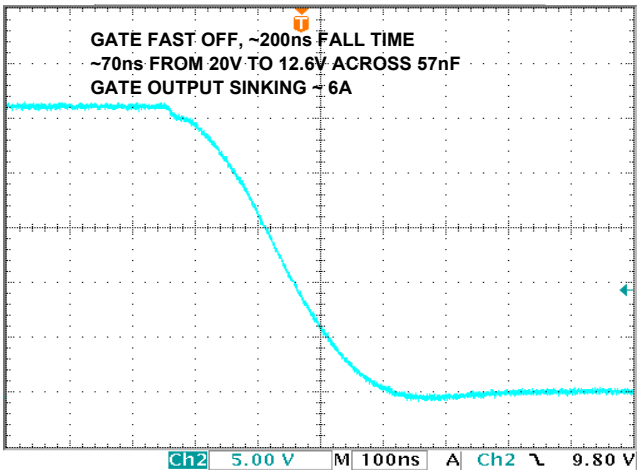


FIGURE 35. FAST GATE TURN-OFF WITH 57nF GATE

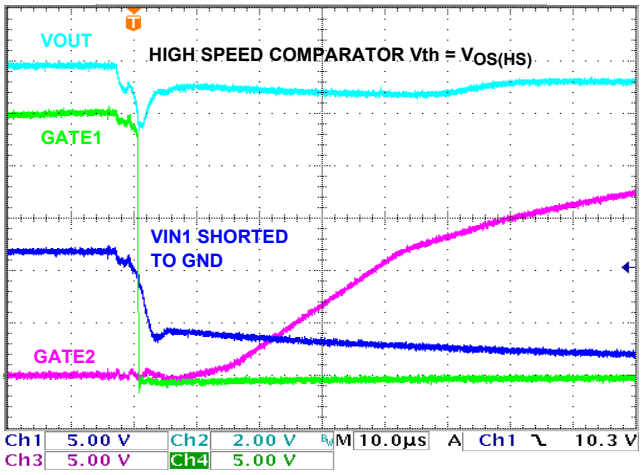


FIGURE 36. RESPONSE TO V_{IN} SHORTED TO GND WITH ADJ SHORTED TO V_{OUT}

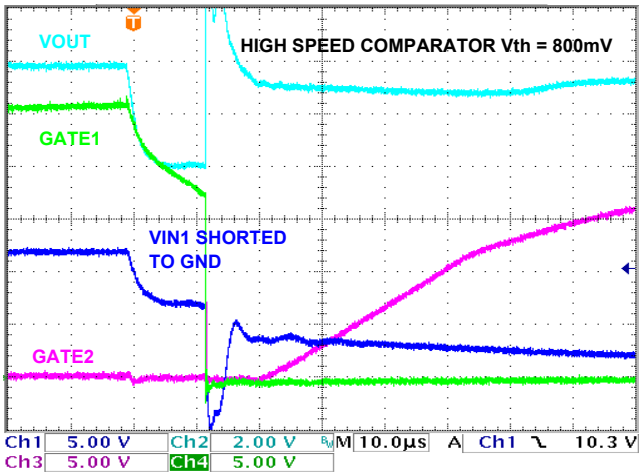


FIGURE 37. RESPONSE TO V_{IN} SHORTED TO GND WITH ADJ 5kΩ TO GND

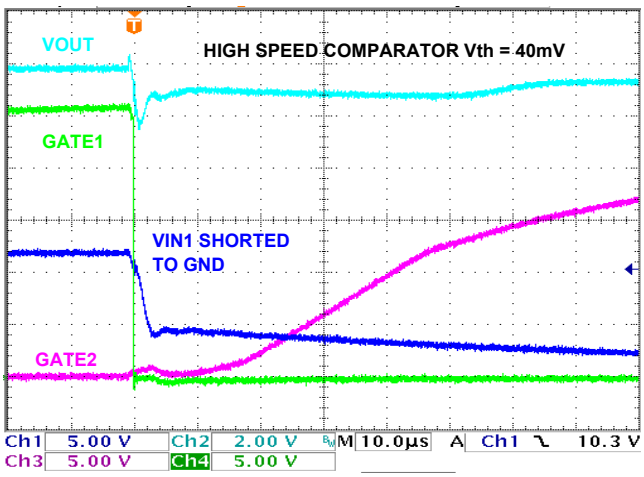


FIGURE 38. RESPONSE TO V_{IN} SHORTED TO GND WITH ADJ 100kΩ TO GND

Typical Performance Curves (Continued)

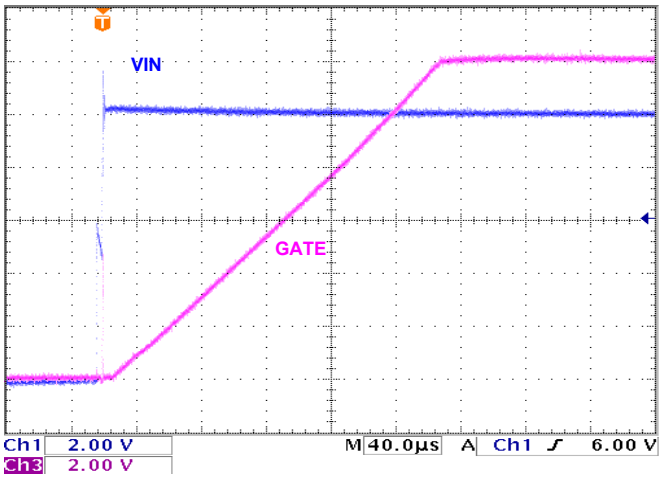


FIGURE 39. V_{IN} HOT SWAPPED TO GATE WITH BIAS = 12V NO LOAD

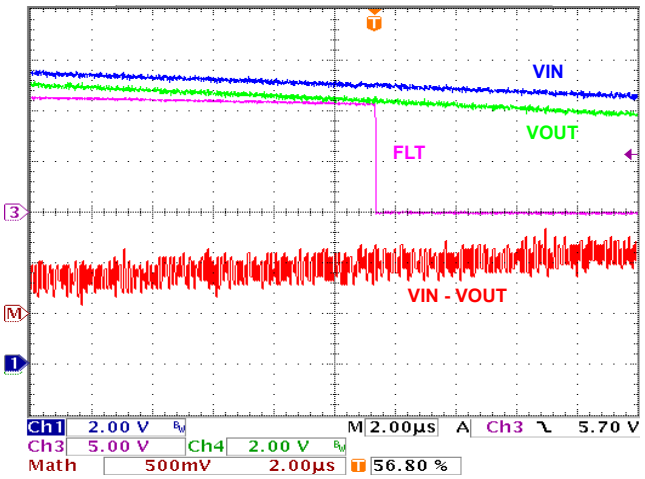


FIGURE 40. FAULT ASSERTING V_{IN} TO V_{OUT} > V_{FWD_FLT}

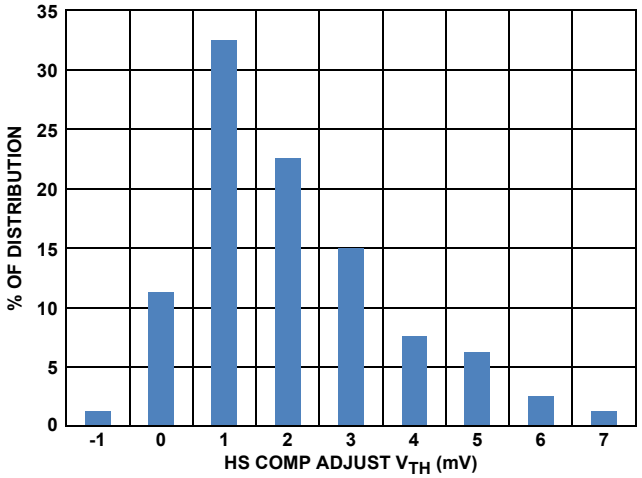


FIGURE 41. HIGH SPEED COMPARATOR OFFSET VOLTAGE

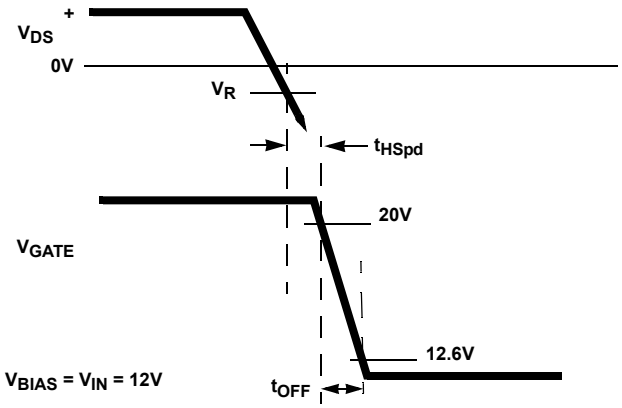


FIGURE 42. FAST RAMP REVERSE PROTECTION TIMING DIAGRAM

Functional Description

Functional Overview

In a redundant power distribution system, similar potential and parallel power supplies each contribute to the load current through various active and passive current sharing schemes. Typically ORing power diodes are used to protect against reverse current flow in the event that one of the power supplies falls below the common bus voltage or develops a catastrophic failure. However, using a discrete ORing diode solution has some significant drawbacks. The primary downside is the increased power dissipation loss in the ORing diodes as system power requirements increase. At the lowest voltages where the ISL6146 is designed for use, the voltage distribution losses across an ORing diode can be a significant percentage, in some cases approaching 70%. Another disadvantage when using an ORing diode, is failure to detect a shorted or opened current path which jeopardizes system power availability and reliability. An open diode may reduce the system to a single point of failure while a shorted diode eliminates the system's power protection.

Using an active ORing FET controller such as the ISL6146 helps with these potential issues. The use of a low on-resistance FET as the ORing component allows for a more efficient system design as the voltage across the FET is much lower than that across a forward biased diode. Additionally, the ISL6146 has a dedicated fault (FAULT) output pin that will indicate when there is a conditional or FET fault short providing the diagnostic capability a diode is unable to.

The ISL6146 is designed to OR together voltages as low as 1V when supplied with a separate bias supply of 3V or greater. Otherwise, the ISL6146 is designed to be biased from and OR voltages across the 3V to 20V nominal supply range.

In a single FET configuration as voltage is first applied to a VIN pin, the FET body diode conducts providing all the ISL6146s connected on a common bus circuit, bias via the VOUT pins. As individual power supply voltages ramp up in excess of the rising POR threshold, the ISL6146's internal charge pump activates to provide a floating gate drive voltage for the external N-channel ORing MOSFET, thus turning the FETs on once $V_{IN} > V_{OUT}$. The ISL6146 continuously monitors the drain and source of the ORing FET and provides a reverse voltage (N-channel MOSFET $V_{OUT} - V_{IN}$) detection threshold (VR) that, when exceeded, indicates a reverse current condition. Once this threshold is exceeded, the ISL6146 will turn-off the ORing FET by pulling down the GATE pin to GND. The ISL6146 also provides high speed $V_{OUT} > V_{IN}$ transient protection as in the case of a catastrophic VIN failure. The ISL6146 additionally provides for adjustment of the $V_{IN} - V_{OUT}$ reverse voltage Vth(VR Vth) via the ADJ pin of the ISL6146 with an external resistor to GND. This allows adjusting the $V_{IN} - V_{OUT}$ voltage threshold level to compensate for normal system voltage fluctuations, thus eliminating unnecessary reaction by the ISL6146.

The total $V_{IN} - V_{OUT}$ VR Vth is the sum of both the internal offset and the external programmed VR Vth.

In the event of a $V_{OUT} > V_{IN}$ condition, the ISL6146 responds either with a high or low current pull-down on the GATE pin depending on whether the High Speed comparator (HSCOMP) has been activated or not. The HSCOMP determines if the VR occurred within 1µs by continuously sampling the FET VDS and if so, the high pull-down current is used to turn off the ORing FET. In the event of a falling VIN transition in <1µs, (i.e., a catastrophic failure of the power source) the HSCOMP protects the common bus from the individual faulted power supply short by turning off the shorted supply's ORing MOSFET in less than 300ns, ensuring the integrity of the common bus voltage from reverse current to the damaged supply.

Once the correct $V_{IN} > V_{OUT}$ relationship is established again, the ISL6146 will again turn on the FET.

The FAULT pin is an open drain, active low output indicating that a fault or specific condition has occurred, these include:

- GATE is OFF (GATE < V_{IN}+0.2V). Lack of conduction, not a fault, just not on.
- Faults resulting in $V_{IN} - V_{OUT} > 0.57V$ when ON.
- An open FET resulting in body diode conduction
- Excessive current through FET
- FET Faults monitored and reported include
  - G-D, gate unable to drive to Q-pump voltage
  - G-S, gate unable to drive to Q-pump voltage
  - D-S shorts, when GATE is OFF VDS < 2V
  - V_{IN} < POR
  - Missing V_{IN}
  - V_{IN} shorted to GND

On the ISL6146C version, a conditional fault will also be signalled if the V_{IN} is not within the programmed UVLO and OVP levels.

The ISL6146 has an on-chip over-temperature fault threshold of ~+140°C with a 20°C hysteresis. Although the ISL6146 itself produces little heat, it senses the environment in which it is, likely including a close by FET.

The ISL6146A and ISL6146B are functional variants with an enabling input of either polarity. This feature is used when the need to interrupt the current path via signaling is necessary. This is accomplished by implementing two FETs in series so that there is a body diode positioned to block current in either direction. This functionality is considered an additional enhancement to the ORing diode it replaces.

The ISL6146C employs the use of a programmable Undervoltage Lock Out (UVLO) and a programmable Overvoltage Protection (OVP) input. This allows the GATE to only turn-on when the monitored voltage is between the programmed lower and upper levels. This application would use the back-to-back FET configuration. In the event the current path does not need to be interrupted then the EN, UVLO and OVP inputs can all be overridden.

Applications Information

Power-Up Considerations

BIAS AND V_{IN} CONSTRAINTS

Upon power-up when the V_{IN} supply is separate from the BIAS supply, the BIAS voltage must be greater or equal to the V_{IN} voltage at all times.

When using a single supply for both the ISL6146 bias and the ORing supply, the V_{IN} and BIAS pins can be configured with a low value resistor between the two pins to provide some isolation and decoupling to support the chip bias even as the OR'd supply experiences voltage droops and surges. Although not necessary to do so, it is a best design practice for particularly noisy environments.

FET TO IC LAYOUT RECOMMENDATIONS

Connections from the FET(s) to the ISL6146 VIN and VOUT pins must be kelvin in nature, as close to the FET drain and source PCB pads as possible to eliminate any trace resistance errors that can occur with high currents. This connection placement is most critical to providing the most accurate voltage sensing particularly when the back-to-back FET configuration is used. Likewise, connections from OVP, UVLO and ADJ are also critical to optimize accuracy.

ADJUSTING THE HS COMPARATOR REVERSE VOLTAGE THRESHOLD

The ISL6146 allows adjustment of the HS Comparator reverse voltage detection threshold (VR Vth), the difference in V_{OUT} - V_{IN}.

There are two valid ADJ pin configurations:

1. ADJ connected to VOUT: This makes the HS comparator threshold equal to the intrinsic error in the HS comparator input. This is the default condition and the most likely used configuration.
2. A single resistor is connected from ADJ pin to ground: Making the HS comparator threshold = V_{OUT} - $4k/R_{ADJ}$. Where $4k = 0.4(V_{ADJ})*10k\Omega$

So, for a 100kΩ R_{EXT}, HS Comparator threshold = 40mV and for a 5kΩ R_{EXT} HS comparator threshold = ~ 800mV.

The recommended resistor range is 5kΩ to 100kΩ for this voltage adjustment.

At power-up, the HS comparator threshold is default set to the internal device error first, and then released to the user programmed threshold after the related circuits are ready. It takes ~20µs for the circuit to switch from the default setting to the user programmed threshold after a POR startup.

The current out of the ADJ pin with a resistor to GND is equal to 0.4V of the ADJ resistor.

BACK-TO-BACK FET CONFIGURATION

When using the back-to-back FET configuration, the FET choice must be such that the voltage across both FETs at full current loading be less than the minimum forward voltage fault threshold of 400mV to avoid unintended fault notification.

In this configuration, it may be tempting to use the enable inputs to force a path by switching between the two as opposed to having both paths on and having the higher voltage source provide current. The problem with that is the timing of the FETs on and off so that excessive V_{OUT} voltage droop is not introduced if the turn-off happens faster or before the turn-on momentarily leaves inadequate power to the load.

Typical Applications Circuits

There are four basic configurations that the ISL6146 can be used in:

1. For voltages >3V where the BIAS and V_{IN} are common
2. For a very low ORing voltage, <3V operation, BIAS >3V
3. For a voltage window compliant operation and
4. For a signaled operation where the current path is controlled by an input signal or minimum voltage condition.

Each of these configurations can be tailored for the High Speed Comparator (HS COMP) reverse threshold via the ADJ input being connected either to VOUT or to GND via a resistor as explained previously. Additionally, the voltage window is adjustable for both a minimum and maximum operating voltage via the UVLO and OVP inputs and a resistor divider also explained earlier. Also soft-start and turn-on and turn-off characteristics can be tailored to suit.

The three evaluation platforms provided demonstrate the four basic configurations and provide for the additional tailoring of the various performance characteristics.

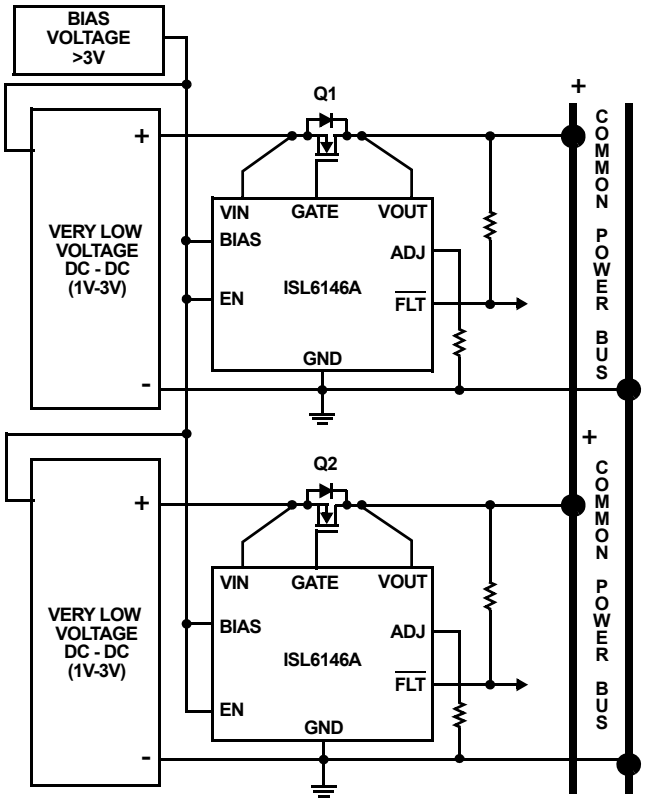


FIGURE 43. LOW VOLTAGE APPLICATION DIAGRAM

The Figure 1 circuit shown on page 1 is the basic circuit used for ORing voltages >3V to 20V.

The ISL6146A application shown in Figure 43 is the configuration for ORing very low voltages of 1V to 3V. Additionally, this application shows the utilization of the ADJ input with a single resistor tied to GND. This provides the user a programmable level of $V_{OUT} > V_{IN}$ before the High Speed (HS) Comparator is activated and the GATE output is pulled down to allow for normal voltage fluctuations in the system.

Notice that in both of these circuits, the EN or $\overline{EN}$ inputs are defaulted to enabled and have no current path on/off control. Failure to do so correctly will result in only body diode conduction and a resulting fault indication.

The V_{IN} and V_{OUT} to FET and GND to ADJ connections are drawn to emphasize the Kelvin connection necessary to correctly monitor the voltage across the FET, and for the VR Vth monitor to eliminate any stray resistance effects.

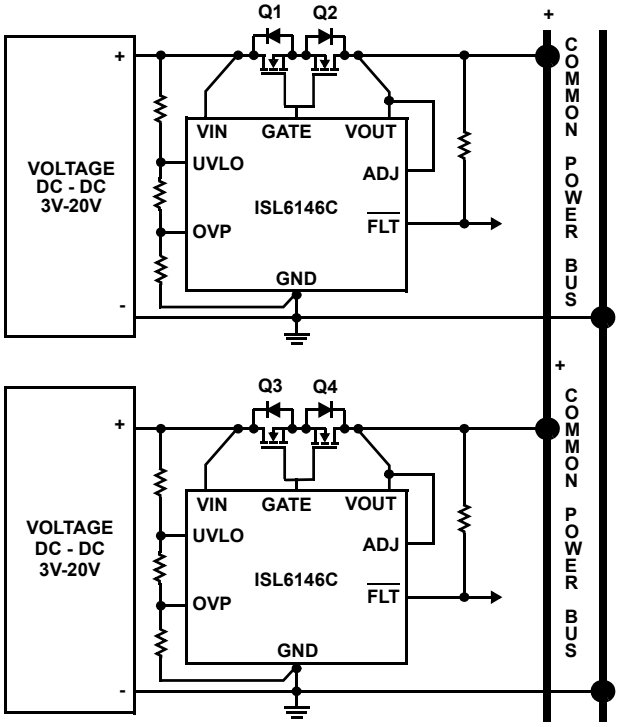


FIGURE 44. TYPICAL ISL6146C APPLICATION DIAGRAM

The ISL6146C application shown in Figure 44 is limited to the 3V to 20V V_{IN} range and must implement the back-to-back FET configuration to utilize the UVLO and OVP inputs and capabilities. As the V_{IN} voltage rises above the minimum programmed voltage, the related ORing FETs will turn on and stay on until either the minimum voltage requirement is no longer met or the V_{IN} voltage exceeds its programmed maximum. The minimum and maximum programmed voltage levels are done with the resistor divider on the UVLO and OVP pins. These levels should be programmed to take into account conduction path losses to the load in addition to the IC operational constraints.

When using the back-to-back FET configuration, the user must chose FETs to ensure $(2r_{DS(ON)} + PCB\ IR)\ I_{LOAD} < 0.5V$ to avoid tripping the $V_{IN} - V_{OUT} > 0.5V$ when ON fault.

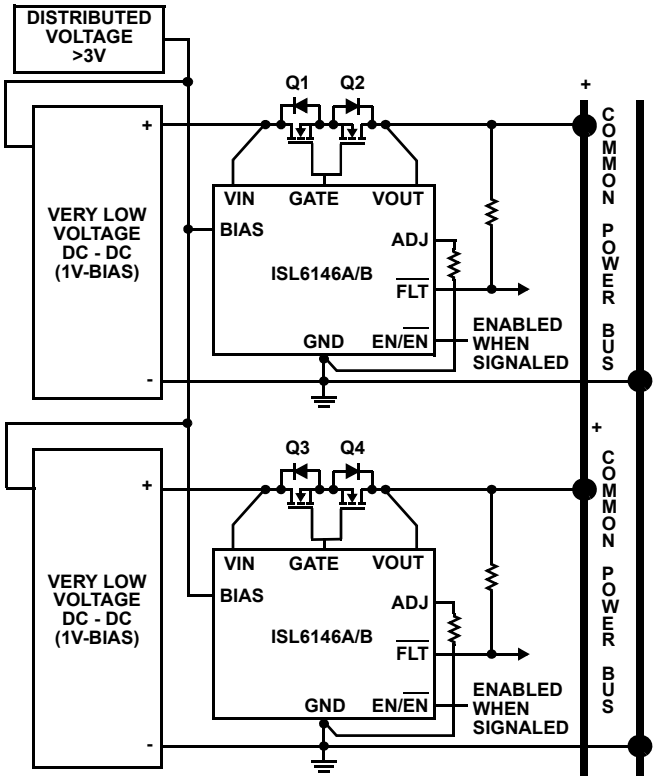


FIGURE 45. CONTROLLED ON/OFF APPLICATION DIAGRAM

The application diagram in Figure 45 shows the ISL6146A or ISL6146B utilizing the EN or $\overline{EN}$ pin as a signalled input to open or close the conduction path from power supply to load. This feature can be implemented on ORing 1V to 20V but is shown for ORing <3V.

The enable input signaling can be simultaneous across the N+1 number of ISL6146s used.

Although not needed for thermal relief, connect the DFN EPAD to GND.

ISL6146 Evaluation Platforms

Description and Use of the Evaluation Boards

The three ISL6146 evaluation boards are to demonstrate the four application configurations discussed earlier. All the boards have ADJ shorted to VOUT with the PCB layout having the component footprints to insert a resistor of choice between ADJ and GND to adjust the HS COMP Vth. Likewise, the VIN is connected to BIAS but these can be separated to provide an adequate BIAS voltage when ORing <3V supplies or if providing a separate from VIN voltage to BIAS.

The **ISL6146AEVAL1Z** is configured as having a 8.5V minimum turn-on threshold with a 1.2V hysteresis.

The **ISL6146BEVAL1Z** is configured as a minimally featured maximum performance ORing FET controller for 3V to 20V.

The **ISL6146CEVAL1Z** is configured to operate with a 10.8V lower turn on threshold and 14.9V upper turn-off threshold.

All three boards are equipped with 50A capable FETs for high current evaluations and with a minimum of V_{IN} and V_{OUT} bulk capacitance likely to be found in any power system design.

After determining the BIAS source along with V_{IN} voltage criteria and configuring the evaluation board if necessary for the application to be evaluated the board is ready for power.

Apply the BIAS voltage first (via the test points labeled BIAS), if separate from VIN, then the V_{IN} voltage. Monitor the provided test points for device performance with current loads up to 50A.

Figures 46 through 51 illustrate the three ISL6146 evaluation boards for the three typical applications in photograph and schematic form.

Figure 52 shows an external voltage switchover circuit as would be used with an external DC supply up to 24V. This circuit uses a P-channel FET driven from the $\overline{FLT}$ output. Since the ISL6146 FLT output is not a simple status output, the P-FET will be turned off when any of the FLT conditions exist on the ISL6146.

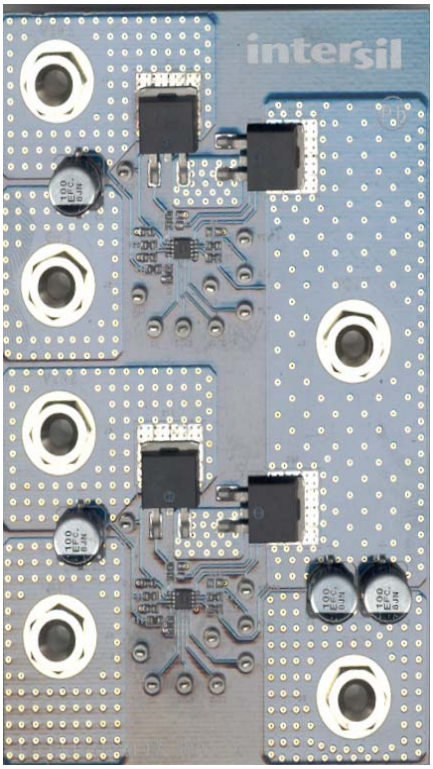


FIGURE 46. ISL6146AEVAL1Z PHOTOGRAPH

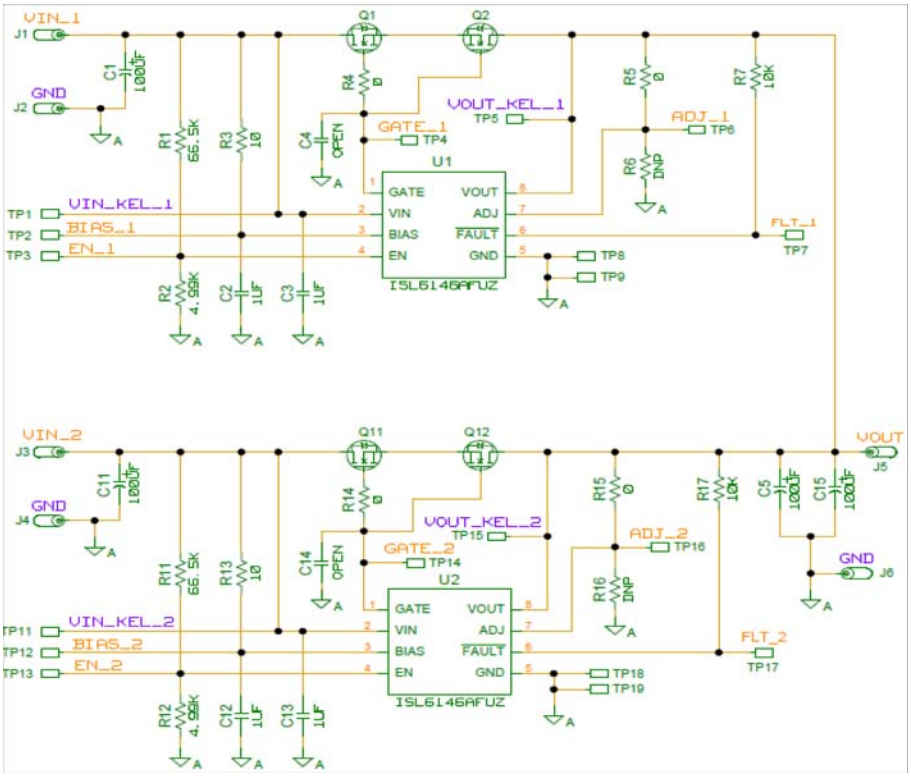


FIGURE 47. ISL6146AEVAL1Z SCHEMATIC

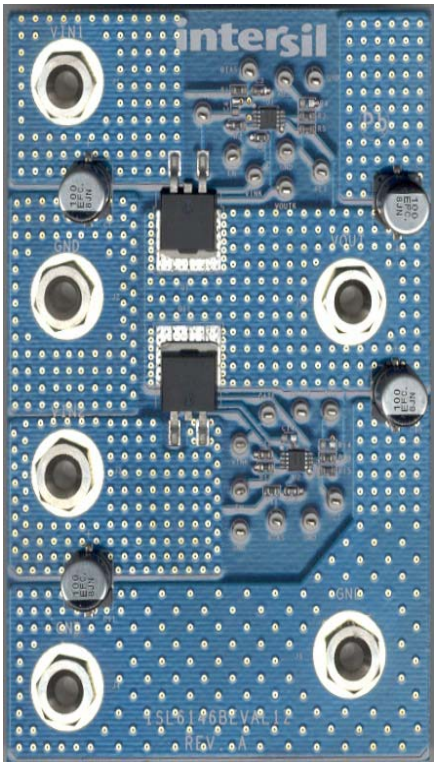


FIGURE 48. ISL6146BEVAL1Z PHOTOGRAPH

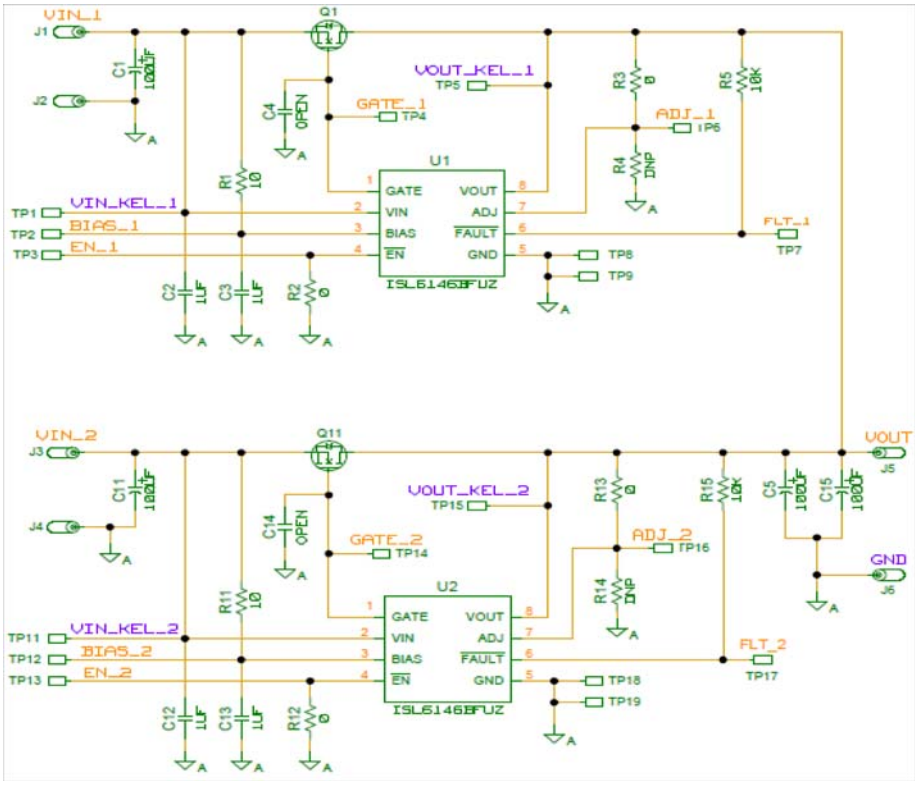


FIGURE 49. ISL6146BEVAL1Z SCHEMATIC

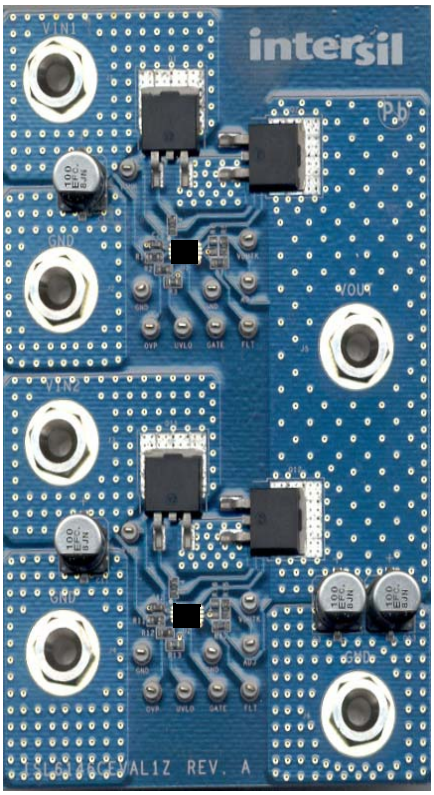


FIGURE 50. ISL6146CEVAL1Z PHOTOGRAPH

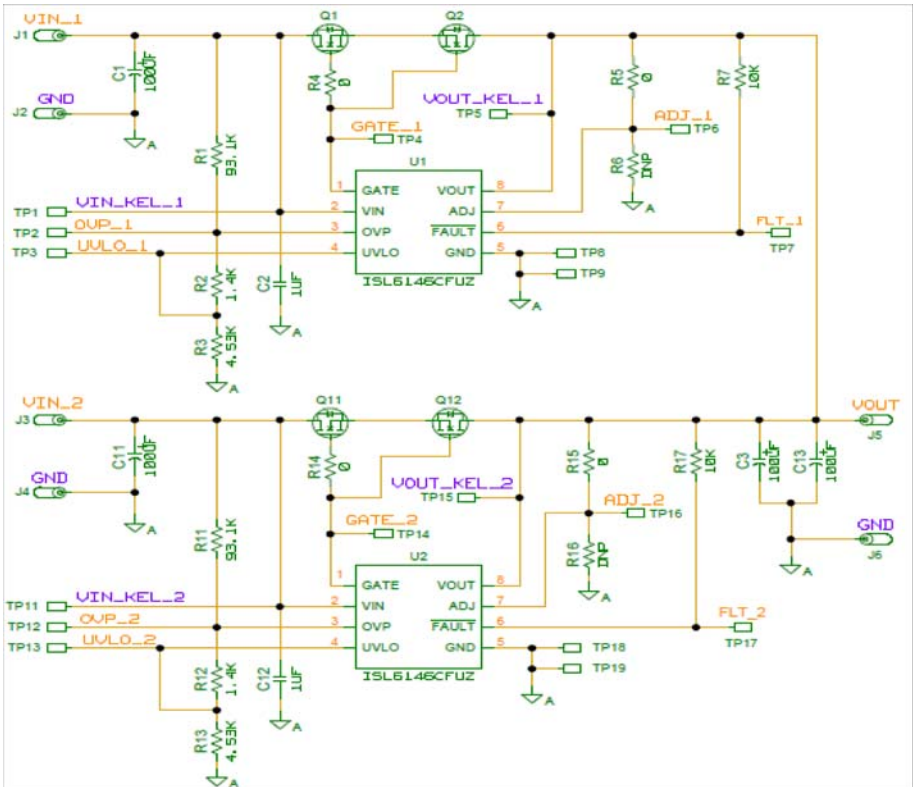


FIGURE 51. ISL6146CEVAL1Z SCHEMATIC (UVLO AND OVP TEST POINT LABELS ARE SWAPPED)

With V_{IN} present, the ISL6146 will control and enhance Q2 as expected. When V_{EXT} is applied, Q1 body diode will conduct when $V_{EXT} > V_{OUT}$, at which time the ISL6146 $V_{OUT} > V_{IN}$ and will turn off Q2 and pull the $\overline{FLT}$ output low. FLT pulling low will turn-on the P-FET Q1 and the output will have switched from V_{IN} to V_{EXT}.

When V_{EXT} is removed and ISL6146 $V_{IN} > V_{OUT}$, Q2 will be turned on and Q1 turned off as $\overline{FLT}$ is released to pull high.

The ISL6146 FLT output is not a simple conduction status output, but is used to report a multitude of faults. Any of these faults will cause $\overline{FLT}$ to pull low but V_{EXT} to output will not be interrupted.

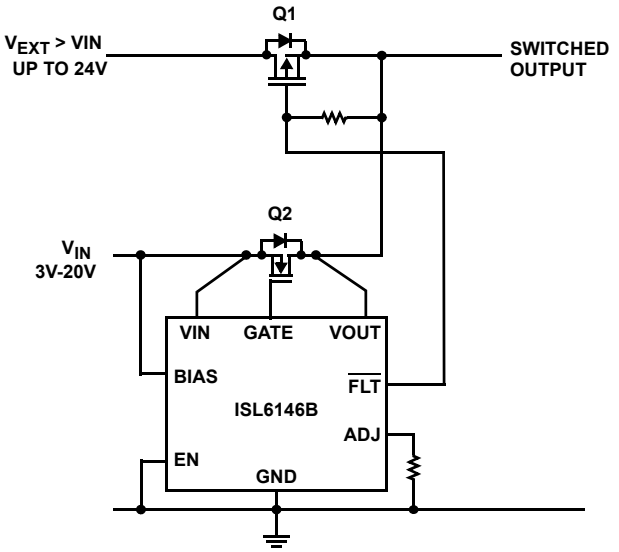


FIGURE 52. ISL6146B EXTERNAL SWITCHOVER SCHEMATIC

TABLE 2. ISL6146xEVALZ BOM

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
ISL6146AEVAL1Z				
U1, U2		ISL6146A ORing FET Controller	Intersil	ISL6146AFUZ
Q1, Q2, Q11, Q12		30V, 50A FET	Various	
R1, 11	66.5kΩ	RES, SMD, 0603, 1%	Generic	
R2, R12, R6, R16	4.99kΩ	RES, SMD, 0603, 1%	Generic	
R3, R13	10Ω	RES, SMD, 0603, 1%	Generic	
R4, R14	0Ω	RES, SMD, 0603, 1%	Generic	
R5, R15	DNP	RES, SMD, 0603, 1%	Generic	
R7, R17	10kΩ	RES, SMD, 0603, 1%	Generic	
C1, C11, C5 C15	100µF	Alum. Elect SMD Cap	Generic	
C2, C3, C12 C13	1µF	CAP, SMD, 0603, 50V, 10%	Generic	
C4, C14	DNP	CAP, SMD, 0603, 50V, 10%	Generic	
TPx		Test Point	Generic	
Jx		Banana Jack	Generic	
ISL6146BEVAL1Z				
U1, U2		ISL6146B ORing FET Controller	Intersil	ISL6146BFUZ
Q1, Q11		30V, 50A FET	Various	
R4, R14	4.99kΩ	RES, SMD, 0603, 1%	Generic	
R1, R10	10Ω	RES, SMD, 0603, 1%	Generic	
R2, R12	0Ω	RES, SMD, 0603, 1%	Generic	
R3, R13	DNP	RES, SMD, 0603, 1%	Generic	
R5, R15	10kΩ	RES, SMD, 0603, 1%	Generic	
C1, C11, C5 C15	100µF	ALum. Elect SMD Cap	Generic	
C2, C3, C12 C13	1µF	CAP, SMD, 0603, 50V, 10%	Generic	
C4, C14	DNP	CAP, SMD, 0603, 50V, 10%	Generic	
TPx		Test Point	Generic	
Jx		Banana Jack	Generic	

TABLE 2. ISL6146xEVALZ BOM (Continued)

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
ISL6146CEVAL1Z				
U1, U2		ISL6146C ORing FET Controller	Intersil	ISL6146CFUZ
Q1, Q2, Q11, Q12		30V, 50A FET	Various	
R1, 11	93.1kΩ	RES, SMD, 0603, 1%	Generic	
R2, R12	1.4kΩ	RES, SMD, 0603, 1%	Generic	
R3, R13	4.53kΩ	RES, SMD, 0603, 1%	Generic	
R4, R14	0Ω	RES, SMD, 0603, 1%	Generic	
R5, R15	DNP	RES, SMD, 0603, 1%	Generic	
R6, R16	4.99kΩ	RES, SMD, 0603, 1%	Generic	
R7, R17	10kΩ	RES, SMD, 0603, 1%	Generic	
C1, C11, C3 C13	100µF	ALum. Elect SMD Cap	Generic	
C2, C12	1µF	CAP, SMD, 0603, 50V, 10%	Generic	
TPx		Test Point	Generic	
Jx		Banana Jack	Generic	

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 16, 2011	FN7667.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6146

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

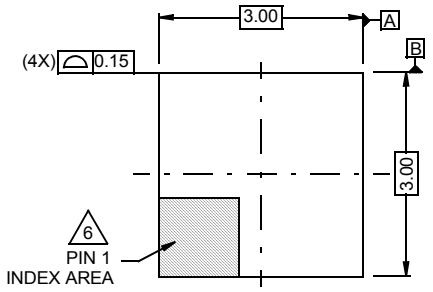
FITs are available from our website at: http://rel.intersil.com/reports/sear

Package Outline Drawing

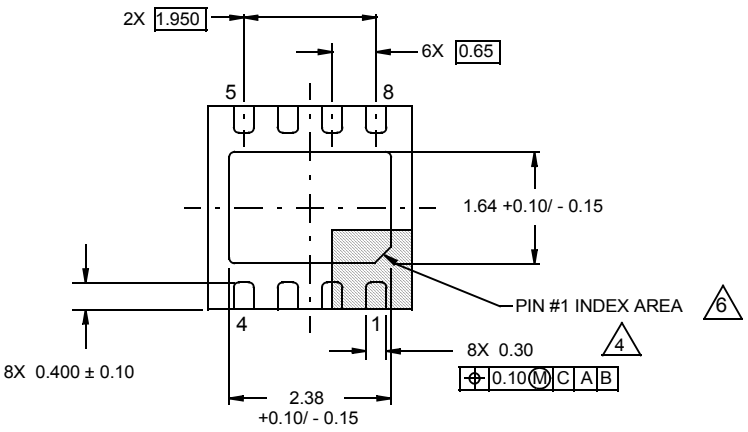
L8.3x3J

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

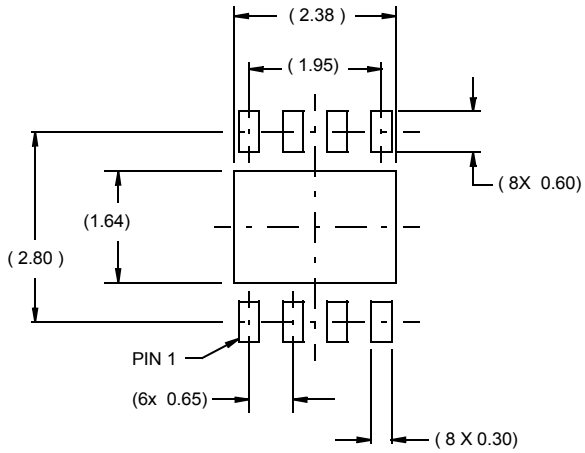
Rev 0 9/09



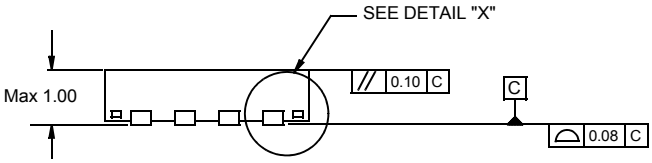
TOP VIEW



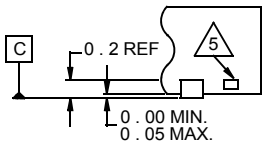
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

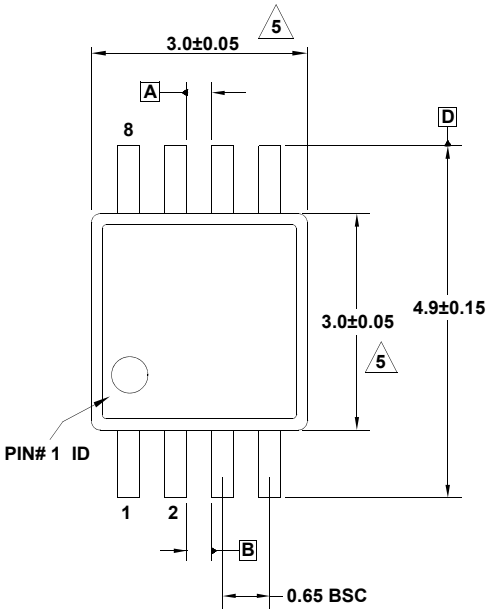
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

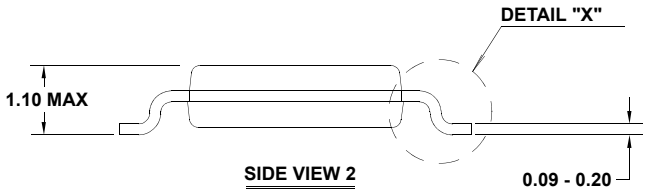
M8.118

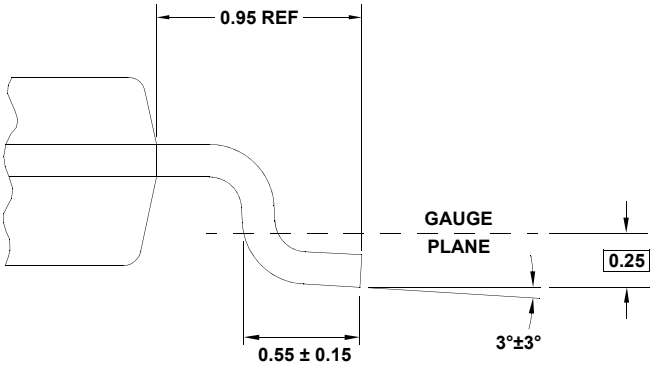
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

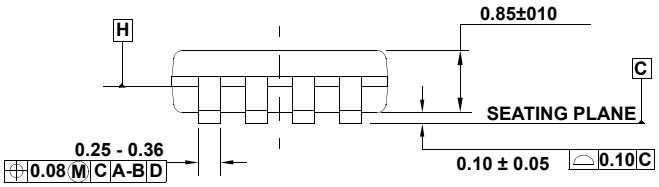


TOP VIEW

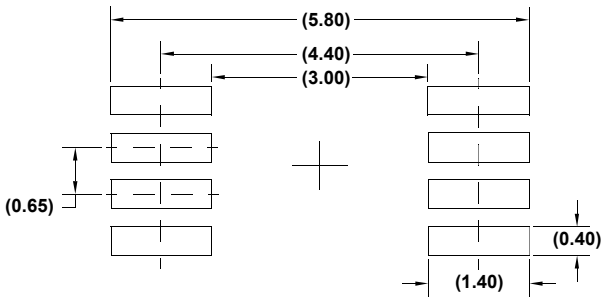




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.