Data Sheet | August 20, 2007 | FN6538.0

5V or 12V Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6341, ISL6341A, ISL6341B makes simple work out of implementing a complete control and protection scheme for a DC/DC stepdown converter driving N-Channel MOSFETs in a synchronous buck topology. Since it can work with either 5V or 12V supplies, this one IC can be used in a wide variety of applications within a system. The ISL6341, ISL6341A, ISL6341B integrates the control, gate drivers, output adjustment, monitoring and protection functions into a single 10 Ld Thin DFN package.

The ISL6341, ISL6341A, ISL6341B provides single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±0.8% over temperature and line voltage variations. A fixed frequency oscillator (300kHz for ISL6341; 600kHz for ISL6341A, ISL6341B) reduces design complexity, while balancing typical application cost and efficiency. The PWM duty cycles range from 0% to around 85% at 300kHz (75% at 600kHz). The frequency, duty cycle and OCP are the only differences among the ISL6341, ISL6341A, ISL6341B. See Table 1 for a summary.

Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the lower MOSFET to inhibit PWM operation appropriately (the ISL6341, ISL6341B are slightly different from the ISL6341A; see “Overcurrent Protection (OCP)” on page 7 for details). This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor. The output voltage is also monitored for undervoltage and overvoltage protection, in addition to monitoring for a PGOOD output.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6341ACRZ*	41AC	0 to +70	10 Ld 3x3 TDFN	L10.3x3B
ISL6341BCRZ*	41BC	0 to +70	10 Ld 3x3 TDFN	L10.3x3B
ISL6341CRZ*	341C	0 to +70	10 Ld 3x3 TDFN	L10.3x3B
ISL6341AIRZ*	41AI	-40 to +85	10 Ld 3x3 TDFN	L10.3x3B
ISL6341BIRZ*	41BI	-40 to +85	10 Ld 3x3 TDFN	L10.3x3B
ISL6341IRZ*	6341	-40 to +85	10 Ld 3x3 TDFN	L10.3x3B
ISL6341EVAL1Z	Evaluation Board			

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

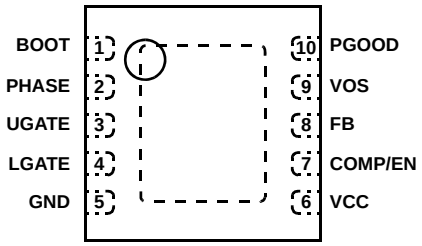
- Operates from +4.5V to 14.4V Supply Voltage (for bias)
  - 1.5V to 12V V_{IN} Input Range (up to 20V is possible with restrictions; see “Input Voltage Considerations” on page 11)
  - 0.8V to ~V_{IN} Output Range (duty cycle limited)
  - Integrated Gate Drivers; LGATE Uses V_{CC} (5V to 12V); UGATE Uses External Boot Diode to 5V to 12V
  - 0.8V Internal Reference; ±0.8% Tolerance
- Simple Single-Loop Control Design
  - Traditional Dual Edge Modulator
  - Voltage-Mode PWM Control
  - Drives N-Channel MOSFETs
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - 0% to 85% Max Duty Cycle for ISL6341 (75% for ISL6341A, ISL6341B)
- Lossless, Programmable Overcurrent Protection
  - Uses Lower MOSFET’s $r_{DS(ON)}$
- Output Voltage Monitoring
  - Undervoltage and Overvoltage Shutdown
  - PGOOD Output
- Small Converter Size in 10 Ld 3x3 Thin DFN
  - 300kHz or 600kHz Fixed Frequency Oscillator
  - Fixed Internal Soft-Start, Capable into a Pre-biased Load
  - Enable/Shutdown Function on COMP/EN Pin
- Pb-Free Available (RoHS Compliant)

Applications

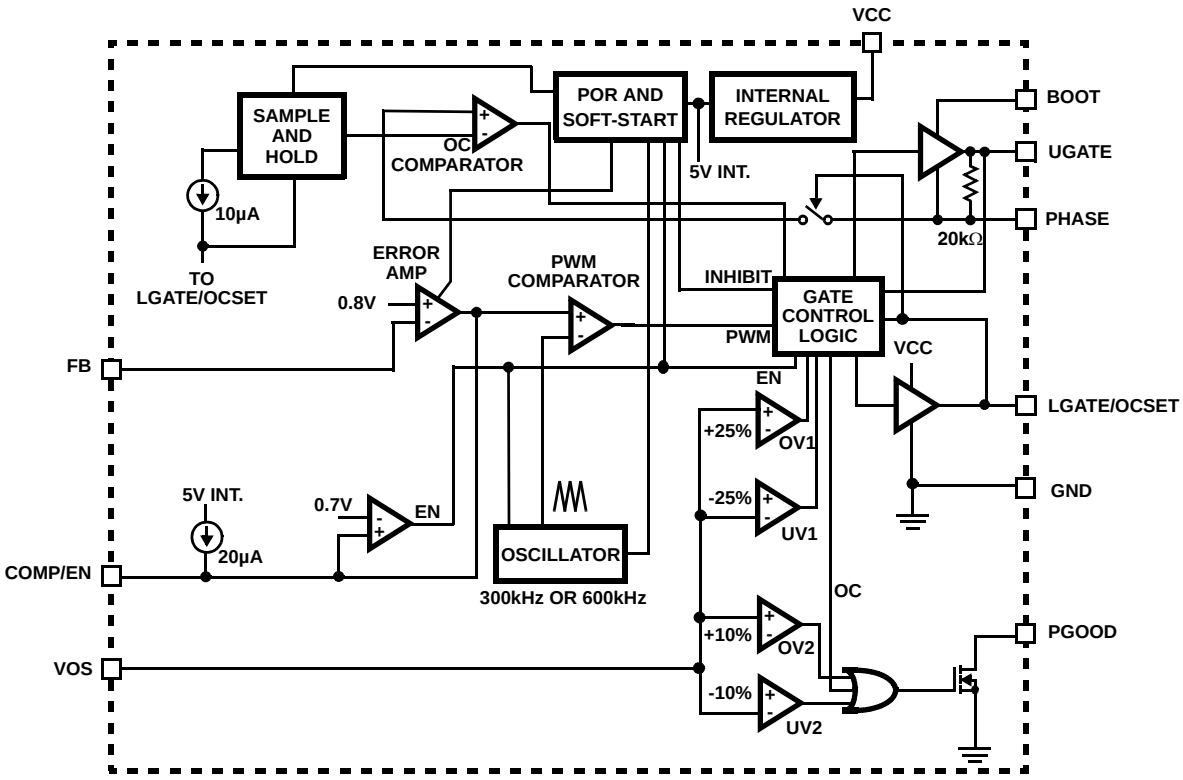
- Power Supplies for Microprocessors or Peripherals
  - PCs, Servers, Memory Supplies
  - DSP and Core Communications Processor Supplies
- Subsystem Power Supplies
  - PCI, AGP; Graphics Cards; Digital TV
  - SSTL-2 and DDR/DDR2/DDR3 SDRAM Bus Termination Supply
- Cable Modems, Set-Top Boxes, and DSL Modems
- Industrial Power Supplies; General Purpose Supplies
- 5V or 12V-Input DC/DC Regulators
- Low-Voltage Distributed Power Supplies; Point of Load

Pinout

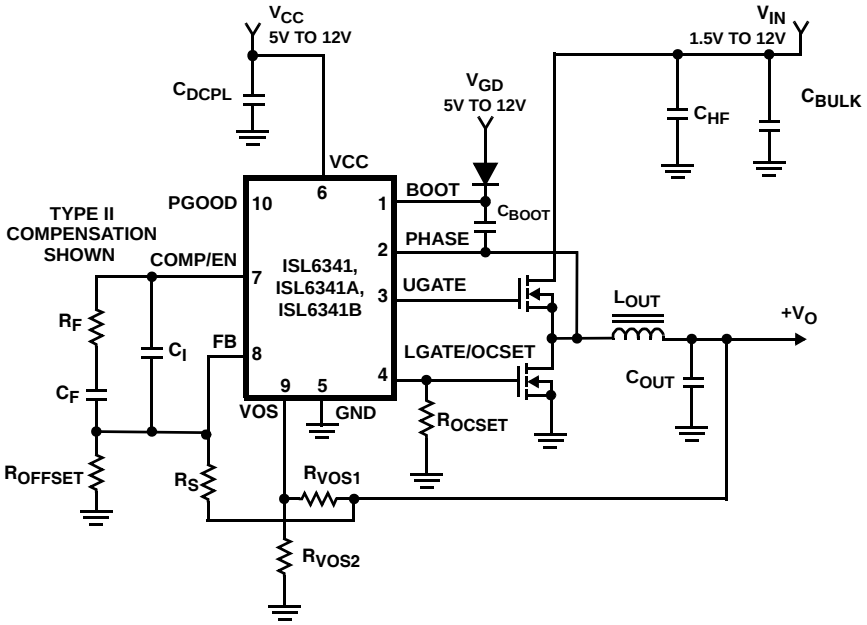
ISL6341, ISL6341A, ISL6341B
(10 LD 3x3 TDFN)
TOP VIEW



Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, (V_{CC}) . . . . . GND - 0.3V to 15V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . GND - 0.3V to 36V
BOOT to PHASE Voltage (V_{BOOT} - V_{PHASE}) . . . GND - 0.3V to 15V
-0.3V to 16V (<10ns, 10µJ)
UGATE Voltage (V_{UGATE}) . . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} +0.3V
LGATE/OCSET Voltage (V_{LGATE}) . . . . . GND - 0.3V to V_{CC} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{CC} + 0.3V
PHASE Voltage (V_{PHASE}) . . . . . GND - 0.3V to V_{BOOT} + 0.3V
GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT-GND}$ <36V)
FB, VOS, COMP/EN Voltage . . . . . GND - 0.3V to 6V
PGOOD Voltage. . . . . GND - 0.3V to 7V
ESD Rating
Human Body Model 2kV
Machine Model. 200V
Charged Device Model. 1.0kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld TDFN Package (Notes 1, 2). . . .	44	3.5

Maximum Power Dissipation. 1.0W
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Supply Voltage Range, V_{CC} . . . . . +4.5V to 14.4V
Ambient Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial. . . . . -40°C to +85°C
Junction Temperature Range. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air, with “direct attach” features. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Limits should be considered typical and are not production tested.
4. Limits established by characterization and are not production tested.

Electrical Specifications

Test Conditions: V_{CC} = 12V, T_J = 0 to +85°C, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Input Bias Supply Current	I_{VCC_dis}	V_{CC} = 12V; disabled		7.0		mA
Input Bias Supply Current	I_{VCC_en}	V_{CC} = 12V; enabled (but not switching)	6.4	8.9	10.4	mA
POWER-ON RESET						
Rising V_{CC} POR Threshold	V_{POR}		3.8	4.2	4.47	V
V_{CC} POR Threshold Hysteresis			0.15	0.48	0.85	V
OSCILLATOR						
Switching Frequency	f_{OSC}	ISL6341C	270	300	330	kHz
		ISL6341I	240	300	330	kHz
		ISL6341AC, ISL6341BC	540	600	660	kHz
		ISL6341AI, ISL6341BI	510	600	660	kHz
Ramp Amplitude (Note 3)	ΔV_{OSC}			1.5		V_{P-P}
REFERENCE						
Reference Voltage Tolerance	V_{REF}	ISL6341C, ISL6341AC, ISL6341BC	0.7936	0.8000	0.8064	V
		ISL6341I, ISL6341AI, ISL6341BI	0.7920	0.8000	0.8080	V
ERROR AMPLIFIER						
DC Gain (Note 3)	GAIN			96		dB
Gain-Bandwidth Product (Note 3)	GBWP			20		MHz
Slew Rate (Note 3)	SR			8		V/µs
GATE DRIVERS						
Upper Gate Source Impedance	$R_{UG-SRCh}$	V_{CC} = 12V; I = 50mA		2.1		Ω
Upper Gate Sink Impedance	$R_{UG-SNKh}$	V_{CC} = 12V; I = 50mA		1.6		Ω
Lower Gate Source Impedance	$R_{LG-SRCh}$	V_{CC} = 12V; I = 50mA		1.4		Ω
Lower Gate Sink Impedance	$R_{LG-SNKh}$	V_{CC} = 12V; I = 50mA		1.0		Ω
Upper Gate Source Impedance	$R_{UG-SRCl}$	V_{CC} = 5V; I = 50mA		2.4		Ω

Electrical Specifications Test Conditions: V_{CC} = 12V, T_J = 0 to +85°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Upper Gate Sink Impedance	$R_{UG-SNKI}$	V_{CC} = 5V; I = 50mA		1.7		Ω
Lower Gate Source Impedance	$R_{LG-SRCI}$	V_{CC} = 5V; I = 50mA		1.5		Ω
Lower Gate Sink Impedance	$R_{LG-SNKI}$	V_{CC} = 5V; I = 50mA		1.1		Ω
PROTECTION/DISABLE						
OCSET Current Source	I_{OCSET}	LGATE/OCSET = 0V	9	10	11	µA
Enable Threshold (COMP/EN pin)	V_{ENABLE}		0.683	0.700	0.717	V
VOS Rising Trip (PGOOD OV; +10%)			0.868	0.880	0.888	V
VOS Rising Trip (PGOOD OV) hysteresis				16		mV
VOS Falling Trip (PGOOD UV; -10%)			0.708	0.720	0.732	V
VOS Falling Trip (PGOOD UV) hysteresis				16		mV
VOS Rising Threshold (OV; +25%)			0.980	1.000	1.020	V
VOS Falling Threshold (UV; -25%)			0.580	0.600	0.620	V
VOS Threshold (OV; 50% of V_{OUT})			0.380	0.400	0.410	V
VOS Bias Current		VOS = 0.25V	-1500	-250	-100	nA
PGOOD		I_{PGOOD} = 4mA	0.10	0.18	0.30	V

Functional Pin Description

VCC (Pin 6)

This pin provides the bias supply for the ISL6341, ISL6341A, ISL6341B, as well as the lower MOSFET's gate. An internal regulator will supply bias as VCC rises above 5V, but the LGATE/OCSET will still be sourced by VCC. Connect a well-decoupled 5V to 12V supply to this pin.

FB (Pin 8)

This pin is the inverting input of the internal error amplifier. Use FB, in combination with the COMP/EN pin, to compensate the voltage-control feedback loop of the converter. A resistor divider from V_{OUT} to FB to GND is used to set the regulation voltage.

VOS (Pin 9)

This input pin monitors the regulator output for OV and UV protection, and PGOOD (OV and UV). Connect a resistor divider from V_{OUT} to VOS to GND, with the same ratio as the FB resistor divider. It is usually not recommended to share one divider for both FB and VOS; the response to a fault may not be as quick or robust. There is a small pull-up bias current on the pin; if the VOS pin is not connected, the OV protection would be tripped to protect the load.

GND (Pin 5)

This pin represents the signal and power ground for the IC. This pin is the high current connection, and should be tied to the ground island/plane through the lowest impedance connection available. The metal pad under the package should also be connected to the GND plane for thermal conductivity, but does not conduct any current.

PHASE (Pin 2)

Connect this pin to the source of the upper MOSFET, and the drain of the lower MOSFET. It is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for overcurrent protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

UGATE (Pin 3)

Connect this pin to the gate of upper MOSFET; it provides the PWM-controlled gate drive. It is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

BOOT (Pin 1)

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive an N-Channel MOSFET (equal to V_{GD} minus the BOOT diode voltage drop), with respect to PHASE.

COMP/EN (Pin 7)

This is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. Use COMP/EN, in combination with the FB pin, to compensate the voltage-control feedback loop of the converter.

Pulling COMP/EN low (V_{ENABLE} = 0.7V nominal) will disable the controller, which causes the oscillator to stop, the LGATE and UGATE outputs to be held low, and the soft-start circuitry to re-arm. The external pull-down device will initially need to overcome up to 5mA of COMP/EN output current. However, once the IC is disabled, the COMP output will also be disabled, so only a 20µA current source will continue to draw current.

When the pull-down device is released, the COMP/EN pin will start to rise, at a rate determined by the 20µA charging up the capacitance on the COMP/EN pin. When the COMP/EN pin rises above the V_{ENABLE} trip point, the ISL6341, ISL6341A, ISL6341B will begin a new initialization and soft-start cycle.

LGATE/OCSET (Pin 4)

Connect this pin to the gate of the lower MOSFET; it provides the PWM-controlled gate drive (from V_{CC}). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

During a short period of time following Power-On Reset (POR) or shut-down release, this pin is also used to determine the overcurrent threshold of the converter. Connect a resistor (R_{OCSET}) from this pin to GND. See "Overcurrent Protection (OCP)" on page 7 for equations. An overcurrent trip latches off the output, requiring cycling V_{CC} off and on, or by toggling COMP/EN. Some of the text describing the LGATE function may leave off the OCSET part of the name when it is not relevant to the discussion.

PGOOD (Pin 10)

This output is an open-drain pull-down device that reflects the state of the PGOOD comparators. An external pull-up resistor should be connected to a supply ≤6V. The output will be held low through the soft-start ramp, and is allowed to go high at the end of soft-start, if the VOS voltage is within its window. The PGOOD window is tighter than the OV or UV protection window, so it may give an early warning of a problem. The PGOOD does respond directly to an OCP condition, but may also go low if V_{OUT} drops low enough before an OCP trip.

Functional Description

TABLE 1. SUMMARY OF FEATURE DIFFERENCES

PART NUMBER	f_{SW}	MAX DUTY CYCLE	OCP (OVERCURRENT PROTECTION)
ISL6341	300kHz	85%	Latch off; toggle POR or COMP/EN to restart
ISL6341A	600kHz	75%	"Hiccup" mode (infinite retries)
ISL6341B	600kHz	75%	Latch off; toggle POR or COMP/EN to restart

Initialization (POR and OCP sampling)

Figure 1 shows a simplified timing diagram. The Power-On-Reset (POR) function continually monitors the bias voltage at the VCC pin. Once the rising POR threshold is exceeded (V_{POR} = 4.3V nominal), the POR function initiates the Overcurrent Protection (OCP) sample and hold operation (while COMP/EN is ~1V). When the sampling is complete, V_{OUT} begins the soft-start ramp.

If the COMP/EN pin is held low during power-up, that will just delay the initialization until it is released and the COMP/EN voltage is above the V_{ENABLE} trip point.

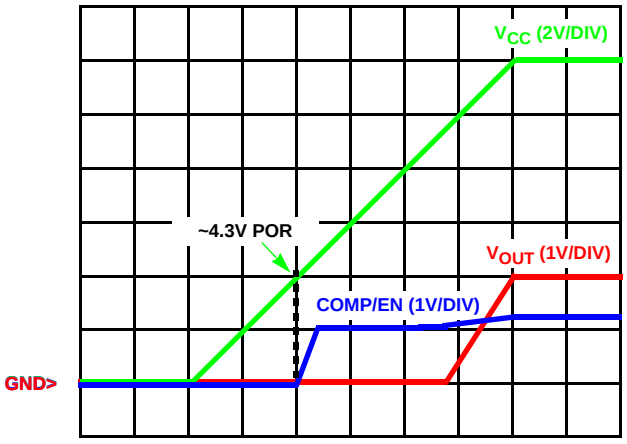


FIGURE 1. POR AND SOFT-START OPERATION

Figure 2 shows a typical power-up sequence in more detail. The initialization starts at t0, when either V_{CC} rises above V_{POR}, or the COMP/EN pin is released (after POR). The COMP/EN will be pulled up by an internal 20µA current source, but the timing will not begin until the COMP/EN exceeds the V_{ENABLE} trip point (at t1). The external capacitance of the disabling device, as well as the compensation capacitors, will determine how quickly the 20µA current source will charge the COMP/EN pin. With typical values, it should add a small delay compared to the soft-start times. The COMP/EN will continue to ramp to ~1V.

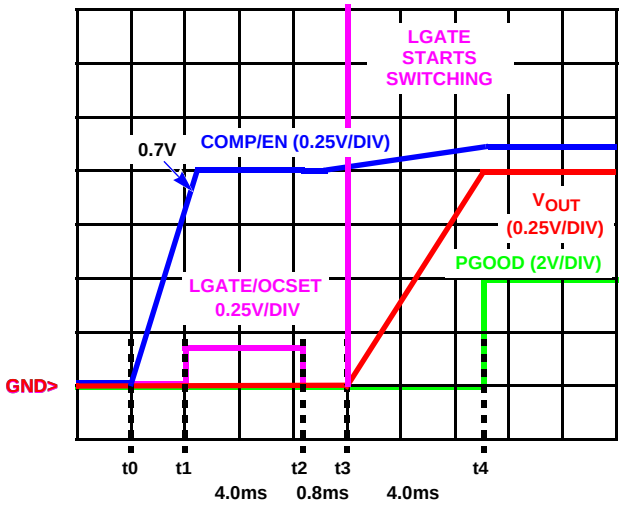


FIGURE 2. LGATE/OCSET AND SOFT-START OPERATION

From t1, there is a nominal 4ms delay, which allows the VCC pin to rise. At the same time, the LGATE/OCSET pin is initialized by disabling the LGATE driver and drawing I_{OCSET} (nominal 10µA) through R_{OCSET}. This sets up a voltage that will represent the OCSET trip point for the OCP sample and hold operation. The sample and hold uses a digital counter and DAC (to save the voltage so the stored value does not degrade) for as long as the V_{CC} is above V_{POR}. See "Overcurrent Protection (OCP)" on page 7 for more details on the equations and variables. Upon the completion of sample and hold at t2, the soft-start operation is initiated (around 0.8ms delay to t3),

and then around 4ms for the output voltage to ramp up (0% to 100%) between t3 and t4. The PGOOD output is allowed to go high at t4 if VOS (and thus V_{OUT}) is within the PGOOD window.

Soft-Start and Pre-Biased Outputs

Functionally, the soft-start internally ramps the reference on the non-inverting terminal of the error amp from zero to 0.8V in a nominal 4ms. The output voltage will thus follow the ramp, from zero to final value, in the same 4ms. The ramp is created digitally, so there will be small discrete steps. There is no simple way to change this ramp rate externally, as it is fixed by the 300kHz (or 600kHz) switching frequency (and the ramp and delay time is the same for both frequencies).

After an initialization period (t2 to t3), the error amplifier (COMP/EN pin) is enabled, and begins to regulate the converter's output voltage during soft-start. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitors. When the internally generated soft-start voltage exceeds the reference voltage (0.8V), the soft-start is complete, and the output should be in regulation at the expected voltage. This method provides a rapid and controlled output voltage rise; there is no large in-rush current charging the output capacitors. The entire start-up sequence from POR typically takes 9ms; 5ms for the delay and OCP sample, and 4ms for the soft-start ramp.

Figure 3 shows the normal V_{OUT} curve in blue; initialization begins at t0, and the output ramps between t1 and t2. If the output is pre-biased to a voltage less than the expected value (as shown by the magenta curve), the ISL6341, ISL6341A, ISL6341B will detect that condition. Neither MOSFET will turn-on until the soft-start ramp voltage exceeds the output; V_{OUT} starts seamlessly ramping from there.

There is a restriction for the pre-bias case; if the pre-biased V_{OUT} is greater than V_{GD}, then the boot cap may get discharged, and will not be able to restart. For example, if V_{IN} = 12V, V_{OUT} = 8V and prebiased to 6V, and V_{GD} is only 5V, then the voltage left on the boot cap (to UGATE) will not be able to turn on the upper FET. The simple solution here is to use the 12V for V_{GD}. The guideline is to make V_{GD} - diode - Vth upper FET > V_{OUT} to prevent this condition.

If the output is pre-biased to a voltage above the expected value (as in the red curve), neither MOSFET will turn-on until the end of the soft-start, at which time it will pull the output voltage quickly down to the final value. Any resistive load connected to the output will help pull-down the voltage (at the RC rate of the R of the load and the C of the output capacitance).

One exception to the over-charged case is if the pre-bias is high enough to trip OV protection (>1V on VOS); then LGATE will pulse to try to pull V_{OUT} lower. The IC will remain latched in this mode until V_{CC} power is toggled.

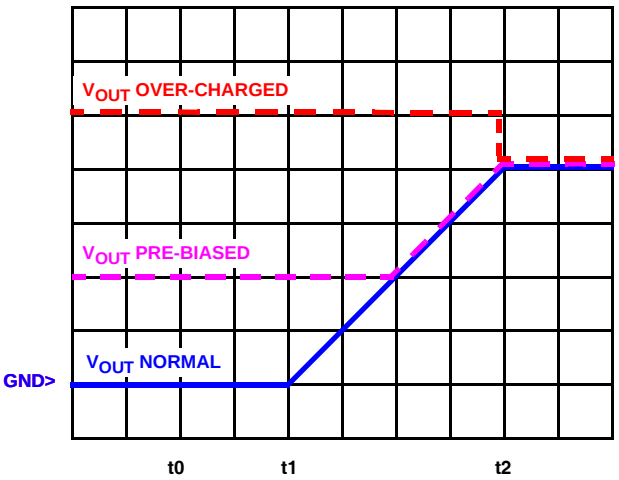


FIGURE 3. SOFT-START WITH PRE-BIAS

If the V_{IN} to the upper MOSFET drain (or the V_{GD} voltage to the boot diode) is from a different supply that comes up after V_{CC}, the soft-start would start its cycle, but with no output voltage ramp. Once the undervoltage protection is enabled (at the end of the soft-start ramp), the output will latch off. Therefore, for normal operation, V_{IN} (and V_{GD}) must be high enough before or with V_{CC}. If this is not possible, then the alternative is add sequencing logic to the COMP/EN pin to delay the soft-start until the V_{IN} (and V_{GD}) supply is ready (see "Input Voltage Considerations" on page 11).

If the IC is disabled after soft-start (by pulling COMP/EN pin low), and then enabled (by releasing the COMP/EN pin), then the full initialization (including a new OCP sample) will take place.

If the output is shorted to GND during soft-start, the OCP will handle it, as described in the next section.

Overcurrent Protection (OCP)

The overcurrent function protects the converter from a shorted output by using the lower MOSFET's ON-resistance, $r_{DS(ON)}$, to monitor the current. A resistor (R_{OCSET}) programs the overcurrent trip level (see "Typical Application" diagram on page 3). This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

Following POR and release of COMP/EN, the ISL6341, ISL6341A, ISL6341B initiates the Overcurrent Protection sample and hold operation. The LGATE driver is disabled to allow an internal 10µA current source to develop a voltage across R_{OCSET}. The ISL6341, ISL6341A, ISL6341B samples this voltage (which is referenced to the GND pin) at the LGATE/OCSET pin, and holds it in a counter and DAC combination. This sampled voltage is held internally as the Overcurrent Set Point, for as long as power is applied, or until a new sample is taken after coming out of a COMP/EN shut-down.

The actual monitoring of the lower MOSFET's ON-resistance starts 200ns (nominal) after the edge of the internal PWM logic signal (that creates the rising external LGATE signal). This is done to allow the gate transition noise and ringing on the PHASE pin to settle out before monitoring. The monitoring ends when the internal PWM edge (and thus LGATE) goes low. The OCP can be detected anywhere within the above window.

To allow sufficient time to detect OCP, the regulator will limit the maximum UGATE duty cycle to ~85% at 300kHz (~75% at 600kHz); there will always be an LGATE pulse of at least 300ns. This minimum width will also act as a boot-refresh function. If the boot capacitor loses any charge while UGATE is high, it will be refreshed each cycle while LGATE is high.

The ISL6341, ISL6341B and ISL6341A share most of the detection circuitry; the main difference between them is what happens after detection.

ISL6341, ISL6341B

When overcurrent is detected (while LGATE is high), the logic will disable UGATE, and leave LGATE high until the current drops to 1/2 of its programmed OCP value. This may take several clock cycles, and it keeps the current from building up too high. Once the current is low enough, UGATE will go high on the next PWM cycle, and OCP will be monitored when LGATE goes high. If OCP trips a 2nd time, it will again wait until the current drops. If it trips again the 3rd time, it will latch off the output (LGATE and UGATE low). If there is no OCP trip on one of the retries, then the trip-counter resets to zero, and three new consecutive cycles are required to latch off.

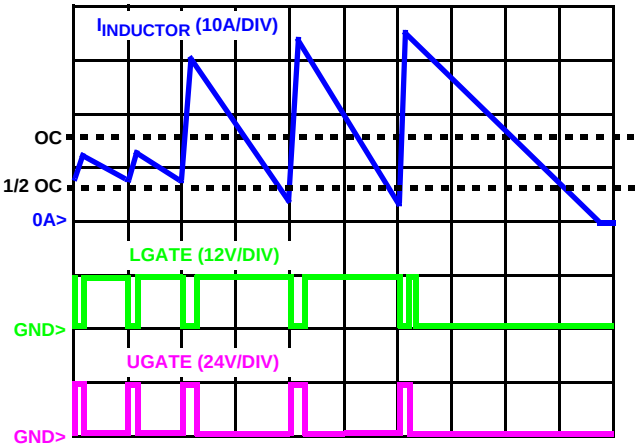


FIGURE 4. OCP TIMING (ISL6341, ISL6341B ONLY)

Figure 4 shows a typical waveform for the ISL6341, ISL6341B, where the normal inductor current is around 10A, and the OCP trip is 16A. This is just an illustration; the actual shape of the waveforms depends on the component values, as well as the characteristics of the load and the short. On the third trip, the gate drivers stop switching, and the current goes to zero. To recover from this latched off condition, the user must toggle V_{CC} (power-down and up) for a new POR, or toggle COMP/EN pin to restart (either includes initialization and soft-start).

As the output inductor current rises and falls, the output voltage is also affected. Note that in extreme cases during the three consecutive trips, the UV may actually trip before the OCP. The IC provides protection in either case, but perhaps not quite at the programmed current. An OCP trip can be reset by toggling either POR or COMP/EN, but a UV trip is only reset by toggling POR. See Table 2 for the protection summary.

Starting up into a shorted load will be handled the same way; but the waveforms may look different, since the output is not yet at its final value. OCP is always enabled during soft-start (UV is not); it will need the three consecutive trips to latch off.

ISL6341A

Figure 5 shows the same conditions for the ISL6341A. For this version, when overcurrent is first detected (while LGATE is high), the logic will shut off the output (LGATE and UGATE both go low), and the current goes to zero.

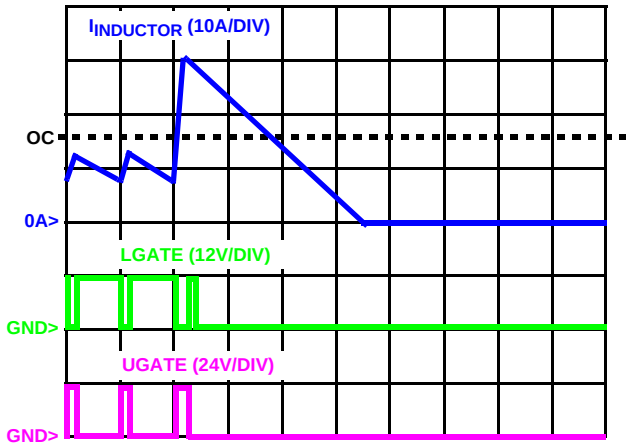


FIGURE 5. OCP TIMING (ISL6341A ONLY)

It will then go into a "hiccup" mode of infinite retries. After two dummy soft-start time-outs, a real soft-start will begin. If the short is still there, it will trip during the soft-start ramp, and will start another retry cycle. Once the short is removed, the next real soft-start will be successful, and normal operation can continue.

Figure 6 shows the ISL6341A output response during a retry of an output shorted to GND. At time t0, the output has been turned off, due to sensing an overcurrent condition. There are two internal soft-start delay cycles (t1 and t2) to allow the MOSFETs to cool down, to keep the average power dissipation in retry at an acceptable level. At time t2, the output starts a normal soft-start cycle, and the output tries to ramp. If the short is still applied, and the current reaches the OCSET trip point any time during soft-start ramp period, the output will shut off and return to time t0 for another delay cycle. The retry period is thus two dummy soft-start cycles plus one variable one, which depends on how long it takes to trip the sensor each time. Figure 6 shows an example where the output gets about half-way up before shutting down; therefore, the retry (or hiccup) time will be around 12ms. The

minimum should be nominally 9.6ms and the maximum 14.4ms. If the short condition is finally removed, the output should ramp up normally on the next t2 cycle.

Starting up into a shorted load looks the same as a retry into that same shorted load. In both cases, OCP is always enabled during soft-start; once it trips, it will go into retry (hiccup) mode. The retry cycle will always have two dummy time-outs, plus whatever fraction of the real soft-start time passes before the detection and shut-off; at that point, the logic immediately starts a new two dummy cycle time-out.

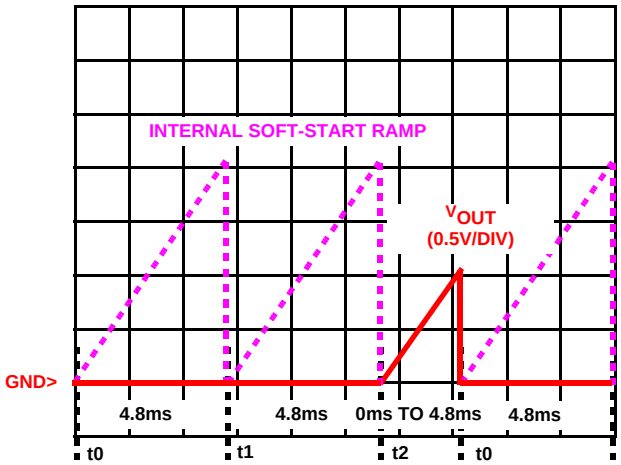


FIGURE 6. OCP RETRY OPERATION (ISL6341A ONLY)

OVERCURRENT EQUATIONS

For both the ISL6341, ISL6341B and ISL6341A, the overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by Equation 1:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 1)}$$

where I_{OCSET} is the internal OCSET current source (10µA typical). The OC trip point varies in a system mainly due to the MOSFET's $r_{DS(ON)}$ variations (over process, current and temperature). To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from Equation 1 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see "Output Inductor Selection" on page 14.

The range of allowable voltages detected (I_{OCSET}*R_{OCSET}) is 0mV to 550mV; but the practical range for typical MOSFETs is smaller. If the voltage drop across R_{OCSET} is set too low, that can cause almost continuous OCP tripping and latch-off. It would also be very sensitive to system noise and in-rush current spikes, so it should be avoided. The maximum setting is 550mV, but most of the recommended MOSFETs for the ISL6341, ISL6341A, ISL6341B are not expected to handle the power of the maximum trip point. Any voltage setting above 600mV will clamp to the maximum setting. No resistor at all should give the clamped maximum value (unless the loading on the LGATE prevents charging the node fully). However, a resistor (>60k) is recommended; there is no low-voltage clamp on LGATE, so it could rise to over 3V and turn-on for 4ms during the sampling; that could discharge a pre-biased output.

There is no way to disable the OCP, but setting it to the maximum value may be far enough above the normal expected range.

Note that conditions during power-up may look different than normal operation. For example, during power-up in a 12V system, the IC starts operation just above 4V; if the supply ramp is slow, the soft-start ramp might be over well before 12V is reached. So with lower gate drive voltages, the $r_{DS(ON)}$ of the MOSFETs will be higher during power-up, effectively lowering the OCP trip. In addition, the ripple current will likely be different at lower input voltage.

Another factor is the digital nature of the soft-start ramp. On each discrete voltage step, there is in effect a small load transient and a current spike to charge the output capacitors. The height of the current spike is not controlled; it is affected by the step size of the output, the value of the output capacitors, as well as the IC error amp compensation. So it is possible to trip the overcurrent with in-rush current, in addition to the normal load and ripple considerations.

OCP is always enabled during soft-start, so there is protection starting up into a shorted load.

Undervoltage Protection

The output is protected against undervoltage conditions by monitoring the VOS pin. An external resistor divider (similar ratio to the one on the FB pin) makes the voltage equal the 0.8V internal reference under normal operation. If the output goes too low (25% below 0.8V = 0.6V nominal on VOS), the output will latch off, with UGATE and LGATE both forced low. This requires toggling V_{CC} (power-down and up) to restart (toggling COMP/EN will NOT restart it). The UV protection is not enabled until the end of the soft-start ramp (as shown in Figure 2).

Figure 7 shows a case where V_{OUT} (and thus VOS) is pulled down to the 75% point; both gate drivers stop switching, and the V_{OUT} is pulled low by the disturbance, as well as the load, at a rate determine by the conditions, and the output components.

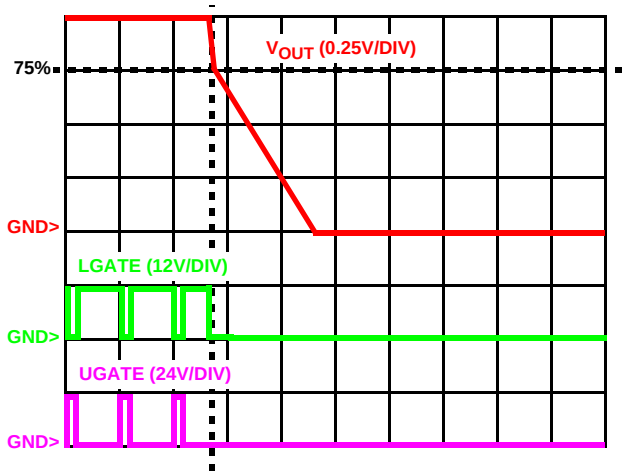


FIGURE 7. UNDERVOLTAGE PROTECTION

Overvoltage Protection

The output is protected against overvoltage conditions by monitoring the VOS pin, similar to undervoltage. If the output goes too high (25% above 0.8V = 1.0V nominal on VOS), the output will latch off. As shown in Figure 8, UGATE will be forced low, but LGATE will be forced high (to try to pull-down the output) until the output drops to 1/2 of the normal voltage (50% of 0.8V = 0.4V nominal on VOS).

Overvoltage latch-off requires toggling V_{CC} (power-down and up) to restart (toggling COMP/EN will NOT restart it). The OV protection is not enabled until the rising V_{CC} POR trip point is exceeded.

If the VOS pin is disconnected, a small bias current on-chip will force an overvoltage condition.

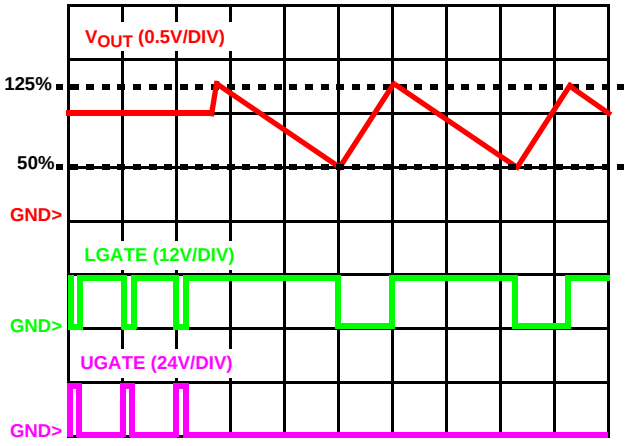


FIGURE 8. OVERVOLTAGE PROTECTION

PGOOD

The PGOOD function output monitors the output voltage using the same VOS pin and resistor divider of the undervoltage and overvoltage protection, but with separate comparators for each. The rising OV trip point (10% above 0.8V = 0.88V nominal on VOS) and the falling UV trip point (10% below 0.8V = 0.72V nominal on VOS) will trip sooner than the protection, in order to give an early warning to a possible problem. The response time of the comparators should be less than 1µs; the separate VOS input is not slowed down by the compensation on the FB pin. If a fast or robust response is not required, it may be possible to connect the VOS pin to the FB pin, in order to share the resistor divider. If the VOS pin is accidentally disconnected, a small bias current on-chip will force an overvoltage condition.

Figure 9 shows how the PGOOD output responds to a ramp that trips in each direction (without reaching either protection trip point at ±25%); PGOOD is valid (high) as long as V_{OUT} (and thus VOS) is within the ±10% window.

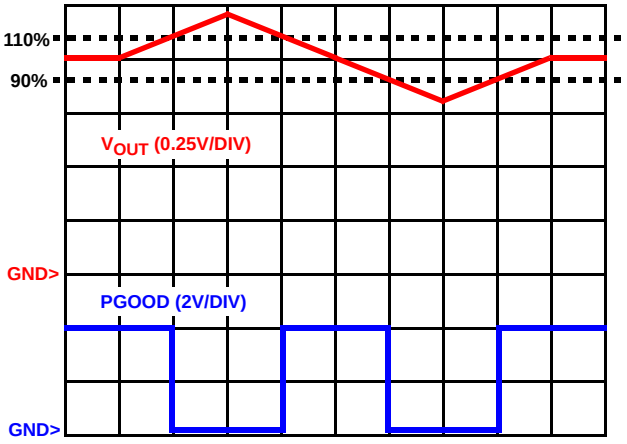


FIGURE 9. PGOOD UNDERVOLTAGE AND OVERVOLTAGE

The PGOOD output is an open-drain pull-down NMOS device; it can deliver 4.0mA of sink current at 0.3V when power is NOT GOOD. A pull-up resistor to an external supply voltage sets the high level voltage when power is GOOD. The supply should be ≤6.0V, and is usually the one that powers the logic monitoring the PGOOD output. If PGOOD function is not used, the PGOOD pin can be left floating.

The PGOOD pin will be held low once V_{CC} is above the rising POR trip point, and during soft-start (but if the PGOOD supply is up before or with V_{CC}, it may be pulled high initially until the logic has enough voltage to turn on the output). Once the soft-start ramp is done (V_{OUT}, VOS and FB should each be at 100% of their final value), the PGOOD pin will be allowed to go high, if the output voltage is within the expected window. There is no additional delay after soft-start is done.

Note that the overcurrent protection does directly affect the PGOOD output, before the output voltage monitoring would sense when V_{OUT} drops 10%. The overvoltage and undervoltage protection circuits don't directly effect PGOOD, but since the PGOOD UV and OV windows are tighter, the PGOOD output should already be low by the time either protection is tripped.

TABLE 2. PROTECTION SUMMARY

PROTECTION	ACTION TAKEN	ENABLED AFTER	RESET BY
OCP (41/41B)	V_{OUT} latches off; LGATE and UGATE low.	POR or COMP/EN	POR or COMP/EN
OCP (41A)	Infinite retries; wait ~10ms, and try a new Soft-Start ramp.	POR or COMP/EN	Not Applicable
UVP (-25%)	V_{OUT} latches off; LGATE and UGATE low.	after SS ramp	POR
OVP (+25%)	V_{OUT} latches off; UGATE low; LGATE goes low and high to keep V_{OUT} within 50% and 125% of nominal. VOS pin open will trigger OV.	POR	POR
PGOOD (**UV;** -10%)	PGOOD goes low if VOS is 10% too low.	after SS ramp	POR or COMP/EN
PGOOD (**OV;** +10%)	PGOOD goes low if VOS is 10% too high.	after SS ramp	POR or COMP/EN
PGOOD (**OCP**)	PGOOD goes low if OCP trips	after SS ramp	POR or COMP/EN or good SS ramp

Switching Frequency

The switching frequency is a fixed 300kHz for the ISL6341, and 600kHz for the ISL6341A, ISL6341B. It cannot be adjusted externally, and the various soft-start delays and ramps are fixed at the same times for either frequency.

Output Voltage Selection

The output voltage can be programmed to any level between the 0.8V internal reference, up to the V_{IN} supply, with the 85% duty cycle restriction for the ISL6341 (75% for the ISL6341A, ISL6341B). Additional duty cycle margin due to the $r_{DS(ON)}$ drop across the upper FET at maximum load needs to be factored in as well.

An external resistor divider is used to scale the output voltage relative to the internal reference voltage, and feed it back to the inverting input of the error amp. See the "Typical Application" schematic on page 3 for more detail; R_S is the upper resistor; R_{OFFSET} (shortened to R_O below) is the lower one. The recommended value for R_S is 1kΩ to 5kΩ (±1% for accuracy) and then R_{OFFSET} is chosen according to Equation 2. Since R_S is part of the compensation circuit (see "Feedback Compensation" on page 12), it is often easier to change R_{OFFSET} to change the output voltage; that way the compensation calculations do not need to be repeated. If V_{OUT} = 0.8V, then R_{OFFSET} can be left open. Output voltages less than 0.8V are not available.

$$V_{OUT} = 0.8V \bullet \frac{(R_S + R_O)}{R_O} \qquad \text{(EQ. 2)}$$

$$R_O = \frac{R_S \bullet 0.8V}{V_{OUT} - 0.8V}$$

The VOS pin is expected to see the same ratio for its resistor divider; R_{VOS1} should also be chosen in the 1kΩ to 5kΩ (±1% for accuracy) range. To simplify the BOM, R_{VOS1} should match R_S, and R_{VOS2} should match R_{OFFSET}.

Input Voltage Considerations

The "Typical Application" diagram on page 3 shows a standard configuration where V_{CC} is 5V to 12V, which includes the standard 5V (±10%) or 12V (±20%) power supply ranges. The gate drivers use the V_{CC} voltage for LGATE, and V_{GD} (also 5V to 12V) for BOOT/UGATE. There is an internal 5V regulator for bias.

The V_{IN} to the upper MOSFET can share the same supply as V_{CC}, but can also run off a separate supply or other sources, such as outputs of other regulators. If V_{CC} powers up first, and the V_{IN} or V_{GD} are not present by the time the initialization is done, then undervoltage will trip at the end of soft-start (and will not recover without toggling V_{CC}; toggling COMP/EN will not restart it). Therefore, either the supplies must be turned on in the proper order (together, or V_{CC} last), or the COMP/EN pin should be used to disable V_{OUT} until all supplies are ready.

Figure 10 shows a simple sequencer for this situation. If V_{CC} powers up first, Q_1 will be off and R_3 pulling to V_{CC} will turn Q_2 on, keeping the ISL6341, ISL6341A, ISL6341B in shut-down. When V_{IN} turns on, the resistor divider R_1 and R_2 determines when Q_1 turns on, which will turn off Q_2, and release the shut-down. If V_{IN} powers up first, Q_1 will be on, turning Q_2 off; so the ISL6341, ISL6341A, ISL6341B will start-up as soon as V_{CC} comes up. The V_{ENABLE} trip point is 0.7V nominal, so a wide variety of NFET's or NPN's or even some logic IC's can be used as Q_1 or Q_2; but Q_2 must be low leakage when off (open-drain or open-collector) so as not to interfere with the COMP output. Q_2 should also be placed near the COMP/EN pin.

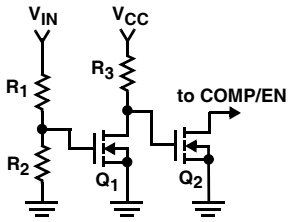


FIGURE 10. SEQUENCER CIRCUIT

The V_{IN} range can be as low as ~1.5V (for V_{OUT} as low as the 0.8V reference). It can be as high as 20V (for V_{OUT} just below V_{IN}, limited by the maximum duty cycle). There are some restrictions for running high V_{IN} voltage.

The first consideration for high V_{IN} is the maximum BOOT voltage of 36V. The V_{IN} (as seen on PHASE) plus V_{GD} (boot voltage - minus the diode drop), plus any ringing (or other transients) on the BOOT pin must be less than 36V. If V_{IN} is 20V, that limits V_{GD} plus ringing to 16V.

The second consideration is the maximum voltage ratings for V_{CC} and BOOT-PHASE (for V_{GD}); both are set at 15V. If V_{IN} is above the maximum operating range for V_{CC} of 14.4V, then both V_{CC} and V_{GD} need to be supplied separately. They can be derived from V_{IN} (using a linear regulator or equivalent), or they can be independent. In either case, they must satisfy the power supply sequencing requirements noted earlier (either power-up in the proper order, or use a sequencer to disable the output until they are all ready).

The third consideration for high V_{IN} is duty cycle. Very low duty cycles (such as 20V in to 1.0V out, for 5% duty cycle) require component selection compatible with that choice (such as low $r_{DS(ON)}$ lower MOSFET, a good LC output filter, and compensation values to match). At the other extreme (for example, 20V in to 12V out), the upper MOSFET needs to be lower $r_{DS(ON)}$. There is also the maximum duty cycle restriction. In all cases, the input and output capacitors and both MOSFETs must be rated for the voltages present.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

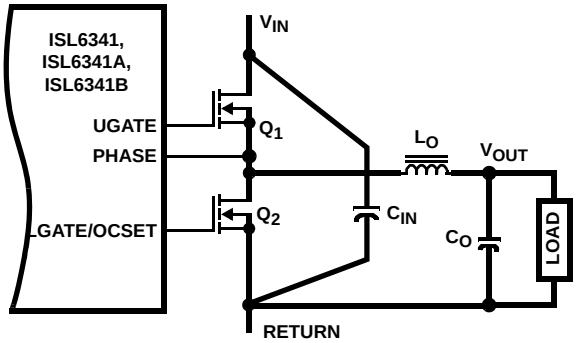


FIGURE 11. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 11 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. The components shown should be located as close together as possible. Please note that the capacitors C_{IN} and C_O may each represent numerous physical capacitors. For best results, locate the ISL6341, ISL6341A, ISL6341B within 1 inch of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFET gate and source connections from the ISL6341, ISL6341A, ISL6341B must be sized to handle up to 2A peak current.

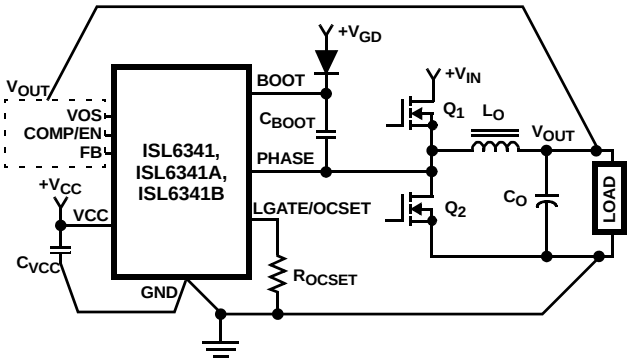


FIGURE 12. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Figure 12 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins. Locate the resistor, R_{OSCET} close to the LGATE/OCSET pin because the internal current source is only 10µA. Minimize any leakage current paths on the COMP/EN pin. All components used for feedback compensation and VOS resistor divider (inside the dotted box) should be located as close to the IC as practical. Near the load, pick a point V_{OUT} that will be the regulation center; run a single unloaded narrow trace from there to the compensation components. The same trace can also be used for VOS divider.

Feedback Compensation

This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended, as shown in the top part of Figure 13.

Figure 13 also highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable to the ISL6341, ISL6341A, ISL6341B circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, V_{REF}. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the channel inductance and its DCR, while C and E represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot E} \qquad \text{(EQ. 3)}$$

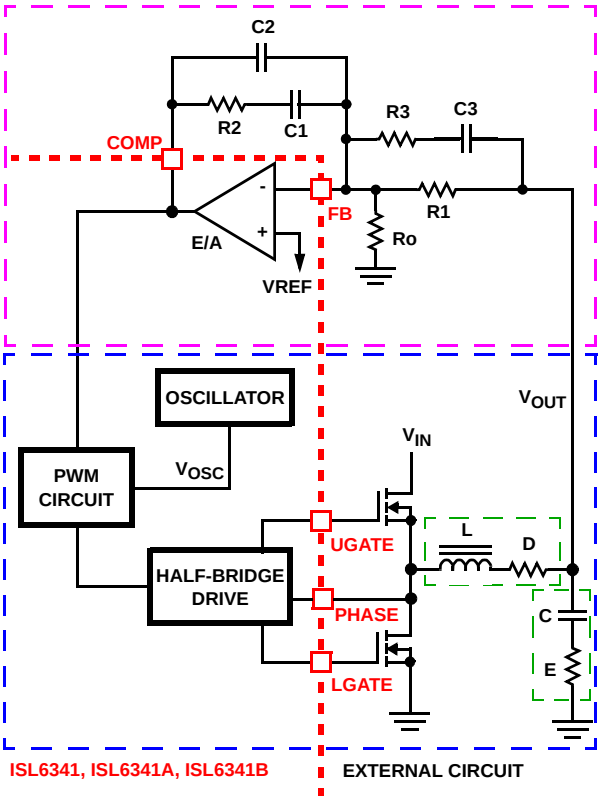


FIGURE 13. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The compensation network consists of the error amplifier (internal to the ISL6341, ISL6341A, ISL6341B) and the external R_1 to R_3, C_1 to C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of f_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 13. Use the following guidelines for locating the poles and zeros of the compensation network:

4. Select a value for R_1 (1kΩ to 5kΩ, typically). Calculate the value for R_2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin (R_0 in Figure 13), the design procedure can be followed as presented.

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \quad \text{(EQ. 4)}$$

5. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \quad \text{(EQ. 5)}$$

6. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \quad \text{(EQ. 6)}$$

7. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below f_{SW} (typically, 0.5 to 1.0 times f_{SW}). f_{SW} represents the switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{f_{SW}}{F_{LC}} - 1} \qquad C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot f_{SW}} \quad \text{(EQ. 7)}$$

It is recommended that a mathematical model be used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j \quad \text{(EQ. 8)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \text{(EQ. 9)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

Figure 14 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 14 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

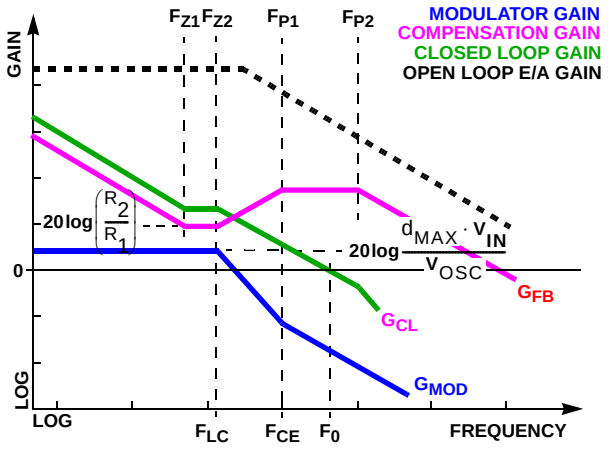


FIGURE 14. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, f_{SW}.

This is just one method to calculate compensation components; there are variations of the compensation break frequency equations. The error amp is similar to that on other Intersil regulators, so existing tools can be used here as well. Special consideration is needed if the size of a ceramic output capacitance in parallel with bulk capacitors gets too large; the calculation needs to model them both separately (attempting to combine two different capacitors types into one composite component model may not work properly; a special tool may be needed; contact your local Intersil person for assistance).

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 10:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fsw \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 10)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6341, ISL6341A, ISL6341B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 11 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 11)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check Equation 11 at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6341, ISL6341A, ISL6341B requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see Equation 12). Equation 12 assumes linear voltage-current transitions and does not adequately model power loss due to the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6341, ISL6341A, ISL6341B and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Losses while Sourcing Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Losses while Sinking Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D \quad \text{(EQ. 12)}$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the combined switch ON and OFF time, and
f_{SW} is the switching frequency.

When operating with a 12V power supply for V_{CC} (or down to a minimum supply voltage of 4.5V), a wide variety of N-MOSFETs can be used. Check the absolute maximum V_{GS} rating for both MOSFETs; it needs to be above the highest V_{CC} voltage allowed in the system; that usually means a 20V V_{GS} rating (which typically correlates with a 30V V_{DS} maximum rating). Low threshold transistors (around 1V or below) are not recommended, for the reasons explained in the following paragraph.

For 5V only operation, given the reduced available gate bias voltage (5V), logic-level transistors should be used for both N-MOSFETs. Look for $r_{DS(ON)}$ ratings at 4.5V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the ISL6341, ISL6341A, ISL6341B may be circumvented by these MOSFETs if they have large parasitic impedences and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50ns or so.

BOOTSTRAP Considerations

Figure 15 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{GD}. For convenience, V_{GD} usually shares the V_{IN} or V_{CC} supply; it can be any voltage in the 5V to 12V range. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. The supply is refreshed to a voltage of V_{GD} less the boot diode drop (V_D) each time the lower MOSFET, Q_2, turns on. Check that the voltage rating of the capacitor is above the maximum V_{CC} voltage in the system; a 16V rating should be sufficient for a 12V system. A value of 0.1µF is typical for many systems driving single MOSFETs.

If V_{CC} is 12V, but V_{IN} is lower (such as 5V), then another option is to connect the BOOT pin to 12V, and remove the BOOT cap (although, you may want to add a local cap from BOOT to GND). This will make the UGATE V_{GS} voltage equal to (12V - 5V = 7V). That should be high enough to drive most MOSFETs, and low enough to improve the efficiency slightly. This also saves a boot diode (and capacitor).

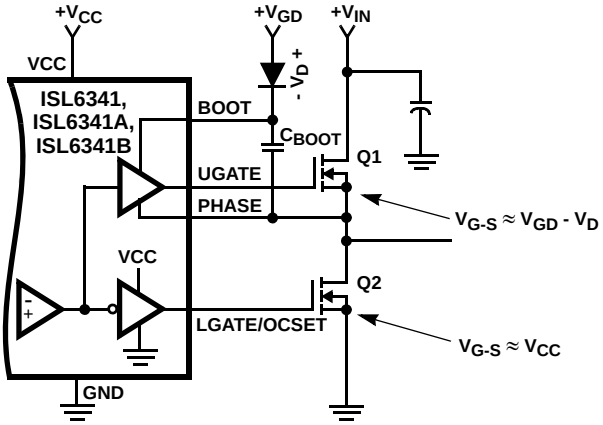
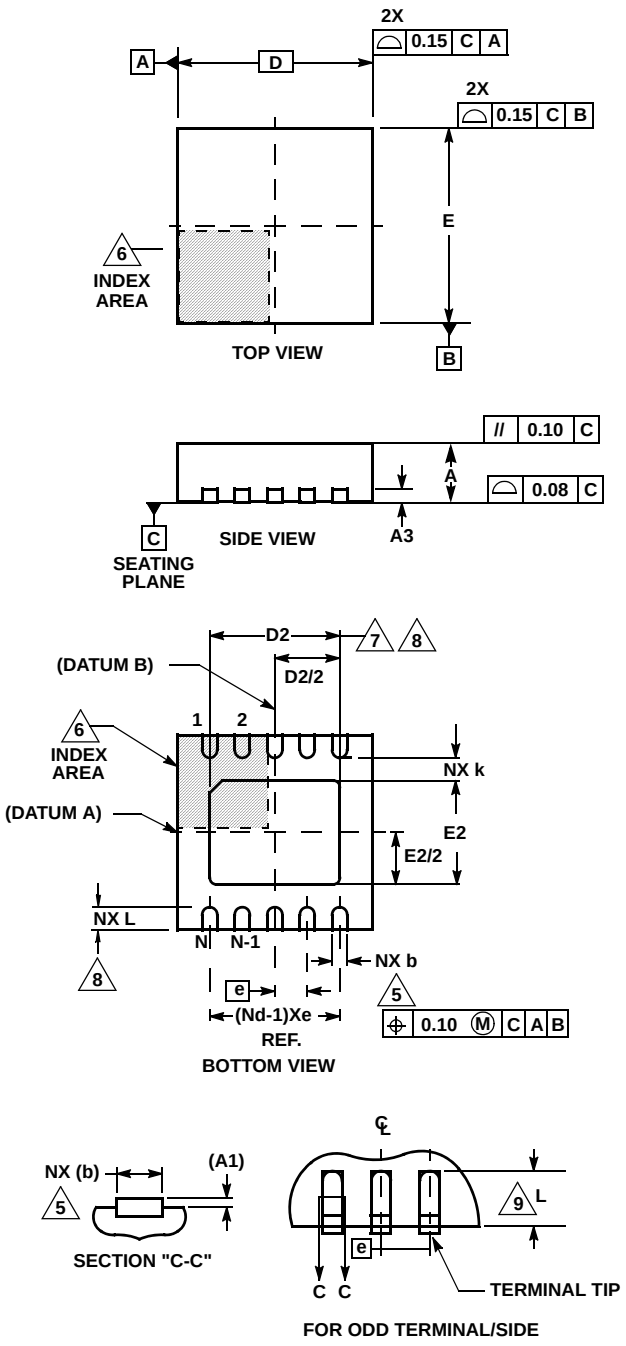


FIGURE 15. UPPER GATE DRIVE BOOTSTRAP

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3B

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.23	2.38	2.48	7, 8
E		3.00 BSC		-
E2	1.49	1.64	1.74	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		10		2
Nd		5		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.