Boost Regulator with Integrated Schottky and Input Disconnect Switch

The ISL97701 represents a high efficiency, boost converter with integrated boost FET, boost diode and input disconnect FET.

With an input voltage of 2.3V to 5.5V the ISL97701 has an output capability of up to 50mA at 18V using integrated 500mA switches. Efficiencies are up to 87%. The integrated protection FET is used to disconnect the boost inductor from the input supply whenever an output fault condition is detected, or when the device is disabled. This gives 0 output current in the disabled mode, compared to standard boost converters where current can still flow when the device is disabled.

The ISL97701 comes in the 10 Ld 3x3 DFN package and is specified for operation over the -40°C to +85°C temperature range.

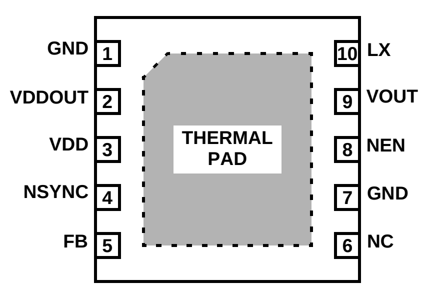
Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
ISL97701IRZ	977 01IRZ	-	10 Ld 3x3 DFN	MDP0047
ISL97701IRZ-T7	977 01IRZ	7”	10 Ld 3x3 DFN	MDP0047
ISL97701IRZ-T13	977 01IRZ	13”	10 Ld 3x3 DFN	MDP0047

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL97701
(10 LD 3X3 DFN)
TOP VIEW



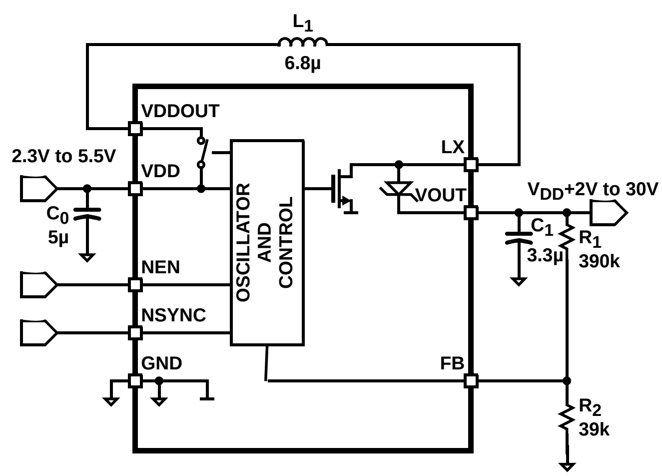
Features

- Up to 87% efficiency
- 2.3V to 5.5V input
- Up to 28V output
- 50mA at 18V
- Integrated boost Schottky diode
- Input voltage disconnect switch
- Synchronization input
- Chip enable
- 10 Ld 3x3 DFN package
- Pb-free plus anneal available (RoHS compliant)

Applications

- OLED display power
- LED display power
- Adjustable power supplies

Typical Application Diagram



NOTE: VOUT = (390k + 39k) / 39k*1.15V = 12.65V

Block Diagram

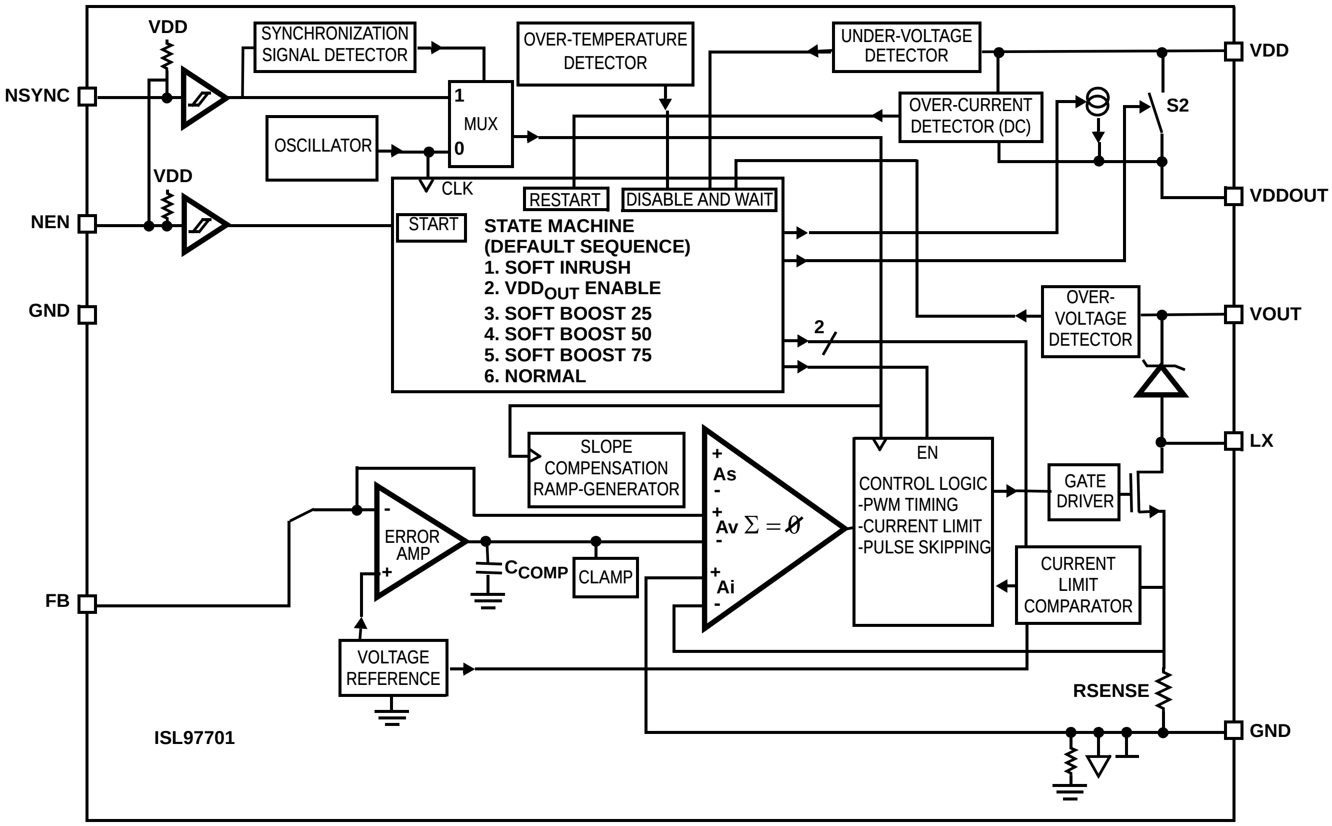


FIGURE 1. ISL97701 BLOCK DIAGRAM

Absolute Maximum Ratings (T_A = +25°C)

VDD to GND . . . . . -0.3 to 6V
V_{OUT} to GND. . . . . -0.3 to 31V
LX to GND . . . . . V_{OUT} + 1V
VDDOUT, NSYNC, FB, NEN
to GND. . . . . -0.3V to VDD + 0.3V
Continuous Current in VDD, GND, VDDOUT, LX 650mA
Continuous Current in NSYNC, FB, NEN 10mA

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package	48	7

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature (T_A) . . . . . -40°C to +85°C
Operating Junction Temperature (T_J) . . . . . +125°C
Maximum Junction Temperature . . . . . +130°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed.

Electrical Specifications

VDD = 3.6V, GND = NEN = 0V, NSYNC = VDD, R_1 = 390k, R_2 = 39k, L = 10µH, T_A = -40°C to +85°C unless otherwise stated

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
VDD	Supply Operating Voltage Range		2.3		5.5	V
I_{DIS}	Supply Current when Disabled	NEN = VDD		0.1	3	µA
LOGIC INPUTS – NEN, NSYNC						
Rup	Pull-up Resistor	Enabled, Input at GND	150	250	350	kΩ
I_{IL}	Leakage Current when Disabled	Disabled, Input at GND	-1		1	µA
VHI	Logic High Threshold		1.8			V
VLO	Logic Low Threshold				0.7	V
POWER-ON RESET – VDD						
V_{RES_ON}	Power On Reset Threshold	VDD rising		2.2	2.3	V
V_{RES_OFF}	Power Off Threshold	VDD falling	1.9	2		V
LX OUTPUT DRIVER						
fosc	LX Switching Frequency with Internal Oscillator		0.9	1	1.1	MHz
fsync	LX Switching Frequency when Externally Synchronized at NSYNC			f (NSYNC)		-
t_{ON-MIN}	Minimum On-Time	FB = 0V, I(LX) > Ilim(LX)		60		ns
$t_{OFF-MIN}$	Minimum Off-time (≥ Maximum Duty Cycle)	FB = 0V, I(LX) < Ilim(LX)		60		ns
r_{ON}	LX On-Resistance	I(LX) = 100mA		0.4		Ω
Ileak	LX Leakage Current	NEN = VDD, V(LX) = 30V		1	5	µA
Ipeak	LX Peak Current Limit	t > 8.32ms (end of soft-start)		1200		mA
SCHOTTKY DIODE – LX, V_{OUT}						
Vdiode	Forward Voltage from LX to V_{OUT}	I = 10mA, T_A = +25°C	0.4	0.5	0.6	V
		I = 10mA, T_A = -40°C to +85°C	0.3	0.5	0.7	V
FEEDBACK INPUTS						
$Vref_{FB}$	Input Reference Voltage on FB	T_A = +25°C	1.13	1.15	1.17	V
		T_A = -40°C to +85°C	1.12	1.15	1.18	V

Electrical Specifications

VDD = 3.6V, GND = NEN = 0V, NSYNC = VDD, R_1 = 390k, R_2 = 39k, L = 10µH, T_A = -40°C to +85°C unless otherwise stated **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
I_{FB}	Input Current in FB	FB = 1.3V	-0.2		0.2	µA
R_{FB}	FB Pull-Down Switch Resistance	I_{FB} = 10mA		15	25	Ω
SYNCHRONIZATION INPUT – NSYNC						
f_{NSYNC}	External Sync. Frequency Range		600		1400	kHz
td_{NSYNC}	NSYNC Falling Edge to LX Falling Edge Delay	f_{NSYNC} = 600kHz		80	100	ns
OVERVOLTAGE DETECTOR - V_{OUT}						
V_{OUT}	Overvoltage Threshold	FB = GND	31	35		V
OVERCURRENT DETECTOR						
$I_{OCTVDDOUT}$	Overcurrent Threshold	t > 2.048ms, DC current		800		mA
OVER-TEMPERATURE DETECTOR						
t_{OFF}	Shut-Down Temperature Threshold	T rising		135		°C
t_{ON}	Turn-On Temperature Threshold	T falling		100		°C
FAULT SWITCH – VDD, VDDOUT						
r_{ONFS}	On-Resistance from VDD to VDDOUT	IOUT = 50mA, t > 2.048ms		0.2		Ω
$Ileak_{VDDOUT}$	Leakage Current	VDDOUT = 0V		0.01	3	µA
I_{SS_VDDOUT}	Soft Inrush Current Source at VDDOUT	VDD - VDDOUT = 0.5V, t_{ON} < 2.048ms		50		mA
REGULATION						
ACC	Output Voltage Accuracy, Assuming Resistor Divider Tolerances of 0.1% or Better	IOUT = 10mA, T_A = +25°C	-1.5		1.5	%
		IOUT = 10mA, T_A = -40°C to +85°C	-2.5		2.5	%
$\Delta V_{OUT}/\Delta IOUT$	Load Regulation	IOUT = 0mA to 50mA		0.05		%
$\Delta V_{OUT}/\Delta VDD$	Line Regulation	VDD = 3.6V to 2.6V, I_{OUT} = 30mA		0.1		%/V

Typical Performance Curves

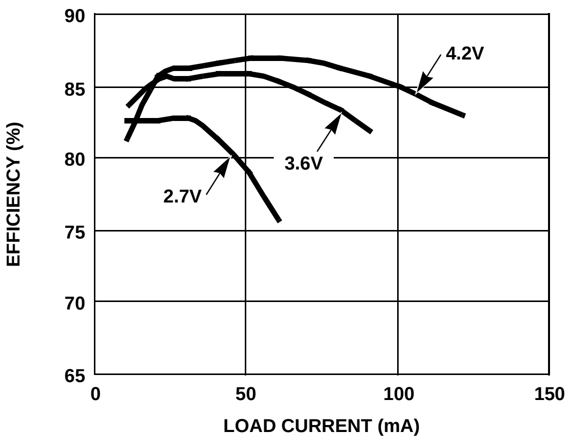


FIGURE 2. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 18.3V) L = 10µH (CDRH4D28C-100NC) C = 6.6µF

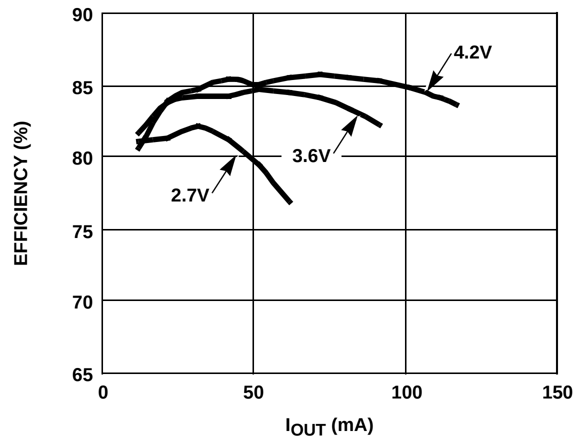


FIGURE 3. EFFICIENCY vs I_{OUT} (V_{OUT} = 18.3V) L = 6.8µH (TDK RLF7030) C = 6.6µF

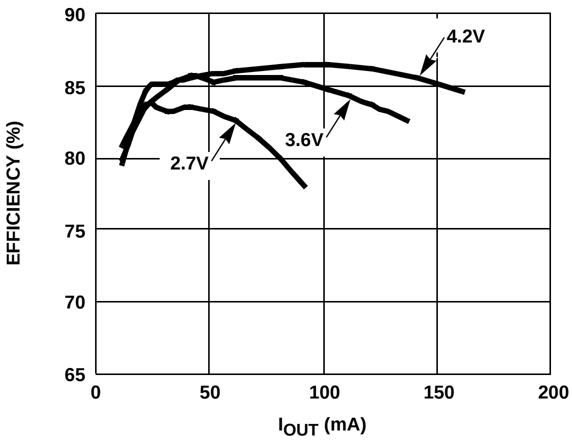


FIGURE 4. EFFICIENCY vs I_{OUT} (V_{OUT} = 12.6V) L = 6.8µH (TDK RLF7030) C = 6.6µF

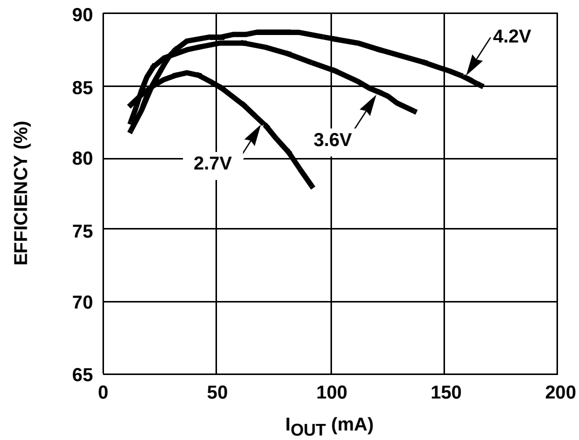


FIGURE 5. EFFICIENCY vs I_{OUT} (V_{OUT} = 12.7V) L = 10µH (CDRH4D28C-100NC) C = 6.6µF

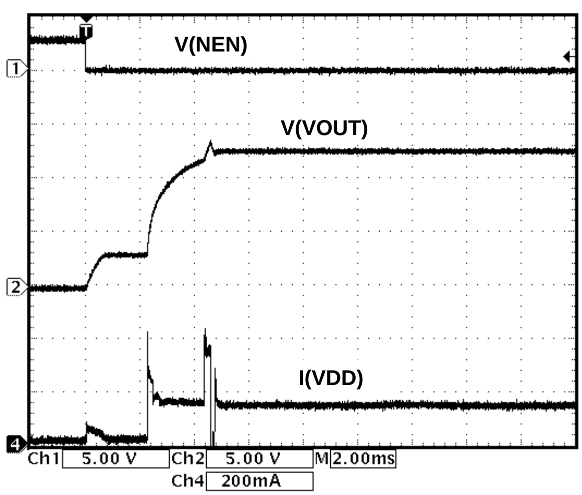


FIGURE 6. START-UP TO 12V (V_{DD} = 3.6V, R_L = 360Ω)

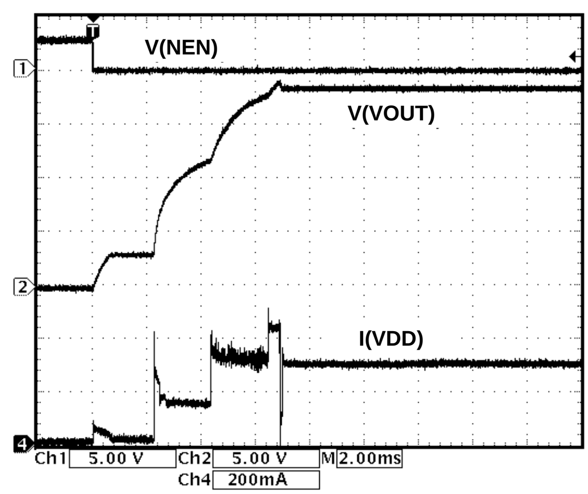


FIGURE 7. START-UP TO 18V (V_{DD} = 3.6V, R_L = 360Ω)

Typical Performance Curves (Continued)

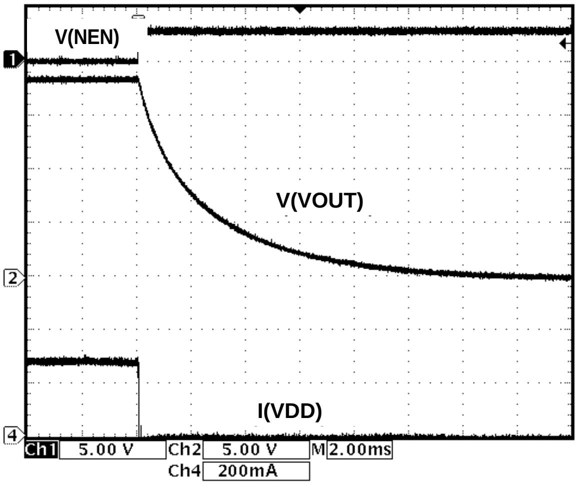


FIGURE 8. SHUT DOWN (V_{DD} = 3.6V, R_L = 360Ω)

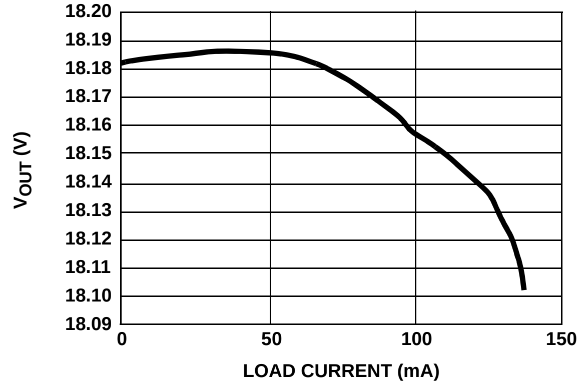


FIGURE 9. LOAD REGULATION (V_{IN} = 3.6V)

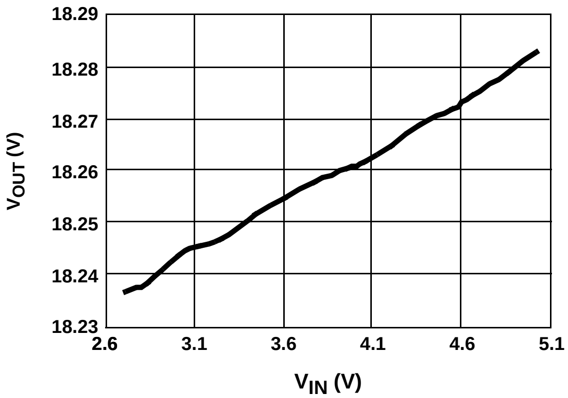


FIGURE 10. LINE REGULATION (I_{OUT} = 30mA)

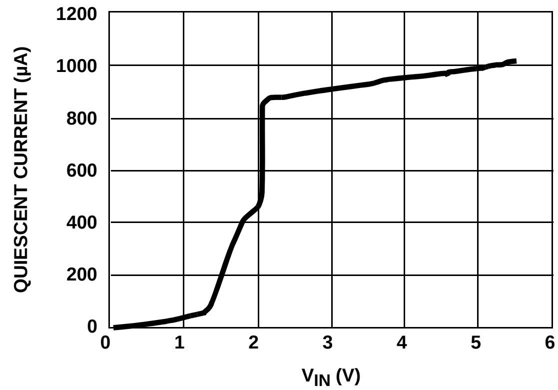
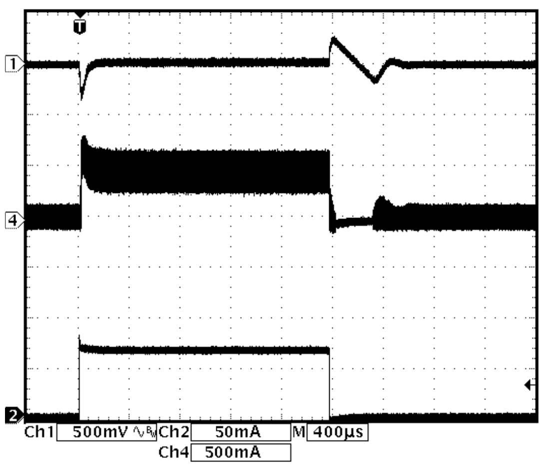


FIGURE 11. QUIESCENT CURRENT vs V_{IN}



(CH1 = V_{OUT}; CH4 = iL; CH2 = I_{OUT})

FIGURE 12. TRANSIENT RESPONSE (V_{IN} = 3.3V; V_{OUT} = 18.3V; STEP LOAD CURRENT FROM 2.6mA TO 70mA)

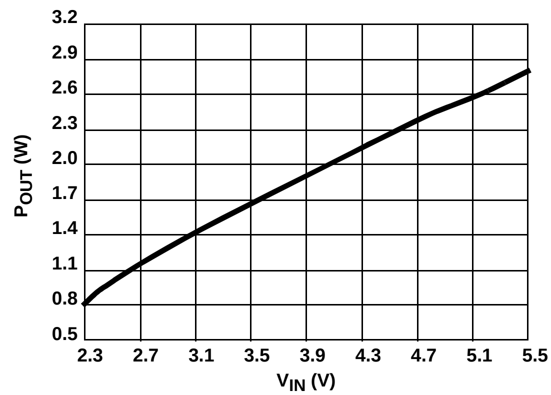


FIGURE 13. RECOMMENDED MAXIMUM OUTPUT POWER vs INPUT VOLTAGE

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	GND	Ground
2	VDDOUT	Protection Switch Output
3	VDD	Supply Input
4	NSYNC	Synchronization Input (Falling Edge)
5	FB	Feedback Input
6	NC	Do Not Connect
7	GND	Ground
8	NEN	Enable Input (Active Low)
9	V_{OUT}	Boost Output Voltage
10	LX	Boost FET

Function Overview

The ISL97701 is a high frequency, high efficiency boost regulator which operates in constant frequency PWM mode. The boost converter generates a stable, higher output voltage from a variable, low voltage input source (e.g. L-Ion battery). The output voltage level is defined from the feedback resistor network in Equation 1.

$$VOUT = \frac{(R1 + R2)}{R2 * Vref_{FB}} \quad \text{(EQ. 1)}$$

The switching frequency is either generated from the fixed 1MHz internal oscillator or provided externally at the synchronization pin in the range from 600kHz to 1.4MHz. The compensation network and soft-start functions are built in with fixed parameters without any need for further external components.

To stop battery discharge into the output load when disabled the inductor is disconnected from the input supply with a low on resistance power switch.

Built in fault protection monitors inductor current and output voltage as well as junction temperature in order to interrupt the high current circuit path through the inductor and diode in the event of a load failure.

Low logic input thresholds allow the ISL97701 to interface directly to micro controllers with lower supply voltage. Alternatively the internal pull-up resistors on all logic inputs provide level shifting when driven from open collector outputs.

Description of Operation

Enable Pin (active low) - NEN

If NEN is high the ISL97701 shuts down all its internal functions and deactivates its I/So. Only the internal pull-up resistor at NEN remains active. If NEN is high the input disconnect switch between VDD and VDDOUT interrupts the circuit path from the input voltage VDD through inductor and diode to the output load at V_{OUT}. If shut down the total supply current in VDD is typically less than 0.1µA.

When NEN is driven low the ISL97701 begins with the start-up sequence.

Start-Up Sequence

After pin NEN is pulled low or a restart is triggered from Fault Control during operation, the ISL97701 goes through a start-up sequence with the following six states: *Soft Inrush -> VDDOUT Enable -> Soft Boost 25 -> Soft Boost 50 -> Soft Boost 75 -> Normal.*

If the sequence has completed, the ISL97701 stays in the "Normal" state until NEN is high again or any fault is detected.

SOFT INRUSH: STATE DURATION ~2.048MS

The switch at VDDOUT is configured as current source and provides a limited current through the inductor to pre-charge the capacitor at V_{OUT}.

VDDOUT ENABLE: STATE DURATION ~128µS

The switch at VDDOUT is fully enabled and connects the inductor to VDD with a low on-resistance.

SOFT BOOST 25 -> 50 -> 75: STATE DURATION 3X ~2.048MS

The boost regulator begins to switch at LX.

The LX current limit increases in three steps representing 25%, 50% and 75% of its final value.

NORMAL

If no fault was detected Normal state is entered ~8.256ms after NEN is pulled low.

The LX current limit steps up to 100%.

In all states Fault Control can force the sequence to restart or even to shut down (see Table 1).

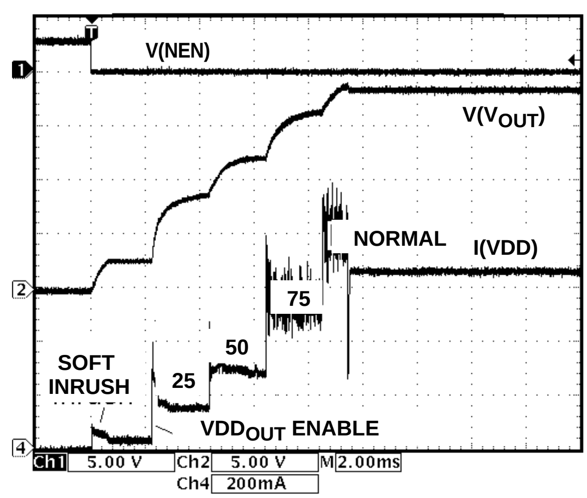


FIGURE 14. FAULT CONTROL SEQUENCE

Fault Control

The input voltage at VDD, current in the VDD_{OUT} switch, voltage at V_{OUT} and junction temperature T_J are continuously monitored and can either restart the start-up sequence or in some cases disable the ISL97701 boost function as long as the fault is present.

TABLE 1. FAULT PROTECTION

FAULT DESCRIPTION	FAULT CONDITION	ISL97701 FAULT REACTION
Undervoltage at VDD	V(VDD) < V(VDD)off	Disables I/Os and waits until V(VDD) reaches V(VDD)on to begin with the start-up sequence
Overcurrent drawn from VDD_{OUT}	$I(VDD_{OUT})$ > $It(VDD_{OUT})err$	Disables VDD_{OUT} switch and LX driver and immediately restarts the start-up sequence
Overvoltage at V_{OUT}	$V(V_{OUT})$ > $Vt(V_{OUT})err$	Disables VDDOUT switch and LX driver and waits until output voltage V(VOUT) drops to Vt(VOUT) to restart the start-up sequence
Over Temperature on chip	Tj > Toff	Disables VDD_{OUT} switch and LX driver and waits until junction temp drops to “Ton” to restart the start-up sequence

Maximum Duty Cycle – LX

The maximum duty cycle Dmax, at which the power FET can operate defines the upper limit of the regulator output to input voltage ratio according to Equation 2:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D_{MAX}} \qquad \text{(EQ. 2)}$$

In the ISL97701, D_{MAX} is defined from the minimum off-time t_{OFF}(LX)min and the switching frequency.

If NSYNC is tied to VDD the internal oscillator defines Dmax to:

$D_{MAX}(f_{OSC}) = 1 - t_{OFF}(LX)min*f_{OSC}$

With external synchronization at pin NSYNC

$D_{MAX}(NSYNC) = 1 - t_{OFF}(LX)min*f(NSYNC)$

The duty cycle at LX can be 0% (**pulse skipping**), if the output voltage exceeds the target voltage set with the feedback resistors.

Internal Schottky Diode – LX, V_{OUT}

The inductor node LX internally connects to the power FET and to the anode of the integrated power Schottky diode. The cathode of the diode is pin V_{OUT}. An overvoltage detector at V_{OUT} continuously monitors the cathode voltage and immediately disables the boost regulator if the voltage exceeds the maximum allowable voltage.

External Synchronization Pin - NSYNC

Pin NSYNC can be used to synchronize the LX output pin with an external clock signal in the range from 600kHz to 1.4MHz.

A frequency detector monitoring NSYNC enables external synchronization if f(NSYNC) is higher than about 300kHz. If the pin is e.g. static high the internal oscillator defines the LX output frequency and phase. When externally synchronized all falling edges at LX are timed from the falling edge of the clock signal applied at NSYNC. The timing of the rising edge at LX is defined by the boost controller.

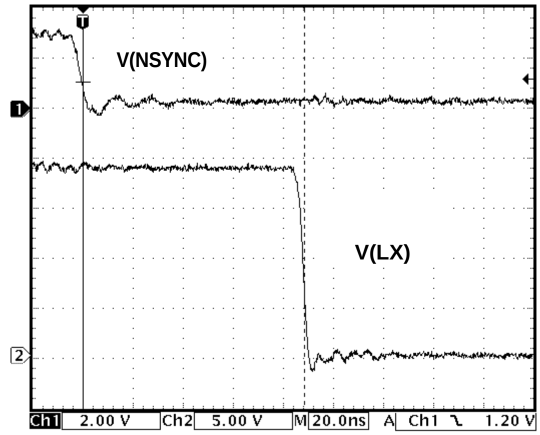


FIGURE 15. NSYNC TO LX SYNCHRONIZATION DELAY

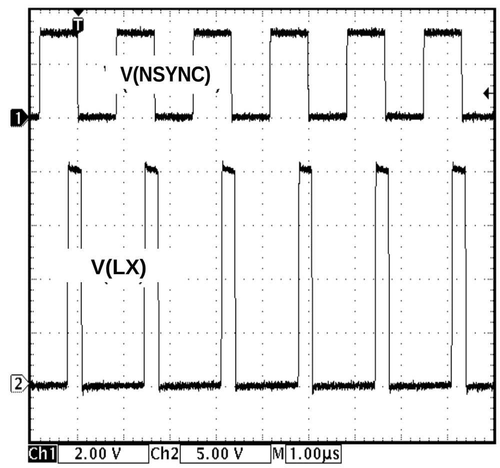


FIGURE 16. LX SYNCHRONIZATION WITH f(SYNC) = 600kHz

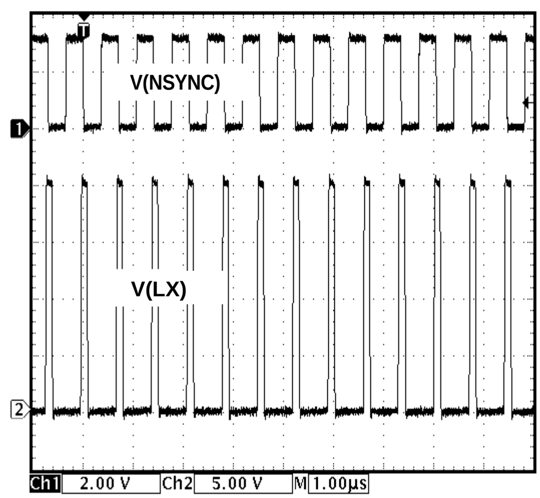


FIGURE 17. LX SYNCHRONIZATION WITH f(SYNC) = 1.4MHz

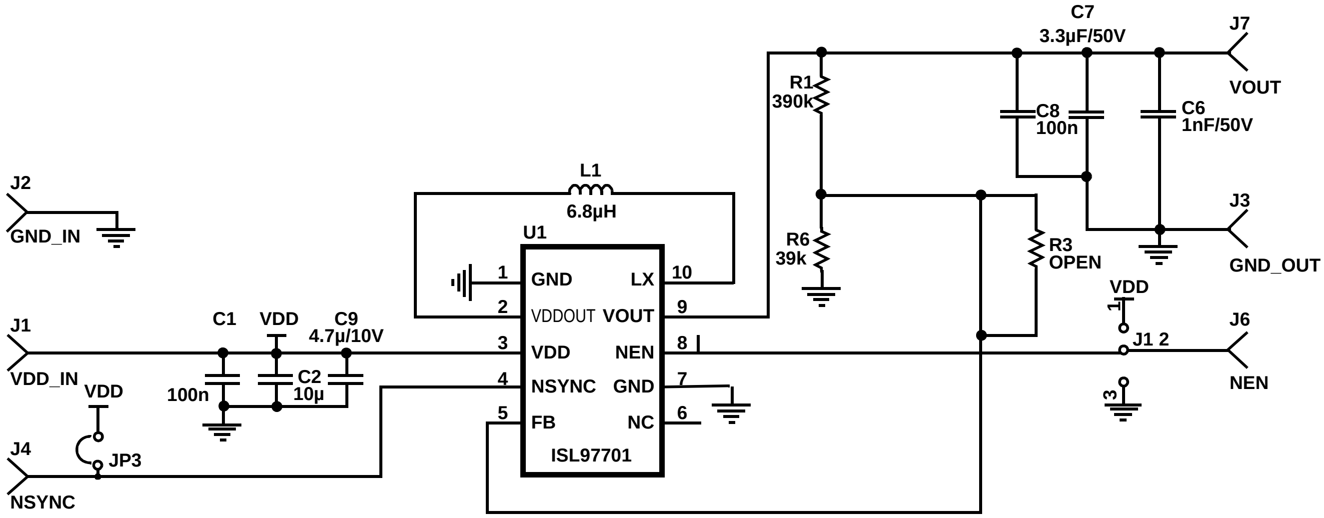


FIGURE 18. ISL97701 APPLICATION BOARD

Typical Application

Typical applications are passive- or active-matrix organic light emitting diode displays (PMOLED, AMOLED) in handheld devices. Applications with low power or screen saver mode is directly supported.

Components Selection

The input capacitance is normally 10µf~15µF and the output capacitor is 3.3µf to 6.6µF. X5R or X7R type of ceramic capacitor with correct voltage rating is recommended. The output capacitor value will affect the output voltage ripple. Higher value of the output capacitor, lower ripple of the output voltage.

When choosing an inductor, make sure the inductor can handle the average and peak currents given by Equations 3, 4 and 5 (80% efficiency assumed):

$$I_{LAVG} = \frac{I_{OUT} \cdot V_{OUT}}{0.8 \cdot V_{IN}} \quad \text{(EQ. 3)}$$

$$I_{LPK} = I_{LAVG} + \frac{1}{2} \cdot \Delta I_L \quad \text{(EQ. 4)}$$

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{L \cdot V_{OUT} \cdot f_{OSC}} \quad \text{(EQ. 5)}$$

Where:

- ΔI_L is the peak-to-peak inductor current ripple in Amperes
- L inductance in H
- f_{OSC} switching frequency, typically 1.0MHz

Optimal combination of the boost inductor L and the output capacitor C_{OUT} are listed in Table 2:

TABLE 2. OPTIMAL COMBINATION OF BOOST INDUCTOR L AND OUTPUT CAPACITOR C_{OUT}

INDUCTOR (µH)	CAPACITOR (µF)	
	MIN	MAX
4.7	2.2	10
6.8	3.3	10
10	4.7	10
15	6.8	10

Recommended Inductor and Ceramic capacitor manufacturers are listed in Table 3:

TABLE 3. RECOMMENDED INDUCTOR AND CERAMIC MANUFACTURERS

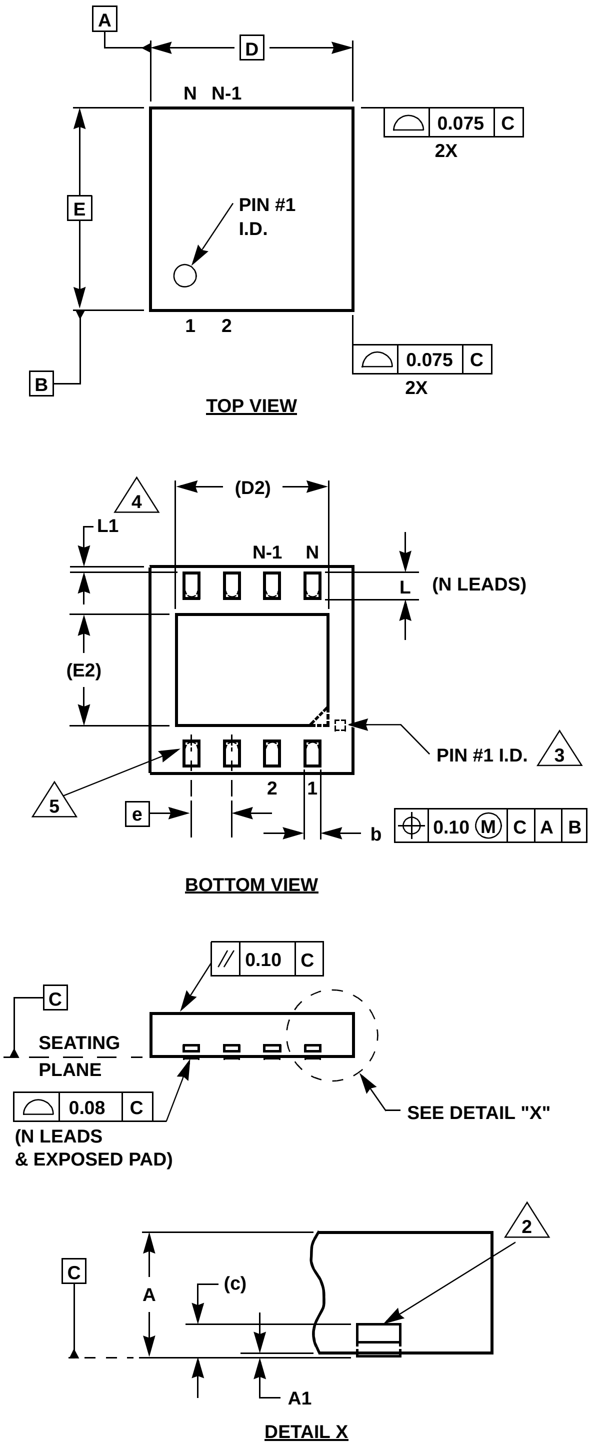
INDUCTOR		CERAMIC CAPACITOR	
Sumida:	www.sumida.com	Taiyo Yuden:	www.t-yuden.com
TDK:	www.tdk.co.jp	AVX:	www.avxcorp.com
Toko:	www.tokoam.com	Murata:	www.murata.com

PCB layout Considerations

The layout is very important for the converter to function properly. To ensure the high pulse current in the power ground does not interfere with the sensitive feedback signals, the current loops (V_{IN}-L1-LX-GND, and V_{IN}-L1-V_{OUT}-C_{OUT}-GND) should be as short as possible. For the DFN package, there is no separated GND. All return GNDs should be connected in GND pin but with no sharing branch.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for the EMI performance.

Dual Flat No-Lead Package Family (DFN)



MDP0047

DUAL FLAT NO-LEAD PACKAGE FAMILY (JEDEC REG: MO-229)

SYMBOL	MILLIMETERS		TOLERANCE
	DFN8	DFN10	
A	0.85	0.90	±0.10
A1	0.02	0.02	+0.03/-0.02
b	0.30	0.25	±0.05
c	0.20	0.20	Reference
D	4.00	3.00	Basic
D2	3.00	2.25	Reference
E	4.00	3.00	Basic
E2	2.20	1.50	Reference
e	0.80	0.50	Basic
L	0.50	0.50	±0.10
L1	0.10	0	Maximum

Rev. 2 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Exposed lead at side of package is a non-functional feature.
3. Bottom-side pin #1 I.D. may be a diepad chamfer, an extended tiebar tab, or a small square as shown.
4. Exposed leads may extend to the edge of the package or be pulled back. See dimension “L1”.
5. Inward end of lead may be square or circular in shape with radius (b/2) as shown.
6. N is the total number of leads on the device.