intersil™

High Power Li-Ion Charger W/I-Path Management

ISL9230

The ISL9230 is a fully integrated high input voltage single-cell Li-ion battery charger with power path management function. This charger performs the CC/CV charge function required by Li-ion batteries. The charger can withstand an input voltage up to 26V but is disabled when the input voltage exceeds 6.6V OVP threshold. The input current limit and charge current are programmable with external resistors. When the battery voltage is lower than 3.0V, the charger preconditions the battery with 10% of the programmed charge current. When the charge current reduces to the end-of-charge (EOC) current level during the CV charge phase, the EOC indicator ($\overline{CHG}$) will toggle to a logic high to indicate the end-of-charge condition.

The ISL9230 uses separate power paths to supply the system load and the battery. This feature allows the system to immediately operate with a completely discharged battery. This feature also allows the charge to terminate when the battery is full while continuing to supply the system power from the input source, thus minimizing unnecessary charge/discharge cycles and prolonging the battery life.

Two indication pins ($\overline{PG}$ and $\overline{CHG}$) allow simple interface to a microprocessor or LEDs.

Features

- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- Current Path Management Optimize for Charge and System Currents
- Intelligent Timeout Interval Based on Actual Charge Current
- 1% Charger Output Voltage Accuracy
- Programmable Input Current Limit
- Programmable Charge Current
- NTC Thermistor Input
- Complies with USB Charger
- Charge Current Thermal Foldback for Thermal Protection
- Trickle Charge for Fully Discharged Batteries
- 26V Maximum Voltage at VIN Pin
- Power Presence and Charge Indications
- Ambient Temperature Range: -40°C to +85°C
- 16 Ld 3x3 TQFN Package
- Pb-Free (RoHS Compliant)

Applications

- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

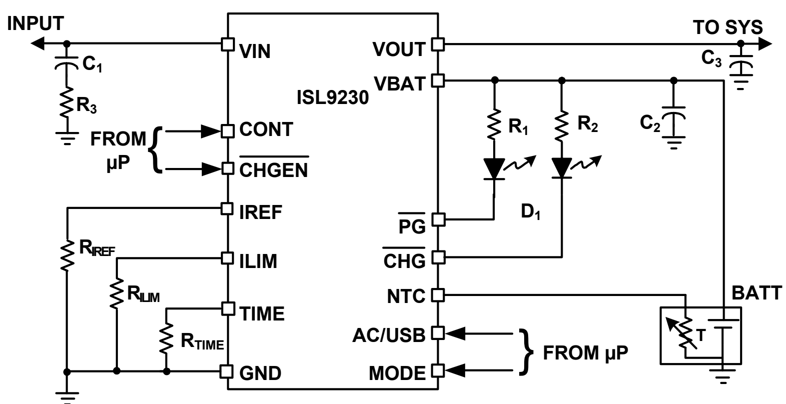
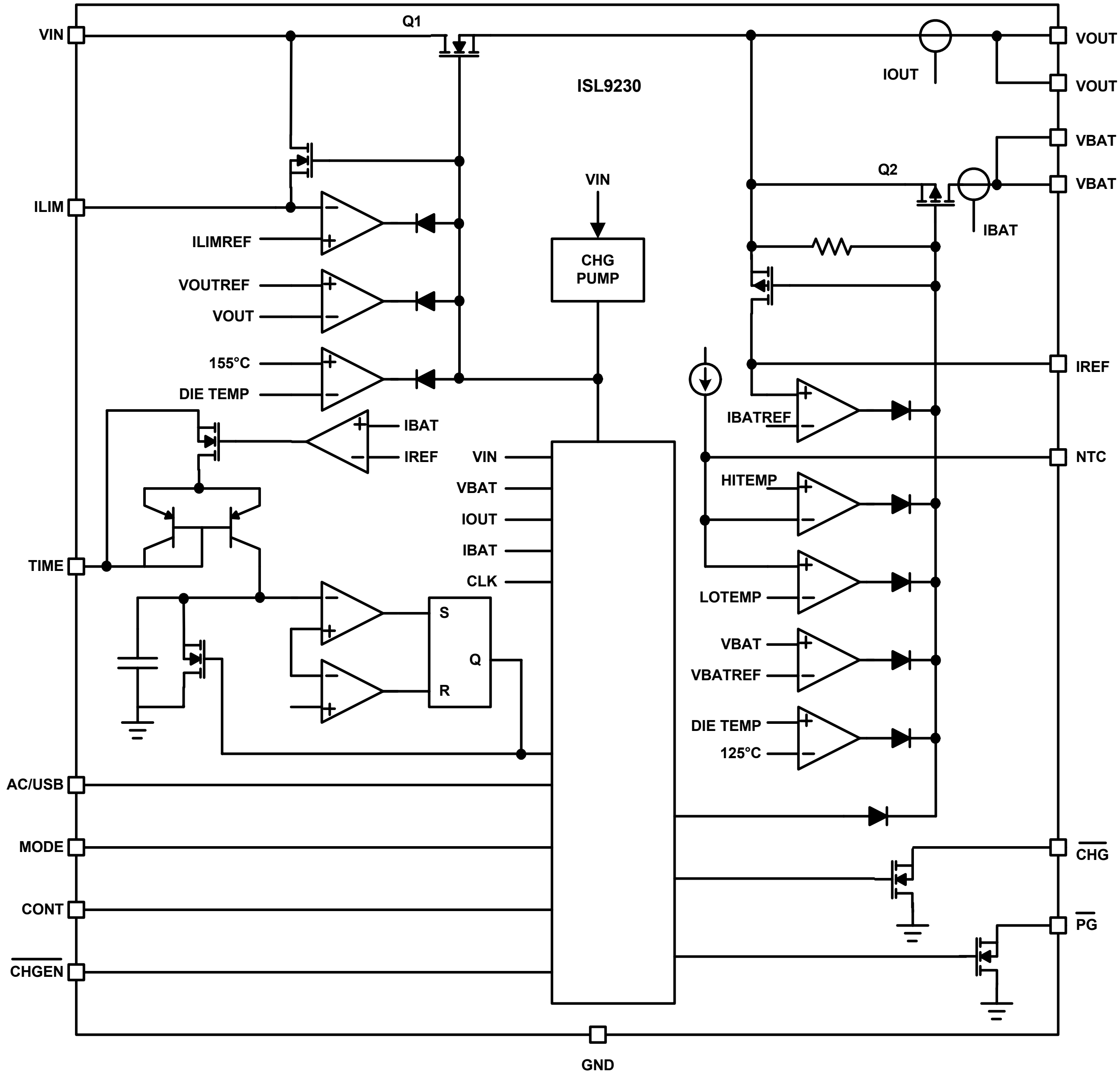


FIGURE 1. TYPICAL APPLICATION CIRCUIT

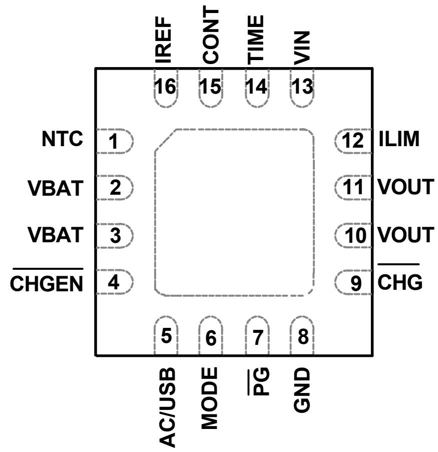
PART	DESCRIPTION
C_1	4.7µF X5R ceramic capacitor
C_2	1µF X5R ceramic capacitor
C3	4.7µF X5R ceramic capacitor
R_3	1Ω, 5% resistor
R_{IREF}	(Application specific)
R_{TIME}	(Application specific)
R_{ILIM}	(Application specific)
R_1, R_2	300 to 1kΩ, 5% resistor
D_1, D_2	LEDs for indication

Block Diagram



Pin Configuration

ISL9230
(16 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	NTC	The NTC pin sources a current to develop a voltage across the battery pack NTC resistor. Placing a 10kΩ NTC thermistor will check if the battery's temperature is out of the safe temperature window. If the temperature is out of the safe operating window, the charger is suspended. For applications that do not require the use of the NTC function, connect a 10kΩ fixed resistor from NTC to GND to maintain a valid voltage level on the NTC pin.
2, 3	VBAT	Charger output pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes.
4	$\overline{CHGEN}$	Battery charger enable pin. The $\overline{CHGEN}$ pin is a logic input pin to provide external charge control. An internal 670kΩ pull-down resistor is connected to this pin. Drive the pin HIGH to disable the charger during charging. When $\overline{CHGEN}$ is high, VOUT is still active and the battery power remains available at VOUT. To ensure proper operation, do not leave this pin unconnected.
5	AC/USB	Selects between Adapter and USB input power. Pull high for selecting adapter power and pull low for USB power. An internal 670kΩ pull-down resistor is connected to this pin. To ensure proper operation, do not leave this pin unconnected.
6	MODE	In combination with the AC/USB pin, this pin selects the input current limit levels. If AC/USB pin is low, a low on the Mode pin sets the USB current to 100mA, and a high selects the 500mA limit. If the AC/USB pin is high, a low on the mode pin selects the ILIM programmed current and a high will put the ISL9230 into a suspend state. An internal 300kΩ pull-down resistor is connected to this pin. To ensure proper operation, do not leave this pin unconnected.
7	$\overline{PG}$	Open-drain power good indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold. This pin is capable of sinking 5mA (minimum) to drive a LED. The maximum voltage rating for this pin is 6.5V and it is recommended to use VOUT as the pull-up voltage.
8	GND	Connect to ground.
9	$\overline{CHG}$	Open-drain charge indication pin. This pin outputs a logic LOW when a charge cycle starts and goes Hi-Z when an end-of-charge (EOC) condition is qualified. This pin is capable of sinking 5mA min. to drive an LED. When the charger is disabled, the $\overline{CHG}$ is also in a Hi-Z state.
10, 11	VOUT	Output connection to the system. When a valid input power is present, this pin provides a 3.4V regulated voltage for the system during trickle charge and is maintained at VBAT + 225mV during fast charging. A 4.7µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes.
12	ILIM	Input current limit programming pin. Connect a resistor between this pin and the GND to set the input current limit determined by Equation 1 when AC/USB = 1, MODE = 0 $I_{LIM} = \frac{1610}{R_{ILIM}} \quad (mA) \qquad 200mA < ILIM < 1.5A$ (EQ. 1) Where R_{ILIM} is in kΩ If the ILIM pin is left unconnected, all input current is disabled.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
13	VIN	Power input. The absolute maximum input voltage is 26V. A 10µF or larger value capacitor is recommended to be placed very close to the input pin for decoupling purposes. Additional capacitance may be required to provide a stable input voltage.
14	TIME	Timing resistor pin. The TIME pin determines the oscillation period by connecting a timing resistor between this pin and GND. The oscillator also provides a time reference for the charger calculated in Equation 2. Equation 3 provides the formula for finding the Pre-charge time, which is 1/10 of the Fast Charge timer. Leaving the TIME pin unconnected sets the timer to the default values of 30 minutes for pre-charge and 5 hours for fast charge. $t_{FAST} = 8 \times R_{TIME} \quad (\mathrm{Min})$ (EQ. 2) $t_{PRE} = 0.8 \times R_{TIME} \quad (\mathrm{Min})$ (EQ. 3) Where R_{time} is in kΩ
15	CONT	Active high overrides the end-of-charge (EOC) or timer termination. By pulling the continuous charge CONT pin high, the device will continue to charge the battery when the current has fallen below IMIN or the safety timer has timed out. The status of this pin can not be changed after POR. The CONT pin is internally pulled down to GND by a 300kΩ resistor, but to ensure proper operation, do not leave the CONT pin floating.
16	IREF	Charge current program and monitoring pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by Equation 4: $I_{REF} = \frac{890}{R_{IREF}} \quad (\mathrm{mA})$ (EQ. 4) Where R_{IREF} is in kΩ. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, V_{IREF} = 0V.
-	EPAD	Exposed pad. Connect as much copper as possible to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

TABLE 1. INPUT CURRENT LIMIT SELECTION

AC/USB	MODE	DESCRIPTION
0	0	USB 100mA limit
0	1	USB 500mA limit
1	0	R_{LIM} current programming
1	1	Suspend mode

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9230IRZ	DLBB	-40 to +85	16 Ld 3x3 QFN	L16.3x3E

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9230. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (Referenced to GND)

VIN . . . . . -0.3V to 26V
All other pins . . . . . -0.3V to 6.5V
I_{VIN} (Input Current) 1.6A
I_O Output Current (Continuous)
- I_{VOUT} (Continuous) 5A
- I_{VBAT} (Discharge Mode) 5A
- I_{VBAT} (Charging Mode) 1.5A
- Output Sink Current $\overline{CHG}$, $\overline{PG}$ 15mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	41	3.0

Maximum Junction Temperature (Plastic Package) . . . . -40°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Maximum Supply Voltage (VIN Pin) 24V
Operating Supply Voltage (VIN Pin) . . . . . 4.3V to 6.4V
Programmed Charge Current . . . . . 200mA to 1500mA
I_{VIN} Input current, VIN Pin 1.5A
I_{VOUT} Current, VOUT Pin 4.5A
I_{VBAT} Current, VBAT Pin (Discharging) 4.5A
I_{VBAT} Current, BAT Pin (Charging) 1.5A
ESD Ratings
- Human Body Model (Tested per JESD22-A114F) 2.5kV
- Machine Model (Tested per JESD22-A115-A) 250V
- Charged Device Model (Tested per JESD22-C101D) 1000V

Latch Up (Tested per JESD78B, Class II, Level A) 100mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical values are tested at V_{IN} = 5V, V_{BAT} = 3.6V and the ambient temperature at +25°C. MIN/MAX limits are across the operating conditions, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER-ON RESET						
Rising POR Threshold	V_{POR_R}	V_{BAT} = 3.0V, use $\overline{PG}$ to indicate the comparator output	**3.2**	3.36	**3.5**	V
Falling POR Threshold	V_{POR_F}		**2.92**	3.05	**3.18**	V
POR Deglitch Time	t_{PG}	V_{IN} >V_{POR} to $\overline{PG}$ Low		1.2		ms
V_{IN-BAT} OFFSET VOLTAGE						
Rising Threshold	V_{OS_R}	V_{BAT} = 3.6V, V_{IN} ramps from 3.5V to 4V	**50**	80	**130**	mV
Falling Threshold	V_{OS_F}	V_{BAT} = 3.6V, V_{IN} ramps from 4V to 3.5V	**20**	60		mV
VIN OVERVOLTAGE PROTECTION						
Overvoltage Protection Threshold	V_{OVP}		**6.25**	6.6	**6.9**	V
OVP Threshold Hysteresis	V_{OVP_HYS}			110		mV
Input Overvoltage Blanking	t_{OVP_BLK}			50		µs
Input OVP Recovery Time	$t_{OVP-REC}$			1.2		ms
BATTERY DETECTION						
Battery Detection Current	I_{DET}	V_{BAT} = 2.5V (Note 7)	**-5**	-7.5	**-10**	mA
Detection Timer	t_{DET}			250		ms
ILIM, IREF SHORT CIRCUIT DETECTION (CHECKED DURING START-UP)						
Current Source	I_{SC}	VIN ≥ VPOR and VIN ≥ VBAT + VOS		1.4		mA

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Short-Circuit Detection threshold	V_{SC}	VIN > VPOR and VIN > VBAT + VOS		510		mV
SHORT CIRCUIT DETECTION						
Battery Short Circuit Detection Current	I_{BSC}	V_{BAT} = 1.5V	**3**	5.5	**8**	mA
Battery Short Circuit Threshold	V_{BSCT}		**1.6**	1.8	**2.0**	V
Output Short Circuit Detection at Valid VIN	V_{OSC1}	VIN > VPOR VIN > VBAT + VOS	**0.8**	0.9	**1.0**	V
Output Short Circuit Detection, Load Sharing Mode (Note 7)	V_{OSC2}	Referenced to VBAT VIN > VPOR VIN > VBAT + VOS	**-200**	-250	**-300**	mV
Blanking Time for VSC2	BT_{OSC2}			250		µs
Recovery Time for VSC2	RT_{OSC2}			60		ms
OPERATING CURRENT						
BAT Pin Supply Current	I_{VBAT}	No supply at V_{IN}, $\overline{CHGEN}$ = LOW			**6.5**	µA
VIN Pin Suspend Current	I_{VIN}	Charger enabled, AC/USB = Mode = 1			**200**	µA
VIN Pin Supply Current	I_{VIN}	Charger enabled			**1.5**	mA
VOLTAGE REGULATION						
Output Voltage	V_{O_REG}	VIN > VOUT + VDO_Q1, VBAT > 3.2V System current + charge current = 15mA	**VBAT + 0.150**	VBAT + 0.225	**VBAT + 0.270**	V
		VIN > VOUT + VDO_Q1, VBAT < 3.2V System current + charge current = 15mA	**3.3**	3.4	**3.5**	
Charger Output Voltage	V_{B_REG}	Charge current = 10mA, T_A = +25°C	4.185	4.20	4.215	V
		Charge current = 10mA	**4.16**	4.20	**4.23**	
IREF Pin Voltage	V_{IREF}	V_{BAT} = 3.8V	**1.8**	2.24	**2.55**	V
POWER PATH						
Output DPPM Threshold Voltage	V_{DPPM}	Output voltage threshold where charge current starts to reduce. Referenced to regulated V_{OUT}	**-200**	-100	**-50**	mV
Input DPM Threshold Voltage	$V_{IN\text{-}DPM}$	Input voltage threshold where the input current starts to reduce, AC/USB = 0, MODE = X		4.36		V
Battery Supply Enter Threshold	V_{BSUP_ON}	Referenced to VBAT, V_{BAT} = 3.6V		-40		mV
Battery Supply Exit Threshold	V_{BSUP_OFF}	Referenced to VBAT, V_{BAT} = 3.6V		-20		mV
DROPOUT VOLTAGE						
Q1 Dropout Voltage (VIN-VOUT) (Note 7)	V_{DO_Q1}	V_{OUT} = 4.3V, I_{IN} = 1A, V_{BAT} = 4.2V		300	**475**	mV
Q2 Dropout Voltage (VBAT-VOUT)	V_{DO_Q2}	V_{IN} = 0V, VBAT > 3V, IOUT = 1A		40	**80**	mV
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RCH}	Referenced to V_{B_REG}	**-215**	-120	**-50**	mV
Recharge Deglitch Time	t_{RCH}	t_{RCH} includes t_{DET} (CONT = 0)		300		ms
Delay Time, Input Power Loss to VOUT LDO Turn-Off	$t_{NO\text{-}IN}$	V_{BAT} = 3.6V Time is measure from VIN: 5V to 3V at 1µs fall time		20		ms
CURRENT REGULATION (Note 6)						
Input Current Limit Range	I_{LIM_RNG}		**200**		**1500**	mA

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Input Current Limit Accuracy	I_{LIM_AC1}	R_{ILIM} = 1.62kΩ	**955**	1000	**1045**	mA
	I_{LIM_AC2}	R_{ILIM} = 4.32kΩ	**340**	375	**410**	mA
	I_{LIM_100}	AC/USB = 0, Mode = 0	**78**	88	**98**	mA
	I_{LIM_500}	AC/USB = 0, Mode = 1	**380**	440	**500**	mA
Fast Charge Current Range	I_{CHG}	V_{BAT} < 4.2V	**300**		**1500**	mA
Fast Charge Current		R_{IREF} = 1.78kΩ	**450**	500	**550**	mA
		R_{IREF} = 887Ω	**900**	1000	**1100**	mA
Trickle Charge Current	I_{TRK}	AC/USB, MODE not equal to (1, 1) R_{IREF} = 1.78kΩ (I_{TRK} = 88/R_{IREF})	**39**	49	**58**	mA
End Of Charge Current	I_{EOC_USB100}	AC/USB = 0, Mode = 0, R_{IREF} = 887Ω	**13**	29	**46**	mA
	I_{EOC_USB500}	AC/USB = 0, Mode = 1, R_{IREF} = 887Ω	**70**	96	**125**	mA
	I_{EOC_AC}	R_{IREF} = 887Ω	**76**	96	**116**	mA
End Of Charge Deglitch Time	t_{EOC}			25		ms
PRECONDITIONING VOLTAGE THRESHOLD						
Preconditioning Threshold Voltage	V_{MIN}	VIN > VPOR and VIN > VBAT + VOS	**2.9**	3.0	**3.1**	V
Precharge to Fast Charge Deglitch Time	t_{CHG_LH}			25		ms
Fast Charge to Precharge Deglitch Time	t_{CHG_HL}			25		ms
CHARGING TIMERS (Note 7)						
Fast Charge Timer	t_{FAST}	R_{TIME} = 30kΩ	**180**	240	**300**	Min
		R_{TIME} = Floating	**240**	300	**360**	
Pre-Charge Timer	t_{PRE}	R_{TIME} = 30kΩ		24		Min
		R_{TIME} = Floating	**24**	30	**36**	
INTERNAL TEMPERATURE MONITORING						
Charger Current Thermal Foldback Threshold	T_{FOLD}			125		°C
Thermal Shutdown Threshold	T_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		°C
EXTERNAL TEMPERATURE MONITORING						
Thermistor Bias Current	I_T	VIN >VPOR and VIN > VBAT + VOS	**72**	75	**78**	µA
High Temperature Threshold	V_{TMAX}	V_{NTC} falling	**240**	295	**340**	mV
High Temperature Hysteresis	V_{TMAX_H}	V_{NTC} rising after reaching V_{TMAX}		30		mV
Low Temperature Threshold	V_{TMIN}	V_{NTC} rising	**2000**	2100	**2200**	mV
Low Temperature Hysteresis	V_{TMIN_H}	V_{NTC} falling after reaching V_{TMIN}		300		mV
Temperature Trip Deglitch Time	t_{T_DG}	Measured from NTC fault to charger disabled		50		ms
NTC Pin Disable Threshold	V_{DIS_NTC}	Referenced to VIN, NTC floating		-300		mV
LOGIC INPUT AND OUTPUTS						
$\overline{CHGEN}$, CONT, MODE, AC/USB Logic Input High			**1.4**			V
$\overline{CHGEN}$, CONT, MODE, AC/USB Logic Input Low					**0.4**	V

Electrical Specifications

Typical values are tested at V_{IN} = 5V, V_{BAT} = 3.6V and the ambient temperature at +25°C. MIN/MAX limits are across the operating conditions, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
$\overline{CHGEN}$ and AC/USB Pin Internal Pull-Down Resistance			**570**	670	**770**	kΩ
CONT and MODE Pin Internal Pull-Down Resistance			**220**	280	**340**	kΩ
$\overline{PG}$, $\overline{CHG}$						
Driving Capability when LOW		Pin Voltage = 0.4V	**5**			mA
Leakage Current when HIGH		Pin Voltage = 5V, V_{OUT} = V_{BAT} = 5V			**1**	µA

NOTES:

6. The input current charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.
7. Limits established by characterization and are not production tested.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Characteristics V_{IN} = 5V, V_{BAT} = 3.6V, AC/USB = 1, MODE = 0, T_A = +25°C, unless otherwise specified.

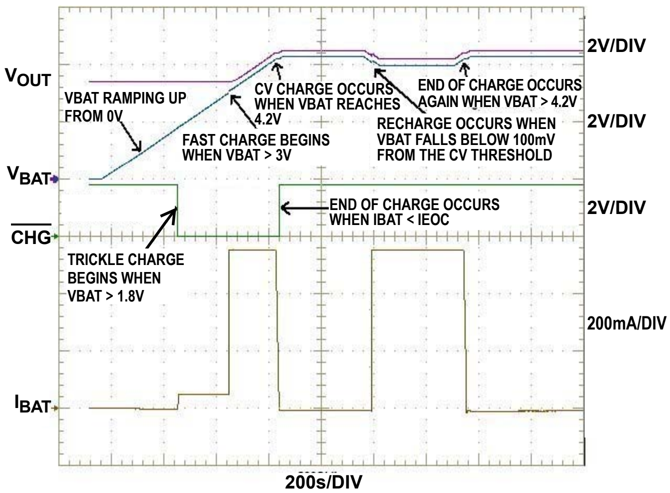


FIGURE 2. DESCRIPTION OF CHARGING MODES AS V_{BAT} VARIES

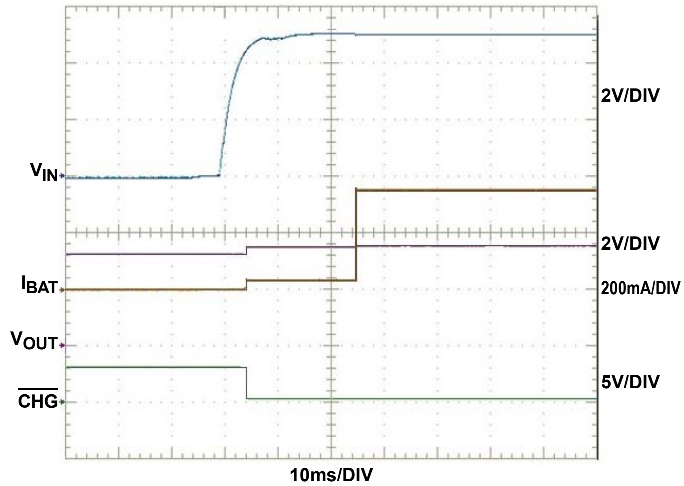


FIGURE 3. ADAPTER PLUG-IN WITH BATTERY CONNECTED

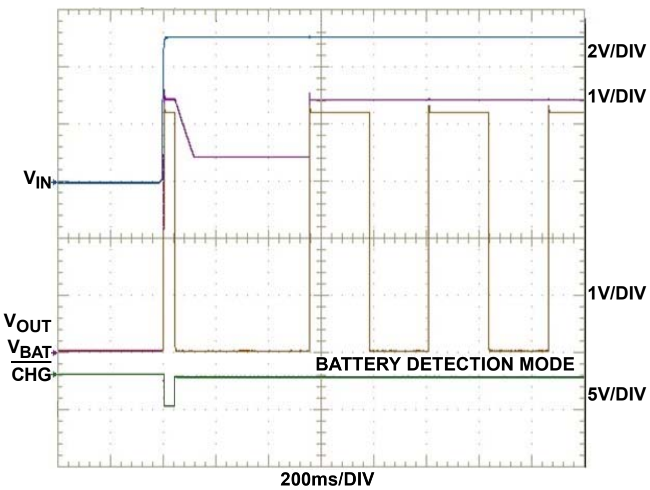


FIGURE 4. BATTERY DETECTION - BATTERY REMOVED

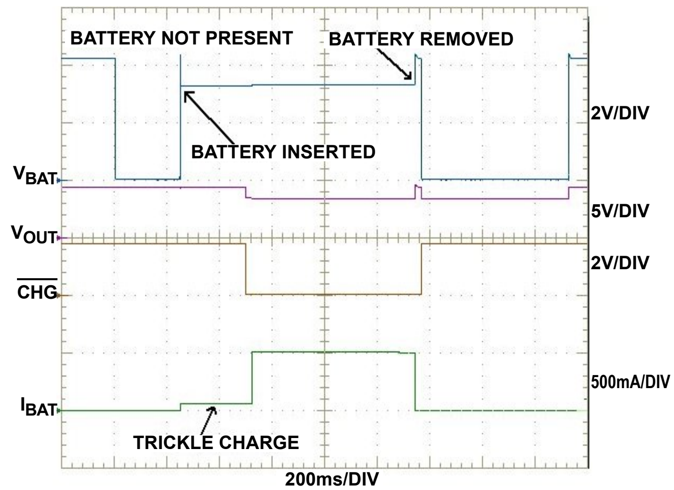


FIGURE 5. BATTERY DETECTION - BATTERY INSERTED/REMOVED

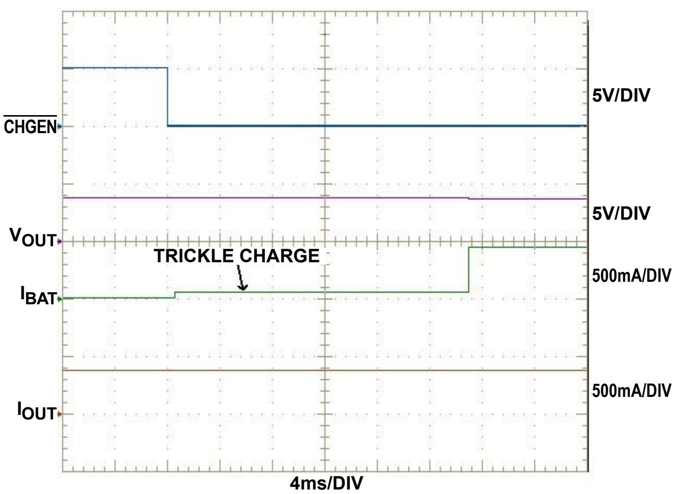


FIGURE 6. CHARGER ON/OFF BY CHGEN (R_{OUT} = 10Ω)

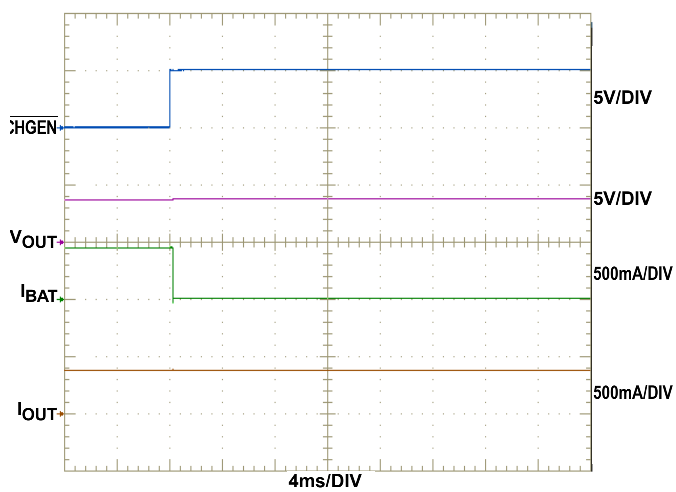


FIGURE 7. CHARGER ON/OFF CHGEN (R_{OUT} = 10Ω, V_{BAT} = 3.6V)

Typical Characteristics V_{IN} = 5V, V_{BAT} = 3.6V, AC/USB = 1, MODE = 0, T_A = +25°C, unless otherwise specified. (Continued)

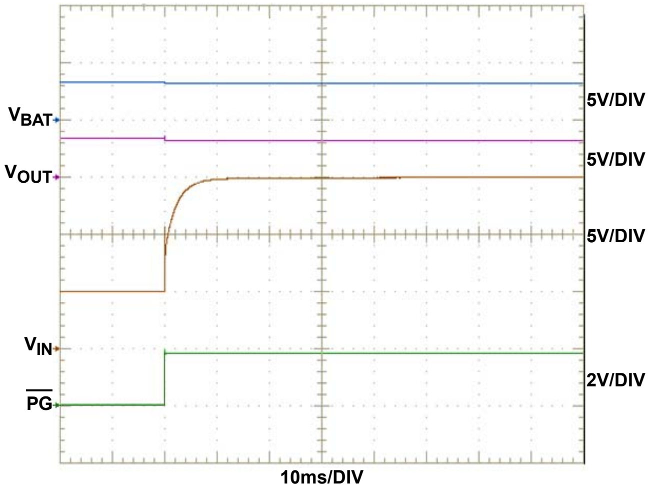


FIGURE 8. OVP FAULT V_{IN} = 5V TO 15V, R_{OUT} = 10Ω

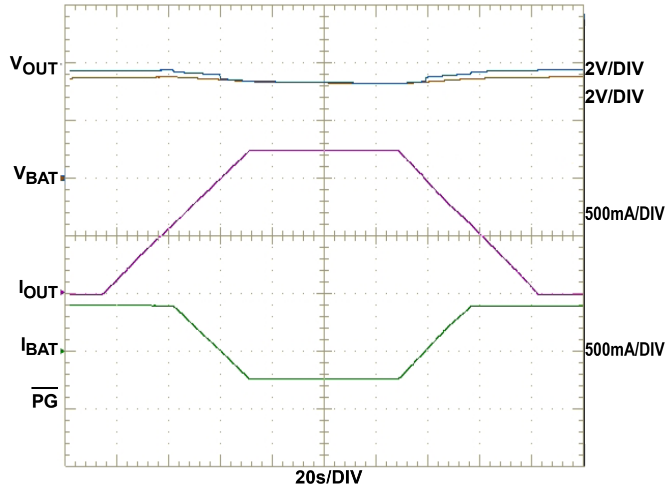


FIGURE 9. ENTERING AND EXITING DPPM MODE

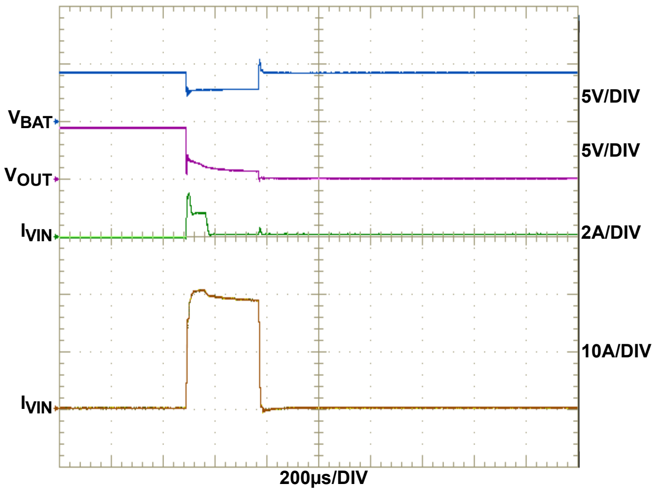


FIGURE 10. V_{OUT} SHORTED WITH BATTERY CONNECTED

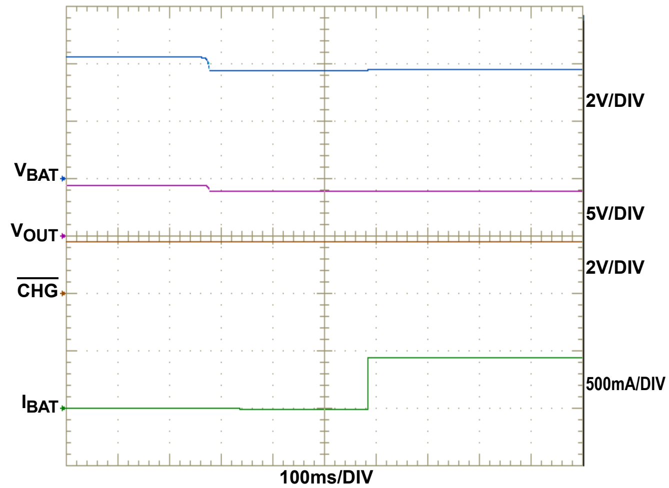


FIGURE 11. V_{BAT} TOGGLE FROM 4.3V TO 3.8V (NO OUTPUT)

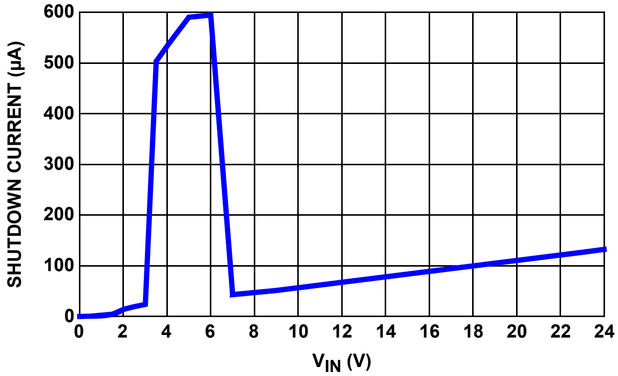


FIGURE 12. SHUTDOWN CURRENT $\overline{CHGEN}$ = 1

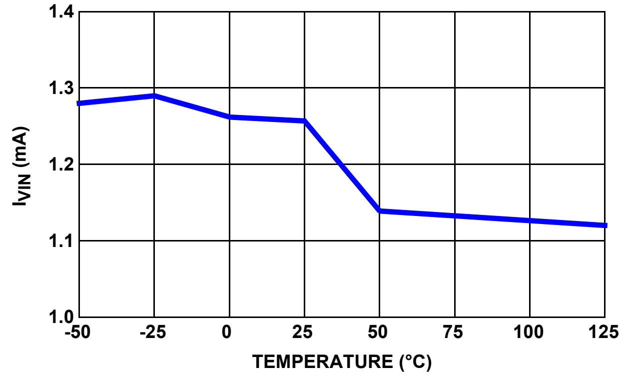


FIGURE 13. VIN PIN SUPPLY CURRENT $\overline{CHGEN}$ = 0

Typical Characteristics
V_{IN} = 5V, V_{BAT} = 3.6V, AC/USB = 1, MODE = 0, T_A = +25°C, unless otherwise specified. **(Continued)**

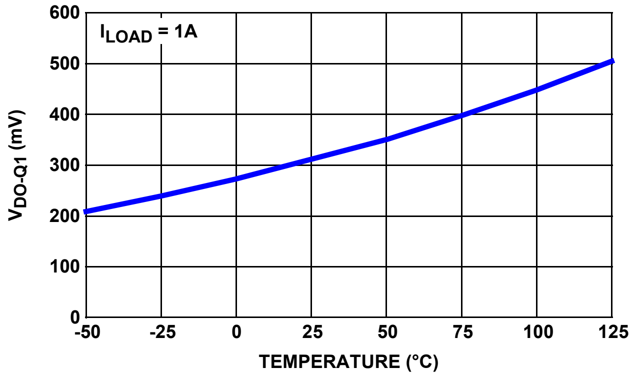


FIGURE 14. DROPOUT VOLTAGE (Q1) vs TEMPERATURE

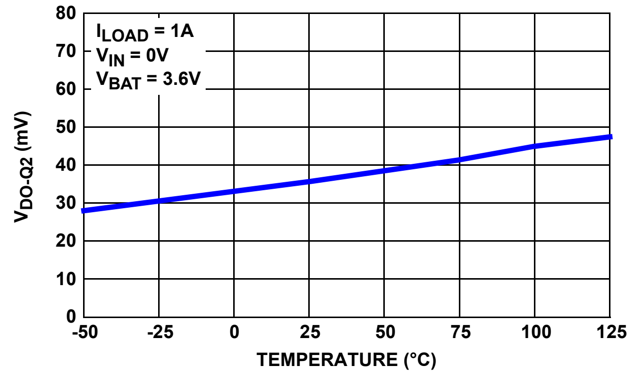


FIGURE 15. DROPOUT VOLTAGE (Q2) vs TEMPERATURE

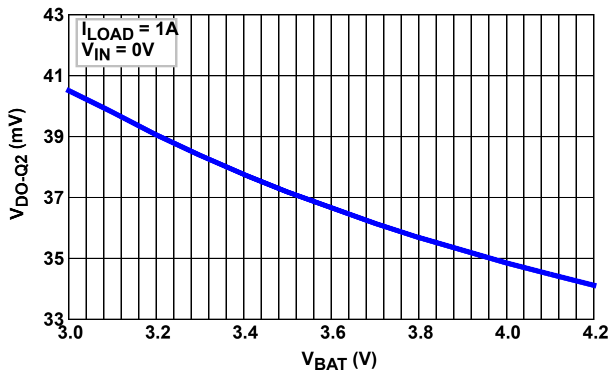


FIGURE 16. DROPOUT VOLTAGE (Q2) vs V_{BAT}

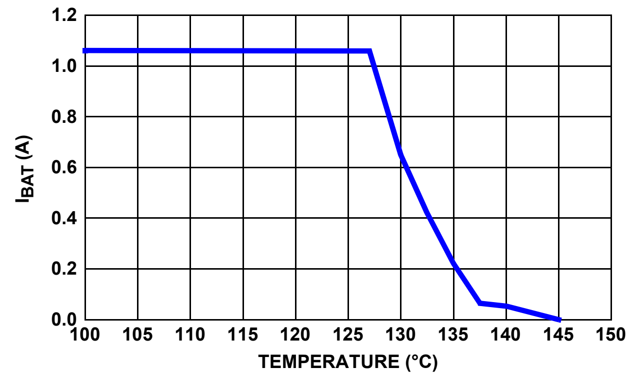


FIGURE 17. THERMAL REGULATION OF I_{BAT}

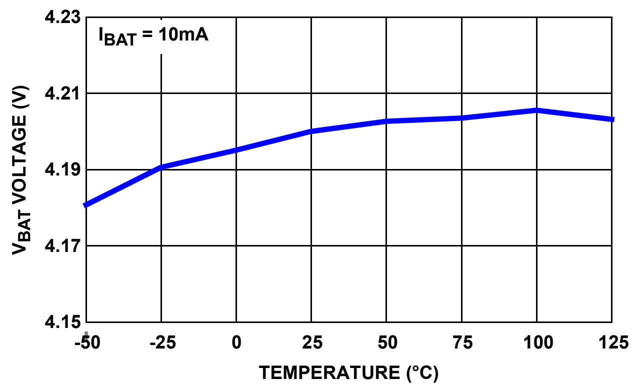


FIGURE 18. BATTERY VOLTAGE REGULATION vs TEMPERATURE

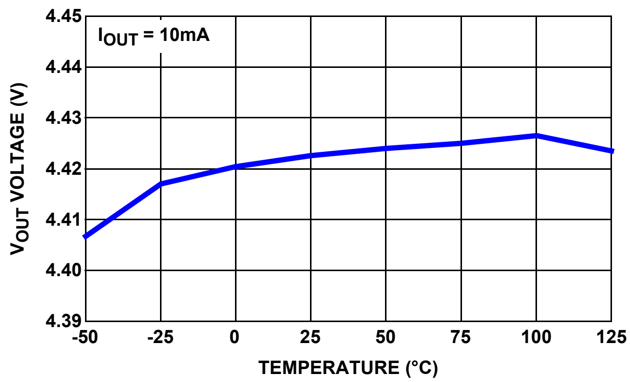


FIGURE 19. OUTPUT VOLTAGE REGULATION vs TEMPERATURE

Typical Characteristics V_{IN} = 5V, V_{BAT} = 3.6V, AC/USB = 1, MODE = 0, T_A = +25°C, unless otherwise specified. (Continued)

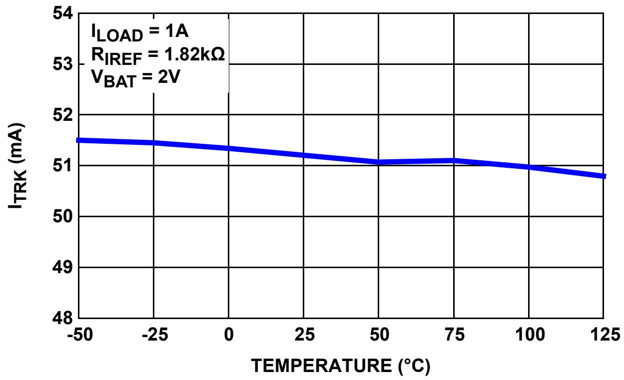


FIGURE 20. TRICKLE CHARGE vs TEMPERATURE

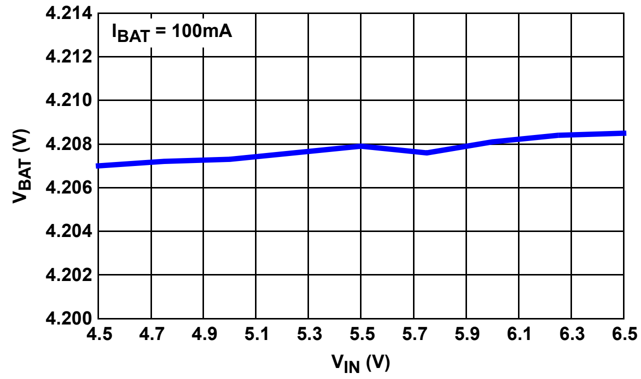


FIGURE 21. BATTERY VOLTAGE vs INPUT VOLTAGE

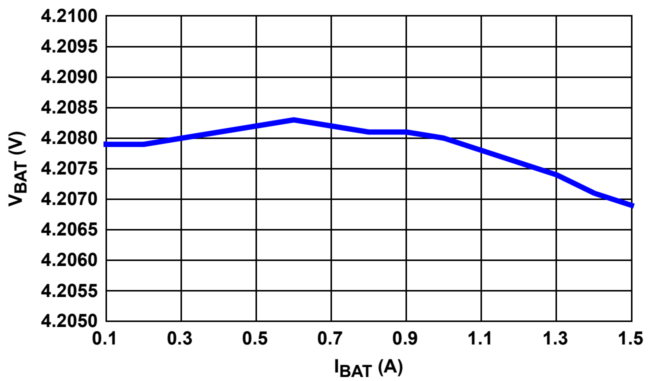


FIGURE 22. BATTERY VOLTAGE vs CHARGE CURRENT (CV MODE)

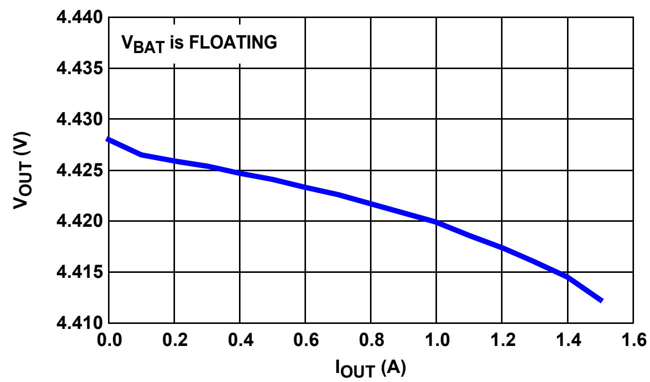


FIGURE 23. OUTPUT VOLTAGE vs OUTPUT CURRENT

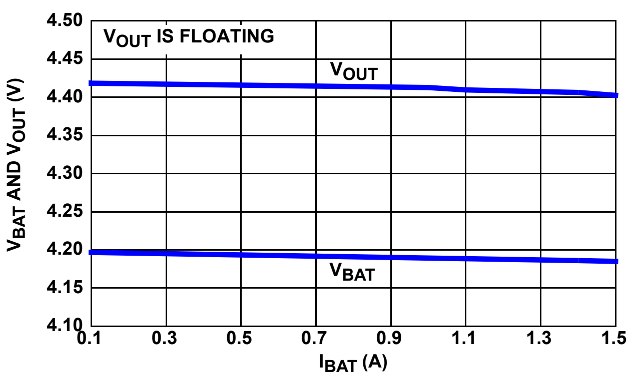


FIGURE 24. V_{BAT} AND V_{OUT} vs CHARGE CURRENT (CV MODE)

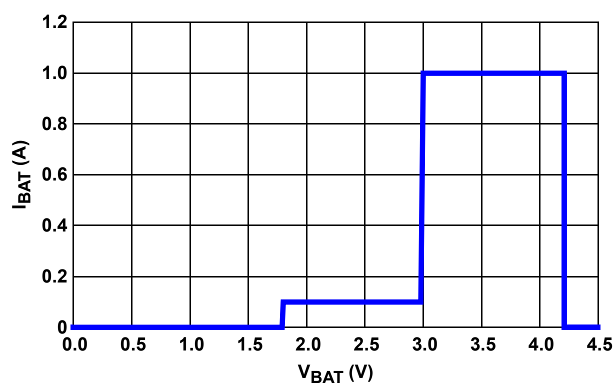


FIGURE 25. BATTERY VOLTAGE vs CHARGE CURRENT (CC MODE)

Typical Characteristics V_{IN} = 5V, V_{BAT} = 3.6V, AC/USB = 1, MODE = 0, T_A = +25°C, unless otherwise specified. **(Continued)**

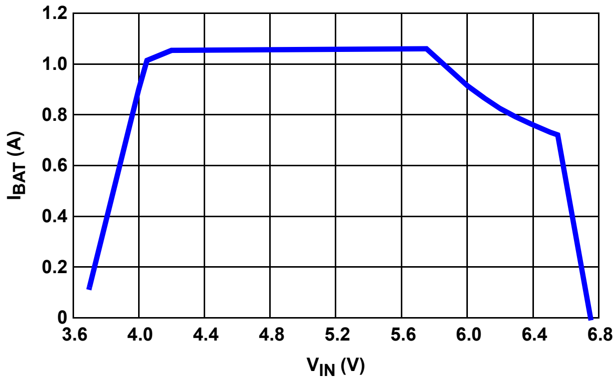


FIGURE 26. CHARGE CURRENT vs INPUT VOLTAGE

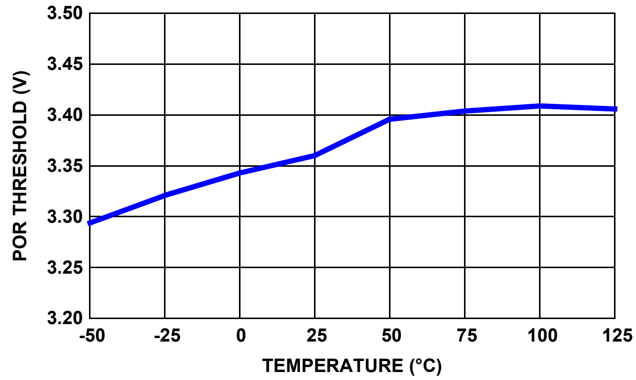


FIGURE 27. INPUT VOLTAGE POR THRESHOLD vs TEMPERATURE

Theory of Operation

When a valid input voltage is applied at VIN, the ISL9230 first regulates V_{OUT} at 3.4V or at VBAT plus 225mV, depending on the battery voltage. If the battery voltage is below 3.2V, the ISL9230 regulates V_{OUT} at 3.4V. If the battery voltage is higher than 3.2V, V_{OUT} will be regulated at VBAT plus 225mV. The charge current is also dependent on the battery voltage. When V_{BAT} is less than 3.0V, the ISL9230 trickle charges the battery at a reduced current, as specified in the "Electrical Specifications" table on page 5. Once V_{BAT} reaches 3.0V, the fast charge phase starts. When the system exceeds the maximum available current, either limited by the IC or by the input power supply, the charger FET Q2 is operated in a reverse mode, i.e. it provides battery current to the system instead of charging.

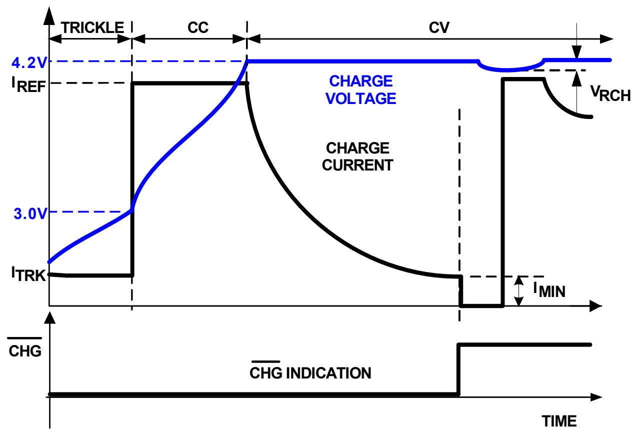


FIGURE 28. TYPICAL CHARGING CYCLE FOR CONT = L

The charger function is similar to other Li-ion battery chargers, i.e., it charges the battery at a constant current (CC) or a constant voltage (CV) depending on the battery terminal voltage. The constant current I_{REF} is set by the external resistor R_{IREF}. Depending on the combination of the AC/USB and the MODE pin status, the actual charge current may be reduced by the input current limit. When the battery voltage reaches the final voltage of 4.2V, the charger enters the CV mode and regulates the battery voltage at 4.2V to fully charge the battery without the risk of overcharging. Upon reaching an end-of-charge (EOC) current, the $\overline{CHG}$ will turn to high impedance to indicate a charge complete state and if CONT is low, Q2 will be turned off to terminate charging. Figure 28 shows the typical charge profile with the EOC/recharge events when CONT is low.

The EOC current level is internally set at 10% of the fast charge current as set by R_{IREF} for AC adapter input and USB500 input types. For USB100 input, the EOC current is set at 3.3% of the fast charge current as set by R_{IREF}. The $\overline{CHG}$ signal pulls low when the trickle charge starts and turns to high impedance at an EOC event.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically +125°C. This function guarantees safe operation when the printed-circuit board (PCB) is not capable of dissipating the heat generated by the linear charger.

The ISL9230 can withstand an input voltage up to 26V but will be disabled when the input voltage exceeds the OVP threshold, 6.6V typical, to protect against unqualified or faulty AC adapters.

$\overline{PG}$ Indication

The $\overline{PG}$ pin is an open-drain output to indicate the presence of a good supply voltage on the VIN pin. If V_{IN} is higher than the POR threshold and lower than the POR threshold, an internal open-drain FET is turned on. If V_{IN} suddenly falls below the POR falling threshold or rises above the OVP rising threshold, the open-drain FET will turn off. When turned on, the $\overline{PG}$ pin should be able to sink at least 5mA current under all operating conditions.

The $\overline{PG}$ pin can be used to drive a LED or to interface with a microprocessor.

Power-Good Range

The power-good range is defined by the following three conditions:

1. $V_{IN} > V_{POR}$
2. $V_{IN} - V_{OUT} > V_{OS}$
3. $V_{IN} < V_{OVP}$

where V_{OS} is the offset voltage between the input and charger output. The V_{OVP} is the overvoltage protection threshold given in the “Electrical Specifications” table on page 5. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis.

$\overline{CHG}$ Indication

The $\overline{CHG}$ is an open-drain output. The open drain FET turns on when the charger starts to charge and turns off when the EOC condition is qualified. Once the EOC condition is qualified, the $\overline{CHG}$ signal is latched in a Hi-Z state. The EOC condition is qualified when both of the following conditions are satisfied:

1. $V_{BAT} > V_{RCH}$
2. $I_{CHG} < I_{EOC}$

After being turned off, even if the battery is being automatically recharged later, the $\overline{CHG}$ indication will not be turned on again until one of the following events is encountered:

1. Input power being re-cycled
2. $\overline{CHGEN}$ signal being toggled
3. The battery is removed and re-inserted

The $\overline{CHG}$ signal can be interfaced either with a microprocessor GPIO or a LED for indication. A de-glitch delay of 25ms for both edges is implemented to prevent nuisance triggering during some short transient conditions.

Charge Termination, Recharge and Timeout

When an EOC condition is reached, the $\overline{CHG}$ pin changes to Hi-Z to indicate the end-of-charge condition and the charging is terminated if the CONT pin is in logic low. When a recharge condition is met, the safety timer will be reset to zero and the charging re-starts.

In the event a timeout interval has elapsed before the EOC condition is reached, a timeout fault condition is triggered. The timeout fault condition is indicated by the $\overline{CHG}$ pin being toggled between HI and LO every 0.5s. The timeout fault condition can be cleared by removing and reapplying the input power to the IC.

Under the EOC, timeout and timeout fault conditions, the power delivery to V_{OUT} is not impacted. The battery continues to supply current to VOUT if needed, as described in “Dynamic Power Path Management” on page 15.

The charge termination current is calculated as follows:

For AC or USB500 input:

$$I_{EOC} = 0.1XI_{CHG} \quad \text{(EQ. 5)}$$

USB100 input:

$$I_{EOC} = 0.033XI_{CHG} \quad \text{(EQ. 6)}$$

Where I_{CHG} is the fast charge current set by R_{IREF}.

Disabling The Charge Termination Option

The charge termination occurring when either $I_{CHG} < I_{EOC}$ or the safety timer times out can be overridden by asserting the CONT pin high. When CONT is high, the safety timers are suspended. The timers resume counting when the pin is pulled low. The EOC detection, $\overline{CHG}$ status is not affected by the state of the CONT pin, i.e. when $I_{CHG} < I_{EOC}$, the $\overline{CHG}$ will turn to high impedance regardless of the status of CONT.

ILIM Pin Function

The ILIM pin is provided to control the maximum current drawn by the ISL9230 at the VIN pin to supply the system and charge the battery. This enables the system designer to ensure that the IC does not draw more than the source can provide.

IREF Pin Function

The IREF pin has the two functions as described in the "Pin Descriptions" on page 4. The charge current can be programmed by the R_{IREF} over the range of 200mA to 1500mA for AC adapter input. The second function of the IREF pin is for monitoring the charge current by measuring the voltage at this pin, which is proportional to the charge current.

Dynamic Power Path Management

The power path management function of the ISL9230 controls the charge current and the system current when charging the battery with system load. The available input current, which is either limited by the ISL9230 or by the input power source, whichever is smaller, is properly split into two paths, one to the battery and the other to the system. The priority is given to the system. When the output voltage drops to the DPPM threshold, which is the regulated output voltage minus 100mV, the Dynamic Power Path Management (DPPM) starts to function. The DPPM control will first allocate the available current to satisfy the system need, using the remaining current to charge the battery. If the total available current is not enough to supply the system need, when the output voltage drops to 40mV below the battery voltage, the DPPM control will turn on the charge control FET, allowing the battery to supply current to the system load. Thus, when DPPM occurs, the battery may be charged at a current smaller than the programmed constant current.

Input DPM Mode (V_{IN}-DPM)

V_{IN}-DPM is a special feature that is designed for current-limited USB ports. V_{IN}-DPM is engaged when the ISL9230 is configured for USB100 (AC/USB = 0, MODE = 0) or USB500 (AC/USB = 0, MODE = 1) modes. During operation of V_{IN}-DPM, the input voltage is monitored and if VIN drops to the threshold of V_{IN}-DPM, the input current is reduced to keep the input voltage from dropping further. Therefore, the V_{IN}-DPM feature prevents the USB port from crashing.

Battery Presence and Short Circuit Detection

A current sink is used to detect if a battery has been installed or removed while power is applied to the VIN pin. A pulsed switch sinks a 7.5mA current from VBAT. If the voltage drops below VMIN (3.0V typ) within 250ms after the switch is on, it indicates the battery may have been removed. If V_{BAT} is above V_{MIN} after the sink test, a 7.5mA current is sourced into the battery for 250ms. If the voltage rises above V_{RCH}, this indicates a missing battery condition. If after these tests, the V_{BAT} voltage is within $V_{MIN} < V_{BAT} < V_{RECHG}$, it is determined that a battery has been installed, and charging is initiated.

Intelligent Timer

The internal timer in the ISL9230 provides a time reference for the maximum charge time limit. The nominal clock cycle for the reference time is set by the external resistor connected between the TIME pin and GND and is given by Equations 2 and 3.

The nominal maximum charge time interval is calculated based on the assumption that the programmed charge current is always available during the entire charging cycle. However, due to the PPM control, the current limit of the input source, or thermal foldback, the actual charge current maybe reduced during the constant current charge period. Under such conditions, the Intelligent Timer control will increase the timeout interval accordingly to allow approximately the same mAh product as the original timeout interval at the programmed current. The Intelligent Timer is suspended when CONT is asserted high.

Thermistor Interface

To ensure a safe charging temperature range, the ISL9230 incorporates a NTC pin to interface with the NTC thermistor in the battery pack to monitor the battery temperature. A constant current source is provided at this pin. The temperature range is determined by the external negative temperature coefficient (NTC) thermistor. The voltage thresholds and the current source value of the ISL9230 are optimized for the 103AT type industry standard thermister.

The ISL9230 uses a window comparator to set the valid temperature window. When the NTC pin voltage is out of the window anytime during charging, indicating either the temperature is too hot or too cold to charge, the ISL9230 stops charging. The $\overline{CHG}$, however will stay low to indicate a "charging" condition. When such an invalid temperature condition is encountered, the safety timer will stop counting. When the temperature returns to the set range, the charging resumes and the timer resumes counting from where it stopped.

When the CONT is high, the temperature sensing function can be disabled by pulling the NTC pin to a voltage level above the V_{DIS_NTC}, as shown on the “Electrical Specifications” table on page 7.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of +125°C. When thermal foldback is encountered, the charge current will be reduced to a value where the die temperature stops rising.

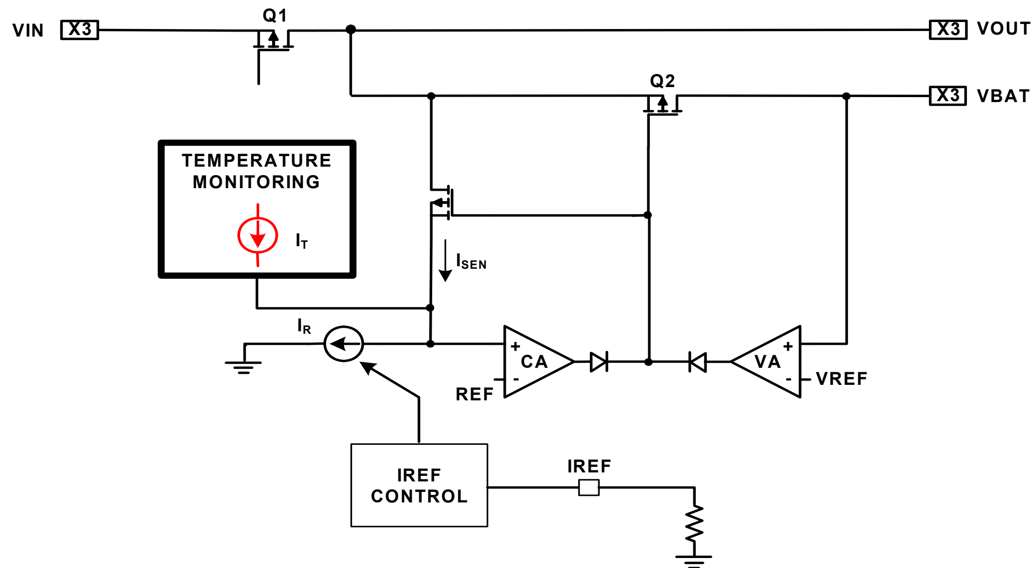


FIGURE 29. CHARGE CURRENT THERMAL FOLDBACK CONTROL

Figure 30 shows the thermal foldback concept whereas the current signals at the summing node of the current error amplifier CA are shown in Figure 29. I_R is the reference. I_T is the temperature tracking current generated from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately +125°C; then I_T starts to rise. In the meantime, as I_T rises, I_{SEN} will fall at the same rate (as the sum is a constant current I_R). As a result, the charging current, which is proportional to I_{SEN}, also decreases, keeping the die temperature constant at +125°C.

The system output current, however, is not impacted by the thermal foldback. Thus, when the charge current is reduced to zero, if the die temperature still rises, the IC will shut down at ~155°C to prevent damage to the IC.

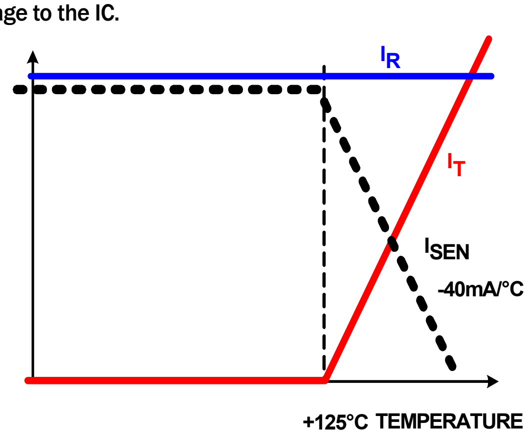


FIGURE 30. THERMAL FOLDBACK CONCEPT

Applications Information

Input Bypass Capacitor

The input capacitor is required to suppress the power supply transient response during transitions. Typically, a 10µF capacitor should be sufficient to suppress the power supply noise.

Due to the inductance of the power leads of the wall adapter or USB source, the input capacitor type must be properly selected to prevent high voltage transient during a hot-plug event. A tantalum capacitor is a good choice for its high ESR, providing damping to the voltage transient. Multi-layer ceramic capacitors, however, have a very low ESR and hence, when chosen as an input capacitor, a 1Ω series resistor must be used to provide adequate damping.

VOUT and VBAT Capacitor Selection

The criteria for selecting the capacitor at the VOUT and VBAT pins is to maintain the stability as well as to bypass any transient load current. The recommended capacitance is a 4.7µF X5R ceramic capacitor for VOUT and 1µF for VBAT. The actual capacitance connected to the output is dependent on the actual application requirement.

Layout Guidance

The ISL9230 uses a thermally-enhanced QFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much copper to the pad as possible. Typically, the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal vias.

Input Power Sources

The input power source is typically a well-regulated wall cube with 1m length wire or a USB port. The recommended input voltage ranges from 4.3V to 6.4V. The ISL9230 can withstand up to 26V on the input without damaging the IC. If the input voltage is higher than the OVP threshold, the IC is disabled.

State Diagram

The state diagram is shown in Figure 31. There are 15 states to cover all the operation modes, including the Power Down, Sleep, Standby, ILIM, IREF check, VOUT check, Idle, VBAT check, Trickle

Charge, CC/CV charge, Charge Complete, Batt Discharge, PPM, CV Charge, Charge Fault, Charge Complete, Battery Detect-1, Battery Detect-2, Battery Detect-3, Fault and Charging and Suspend states.

The IC flow chart starts by checking the voltage applied at VIN. If $V_{POR} < V_{IN} < V_{BAT} + V_{OS}$, the IC stays in the Sleep state. If $V_{BAT} + V_{OS} < V_{IN} < V_{OVP}$, the IC pulls the $\overline{\text{PG}}$ pin low and moves into the ILIM, IREF check state where the ILIM and IREF pins are being checked for short circuit condition. If there is no short at either pins, the regulator FET Q1 will regulate V_{OUT} with 100mA current limit. Following this, the IC moves to the V_{OUT} check state where V_{OUT} is checked for short circuit condition. If V_{OUT} is below 0.9V, indicating a V_{OUT} short condition, the IC will stay at the V_{OUT} check state. If V_{OUT} is above 0.9V, the IC will set the input current limit according to the setting on the AC/$\overline{\text{USB}}$ and the MODE pins. The IC then checks the status of the $\overline{\text{CHGEN}}$ pin.

If the $\overline{\text{CHGEN}}$ is low, the IC moves to the V_{BAT} short circuit check state where a 7.5mA current is sourced at the VBAT pin and the voltage is checked against the 1.8V threshold. If V_{BAT} is above 1.8V, the IC moves to the trickle charge state where the trickle charge timer starts, the charge current is set to I_{TRK} and $\overline{\text{CHG}}$ is turned on to indicate charging is in progress.

When V_{BAT} reaches the V_{MIN} threshold (3.0V typ), the fast charge starts where the charge current is set by R_{IREF} or by the IC's input current limit, whichever is smaller. When V_{BAT} reaches the V_{BAT} regulated voltage (4.2V typ), the charger moves to constant voltage mode where V_{BAT} is regulated at 4.2V. If the charge current drops to below the EOC threshold, the $\overline{\text{CHG}}$ turns off to indicate a charge complete condition. The charge current will be terminated if the CONT pin is at logic low status. Recharge will occur when V_{BAT} drops below the recharge threshold which is 100mV below the regulated VBAT voltage.

There are 3 scenarios for fast charge depending on the output current. When the sum of the output current and the fast charge current is smaller than the input current limit, the IC enters the Fast Charge state with the charge current set by R_{IREF}. When the sum of the output current and the fast charge current are greater than the input current limit, the IC will enter the DPPM mode, where the charging current is reduced to a point such that the sum of output current and the charging current equals to the input current limit. If the output current by itself is greater than the programmed input current limit, the IC enters the battery supplemental mode, where the battery is discharged to the system to aid in meeting the output demand.

The output voltage, depending on V_{BAT}, is regulated at either V_{BAT} + 225mV (when V_{BAT} >3.2V) or regulated at 3.4V (when V_{BAT} < 3.2V).

During the constant voltage mode, the output voltage is regulated at V_{BAT} + 225mV if the DPPM event is not encountered.

If the timeout limit is reached before reaching the Charge Complete state, the IC enters the Charger Fault state, where $\overline{\text{PG}}$ is LO, $\overline{\text{CHG}}$ is blinking once in 0.5S, V_{OUT} is regulated at 4.4V and the charger is OFF. This state is latched until the input power is removed and re-applied to start a new cycle.

At any time during the operation, if the die temperature reaches the OTP threshold, the IC will enter the OTP state, where $\overline{\text{PG}}$ is LO, $\overline{\text{CHG}}$ is HI, and the charger is OFF. VOUT is disconnected from VIN and connected to VBAT internally to maintain system power need.

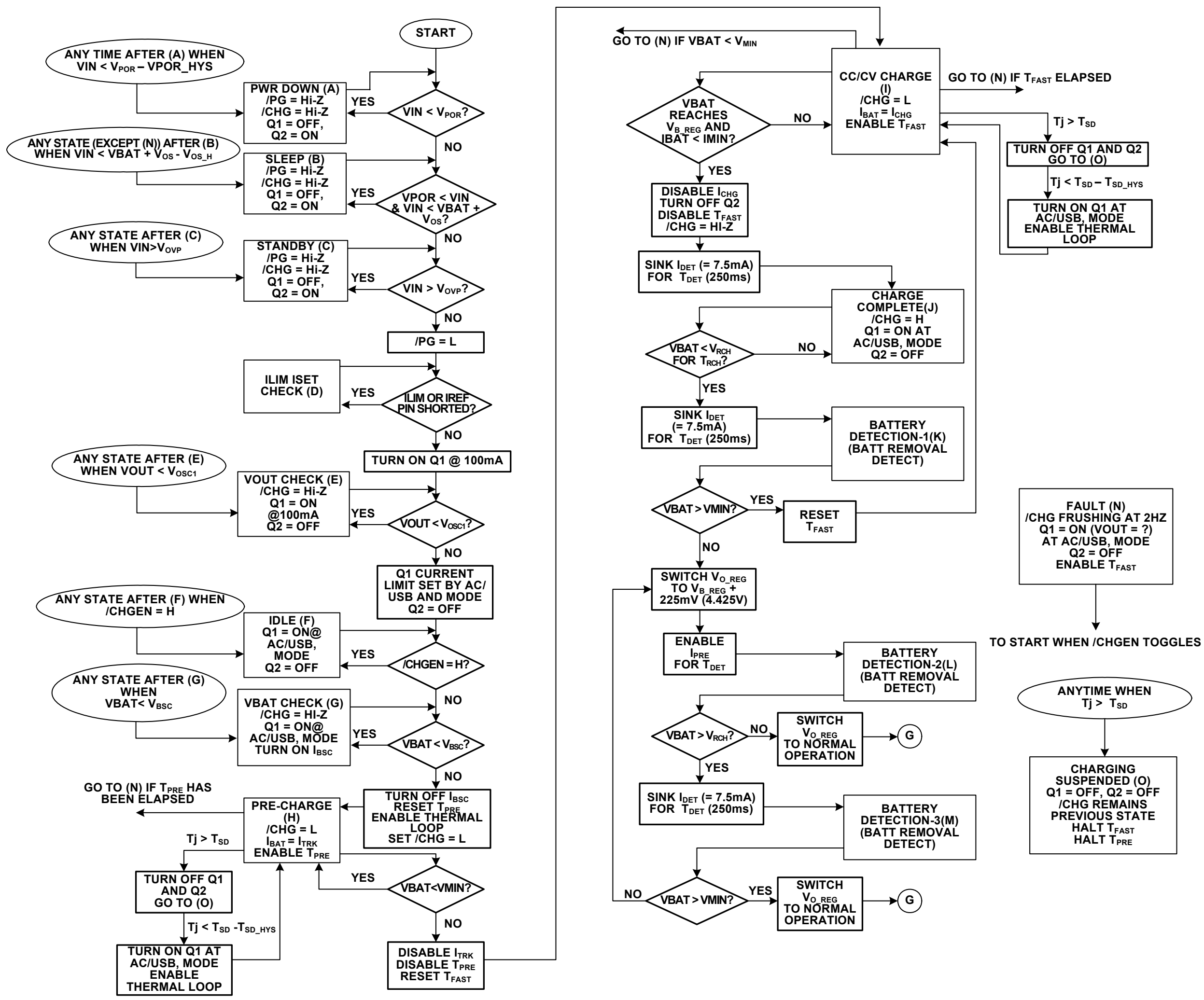


FIGURE 31. STATE DIAGRAM

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 12, 2011	FN7642.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL9230

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

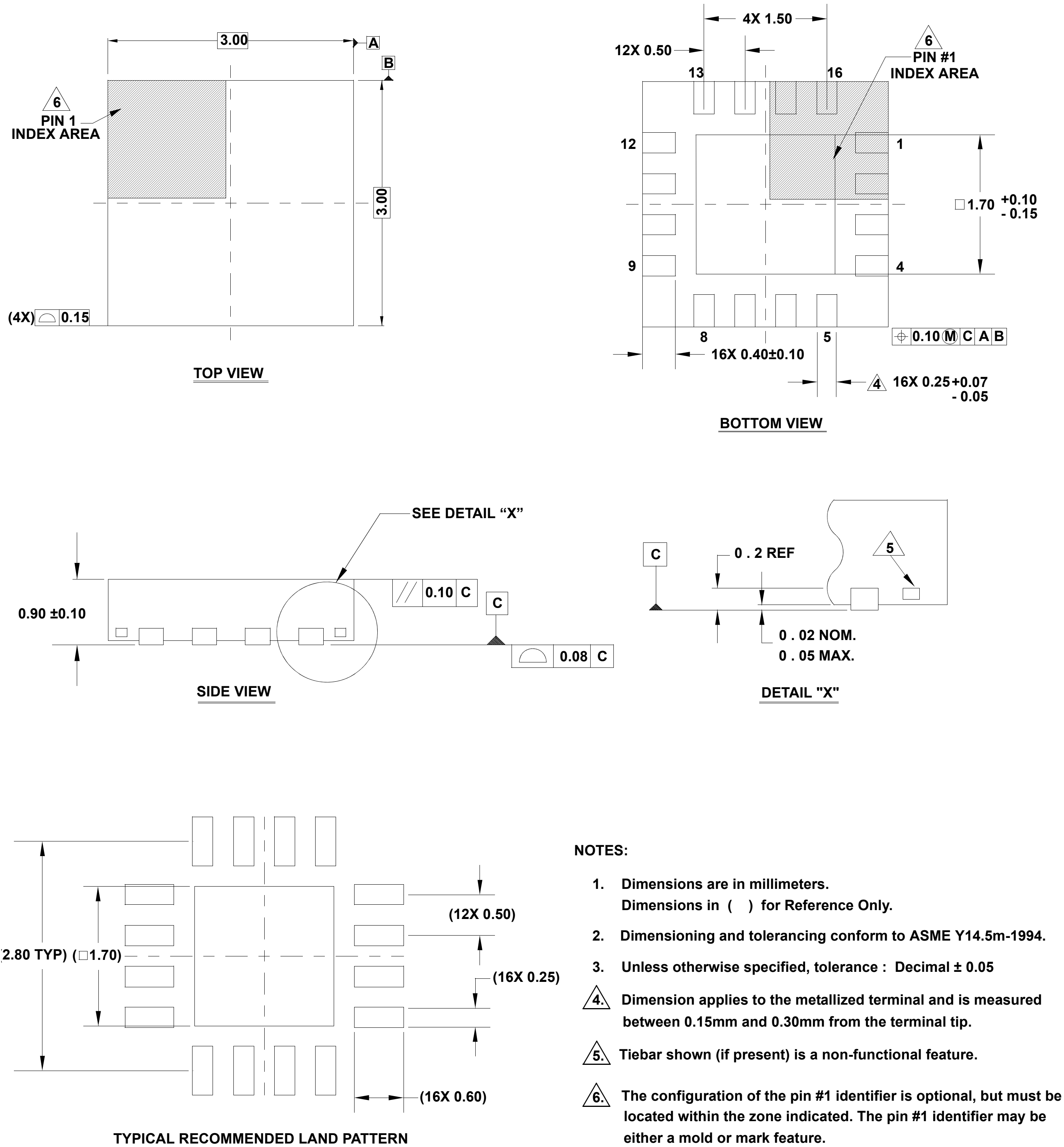
FITs are available from our website at: http://rel.intersil.com/reports/sear

Package Outline Drawing

L16.3x3E

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 3/11



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.