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Triple, 180° Out-of-Phase, Synchronous Step-Down PWM Controller

ISL9444

The ISL9444 is a triple-output synchronous buck controller that integrates three PWM controllers which are fully featured and designed to provide multi-rail power for use in products such as cable and satellite set-top boxes, VoIP gateways, cable modems, and other home connectivity products as well as a variety of industrial and general purpose applications. Each output is adjustable down to 0.7V. The PWMs are synchronized at 180° out-of-phase, thus reducing the input RMS current and ripple voltage.

The ISL9444 offers independent power-good indicators, programmable soft-start and tracking functions for ease of supply rail sequencing and integrated UV/OV/OC/OT protections in a space conscious 5mmx5mm QFN package.

Switching frequency can be set between 200kHz and 1200kHz using a resistor. The ISL9444 can be synchronized to another ISL9444 to reduce any beat frequency.

The ISL9444 utilizes internal loop compensation to keep minimum peripheral components for a compact design and a low total solution cost. These devices are implemented with current mode control with feed-forward to cover various applications even with fixed internal compensations.

Related Literature

- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages"

Features

- Three Integrated Synchronous Buck PWM Controllers
  - Internal Bootstrap Diodes
  - Independent Programmable Output Voltage
  - Independent Power-Good Indicators, Soft-Starting and Tracking
- Power Failure Monitor
- Light Load Efficiency Enhancement
  - Low Ripple Diode Emulation Mode with Pulse Skipping
- Supports Pre-Biased Output
- Programmable Frequency: 200kHz to 1200kHz
- Adaptive Shoot-through Protection
- Out-of-Phase Switching (0°/180°/0°)
- No External Current Sense Resistor
  - Uses Lower MOSFET's $r_{DS(ON)}$
- Complete Protection
  - Overcurrent, Overvoltage, Over-Temperature
- Wide Input Voltage Range: 4.5V to 26V
- Pb-Free (RoHS Compliant)

Applications

- VoX Gateway Devices
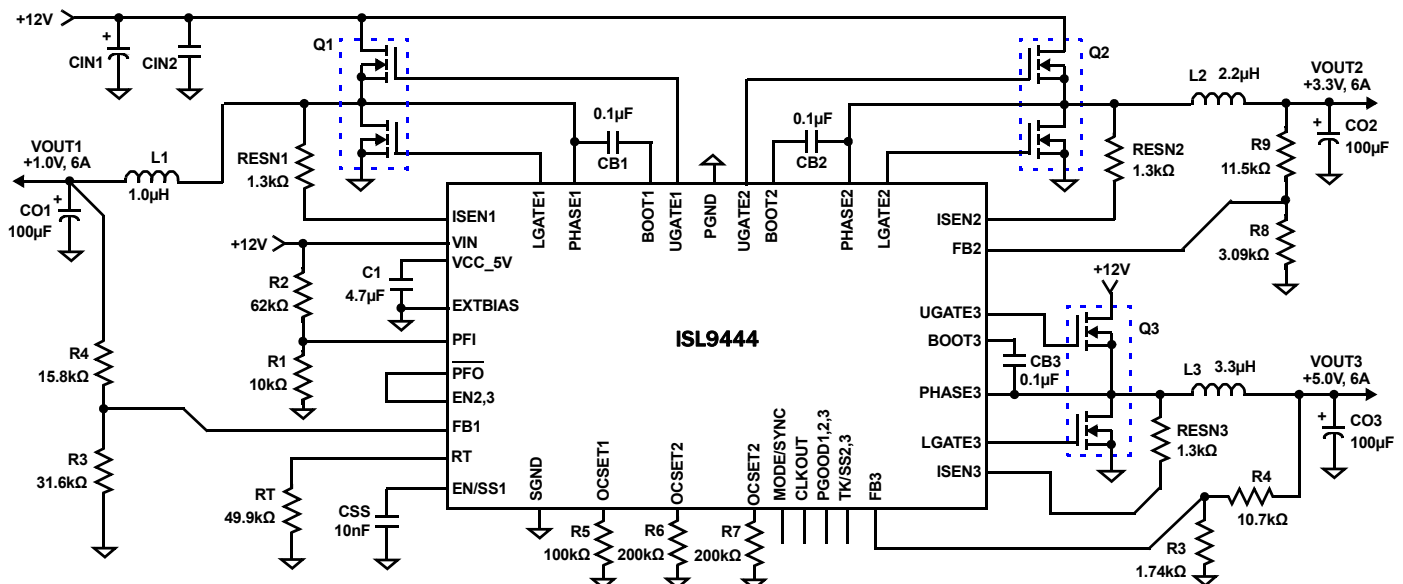- NAS/SAN Devices
- ATX Power Supplies
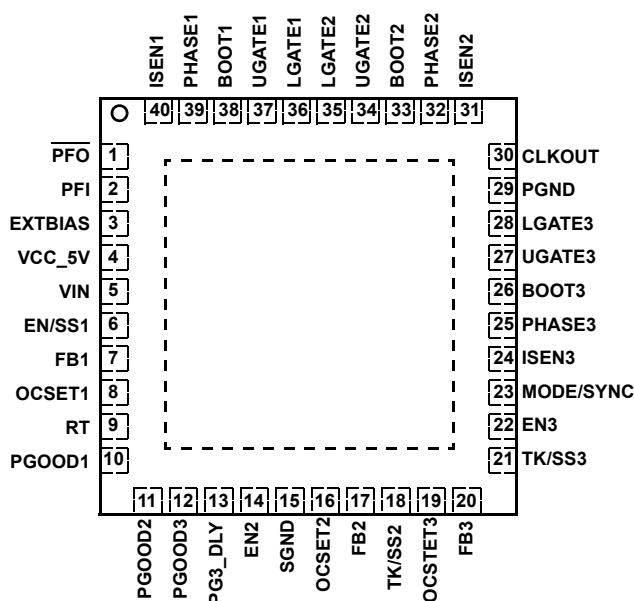

FIGURE 1. TYPICAL APPLICATION

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9444IRZ	ISL9444 IRZ	-40 to +85	40 Ld 5x5 QFN	L40.5X5B

NOTES:

1. Add "-T*" for tape and reel. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9444. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL9444
(40 LD 5x5 QFN)
TOP VIEW

Pin Descriptions

| PIN	NAME	FUNCTION
1	$\overline{PFO}$	Output of the auxiliary power monitor. $\overline{PFO}$ goes high if the voltage on PFI is greater than 1.2V (typical). Otherwise the $\overline{PFO}$ outputs low.
2	PFI	Input to the auxiliary power monitor. The internal threshold voltage is 1.2V (typical).
3	EXTBIAS	Input from an optional external 5V bias supply. There is an internal switch from this pin to VCC_5V. This switch closes and supplies the IC power, bypassing the internal linear regulator, when voltage at EXTBIAS is higher than 4.7V (typ). Do not allow voltage at the EXTBIAS pin to exceed VIN at any time. Decouple this pin to ground with a small ceramic capacitor (0.1µF to 1µF) when it is in use, otherwise tie this pin to ground. Do not float this pin.
4	VCC_5V	Output of the internal 5V linear regulator. This output supplies bias for the IC, the low side gate drivers, and the external boot circuitry for the high-side gate drivers. The VCC_5V pin must be always decoupled to power ground with a minimum of 4.7µF ceramic capacitor, placed very close to the pin. Do not allow the voltage at VCC_5V to exceed VIN at any time.
5	VIN	This pin should be tied to the input rail. It provides power to the internal linear drive circuitry and is also used by the feed-forward controller to adjust the amplitude of each PWM sawtooth. Decouple this pin with a small ceramic capacitor (0.1µF to 1µF) to ground.

Pin Descriptions (Continued)

| PIN	NAME	FUNCTION
6	EN/SS1	This pin provides an enable/disable function and soft-starting for PWM1 output. The output is disabled when the pin is pulled to GND. During start-up, a regulated 1.55µA soft-start current charges an external capacitor connected at this pin. When the voltage on the EN/SS1 pin reaches 1.3V, the PWM1 output becomes active. From 1.3V to 2.0V, the reference voltage of the PWM1 is clamped to the voltage at EN/SS1 minus 1.3V. The capacitance of the soft-start capacitors sets the soft-starting time and enable delay time. Setting the soft-starting time too short might create undesirable overshoot at the output during start-up. VCC_5V UVLO discharges the EN/SS1 via an internal MOSFET.
7	FB1	PWM1 feedback input. Connect FB1 to a resistive voltage divider from the output of PWM1 to GND to adjust the output voltage.
8	OCSET1	A resistor from this pin to ground adjusts the overcurrent threshold for PWM1.
9	RT	A resistor from this pin to ground adjusts the switching frequency from 200kHz to 1.2MHz. The switching frequency of the PWM controller is determined by the resistor, R_T, $$R_T = (23.36 \times (1.5 \times t_{SW} - 0.36)) \cdot k\Omega \qquad \text{(EQ. 1)}$$ where t_{SW} is the switching period in µs.
10	PGOOD1	Open drain logic output used to indicate the status of the PWM1 output voltage. This pin is pulled down when the PWM1 output is not within ±11% of the nominal voltage.
11	PGOOD2	Open drain logic output used to indicate the status of the PWM2 output voltage. This pin is pulled down when the PWM2 output is not within ±11% of the nominal voltage.
12	PGOOD3	Open drain logic output used to indicate the status of the PWM3 output voltage. This pin is pulled down when the PWM3 output is not within ±11% of the nominal voltage.
13	PG3_DLY	A capacitor connected between this pin and ground sets a delay between PWM3 output voltage reaching ±11% of regulation and PGOOD3 going high. There is no delay when PWM3 goes out of regulation and PGOOD3 is pulled low.
14	EN2	Enable/Disable input for PWM2. The output of PWM2 is enabled when this pin is pulled HIGH, and disabled when this pin is pulled LOW. PGOOD2 is pulled LOW 1µs after EN2 is pulled LOW. Do not leave this pin floating.
15	SGND	This is the small-signal ground common to all 3 controllers. It is suggested to route this separately from the high current ground (PGND). SGND and PGND can be tied together if there is one solid ground plane with no noisy currents around the chip. All voltage levels are measured with respect to this pin.
16	OCSET2	A resistor from this pin to ground adjusts the overcurrent threshold for PWM2.
17	FB2	PWM2 feedback input. Connect FB2 to a resistive voltage divider from the output of PWM2 to GND to adjust the output voltage.
18	TK/SS2	Dual function pin. The reference voltage of PWM2 is clamped to the voltage at TK/SS2 during start-up. When this pin is used for tracking, another channel is configured as the master and the output voltage of the master channel is applied to this pin via a resistor divider. When used for soft-starting control, a soft-start capacitor is connected from this pin to GND. A regulated 1.55µA soft-starting current charges up the soft-start capacitor. Value of the soft-start capacitor sets the PWM2 output voltage ramp.
19	OCSET3	A resistor from this pin to ground adjusts the overcurrent threshold for PWM3.
20	FB3	PWM3 feedback input. Connect FB3 to a resistive voltage divider from the output of PWM3 to GND to adjust the output voltage.
21	TK/SS3	Dual function pin. The reference voltage of PWM3 is clamped to the voltage at TK/SS3 during start-up. When this pin is used for tracking, another channel is configured as the master and the output voltage of the master channel is applied to this pin via a resistor divider. When used for soft-starting control, a soft-start capacitor is connected from this pin to GND. A regulated 1.55µA soft-starting current charges up the soft-start capacitor. Value of the soft-start capacitor sets the PWM3 output voltage ramp.
22	EN3	Enable/Disable input for PWM3. The output of PWM3 is enabled when this pin is pulled HIGH, and disabled when this pin is pulled LOW. PGOOD3 is pulled LOW 1µs after EN3 is pulled LOW. Do not leave this pin floating.
23	MODE/SYNC	Dual function pin. Tie this pin to ground or VCC_5V for light load operation mode selection. Connect this pin to ground to select Diode Emulation Mode with pulse skipping at light load. While connected to VCC_5V, the controllers operate in PWM Mode at light load. Connect this pin to CLKOUT of another ISL9444 or an external clock for synchronization. The controller operates in PWM at light load when synchronized with another ISL9444 or with an external clock.

Pin Descriptions (Continued)

| PIN	NAME	FUNCTION
24	ISEN3	Current signal input for PWM3. This pin is used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.
25	PHASE3	Phase node connection for PWM3. This pin is connected to the junction of the upper MOSFET's source, output filter inductor, and lower MOSFET's drain. PHASE3 is the internal lower supply rail for the UGATE3.
26	BOOT3	Bootstrap pin to provide bias for PWM3 high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. The bootstrap diodes are integrated to help reduce total cost and reduce layout complexity.
27	UGATE3	High-side MOSFET gate driver output for PWM3.
28	LGATE3	Low-side MOSFET gate driver output for PWM3.
29	PGND	Power ground connection for all three PWM channels. This pin should be connected to the sources of the lower MOSFETs and the (-) terminals of the external input capacitors
30	CLKOUT	Clock signal output. The frequency of the clock signal is two times of the ISL9444 switching frequency set by the resistor from RT to ground.
31	ISEN2	Current signal input for PWM2. This pin is used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.
32	PHASE2	Phase node connection for PWM2. This pin is connected to the junction of the upper MOSFET's source, output filter inductor, and lower MOSFET's drain. PHASE2 is the internal lower supply rail for the UGATE2.
33	BOOT2	Bootstrap pin to provide bias for PWM2 high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. The bootstrap diodes are integrated to help reduce total cost and reduce layout complexity.
34	UGATE2	High-side MOSFET gate driver output for PWM2.
35	LGATE2	Low-side MOSFET gate driver output for PWM2.
36	LGATE1	Low-side MOSFET gate driver output for PWM1.
37	UGATE1	High-side MOSFET gate driver output for PWM1.
38	BOOT1	Bootstrap pin to provide bias for PWM1 high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. The bootstrap diodes are integrated to help reduce total cost and reduce layout complexity.
39	PHASE1	Phase node connection for PWM1. This pin is connected to the junction of the upper MOSFET's source, output filter inductor, and lower MOSFET's drain. PHASE1 is the internal lower supply rail for the UGATE1.
40	ISEN1	Current signal input for PWM1. This pin is used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.
-	EPAD	EPAD at ground potential. Solder it directly to GND plane for better thermal performance.

Block Diagram
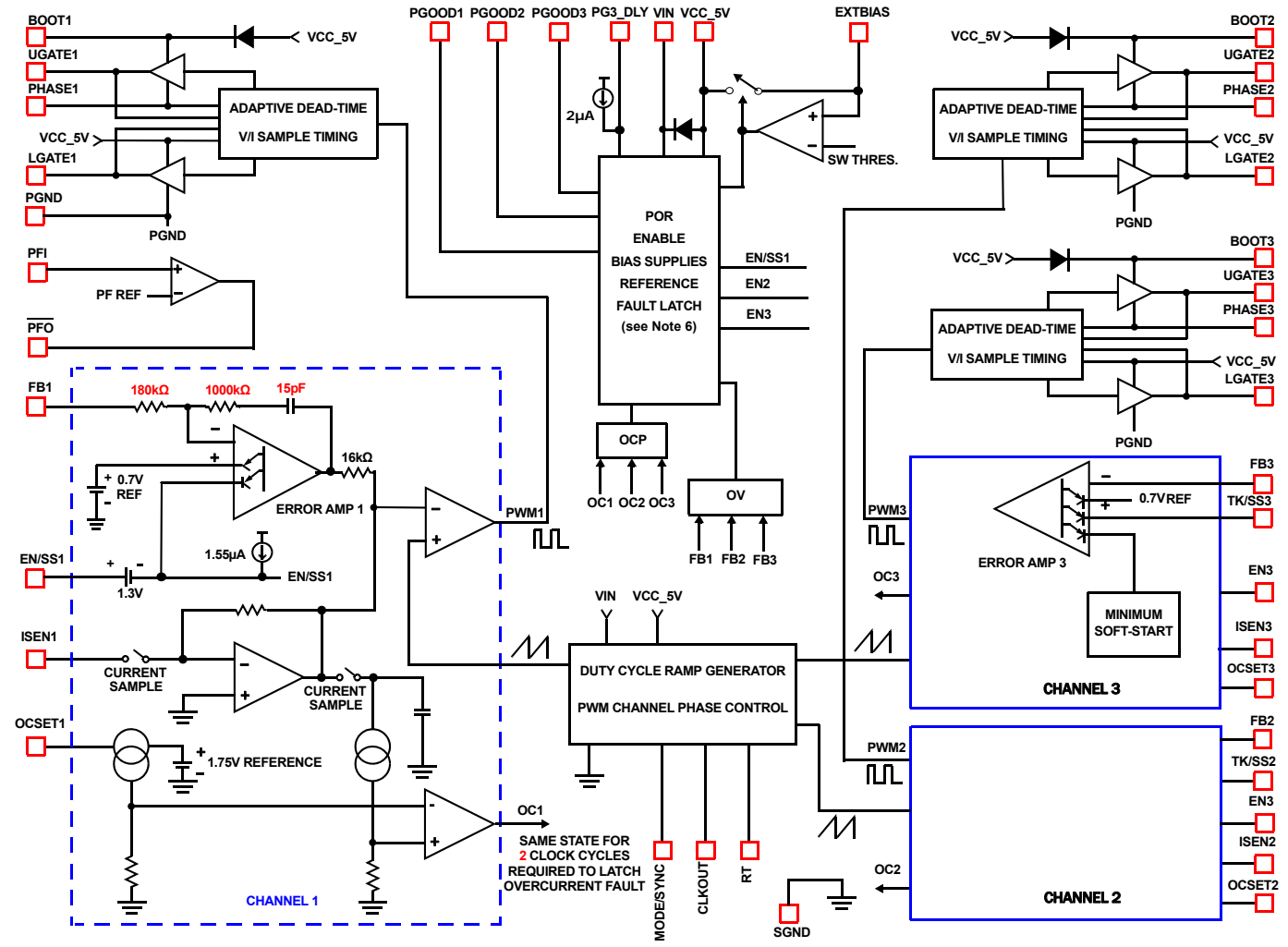
ISL9444

Typical Application - ISL9444
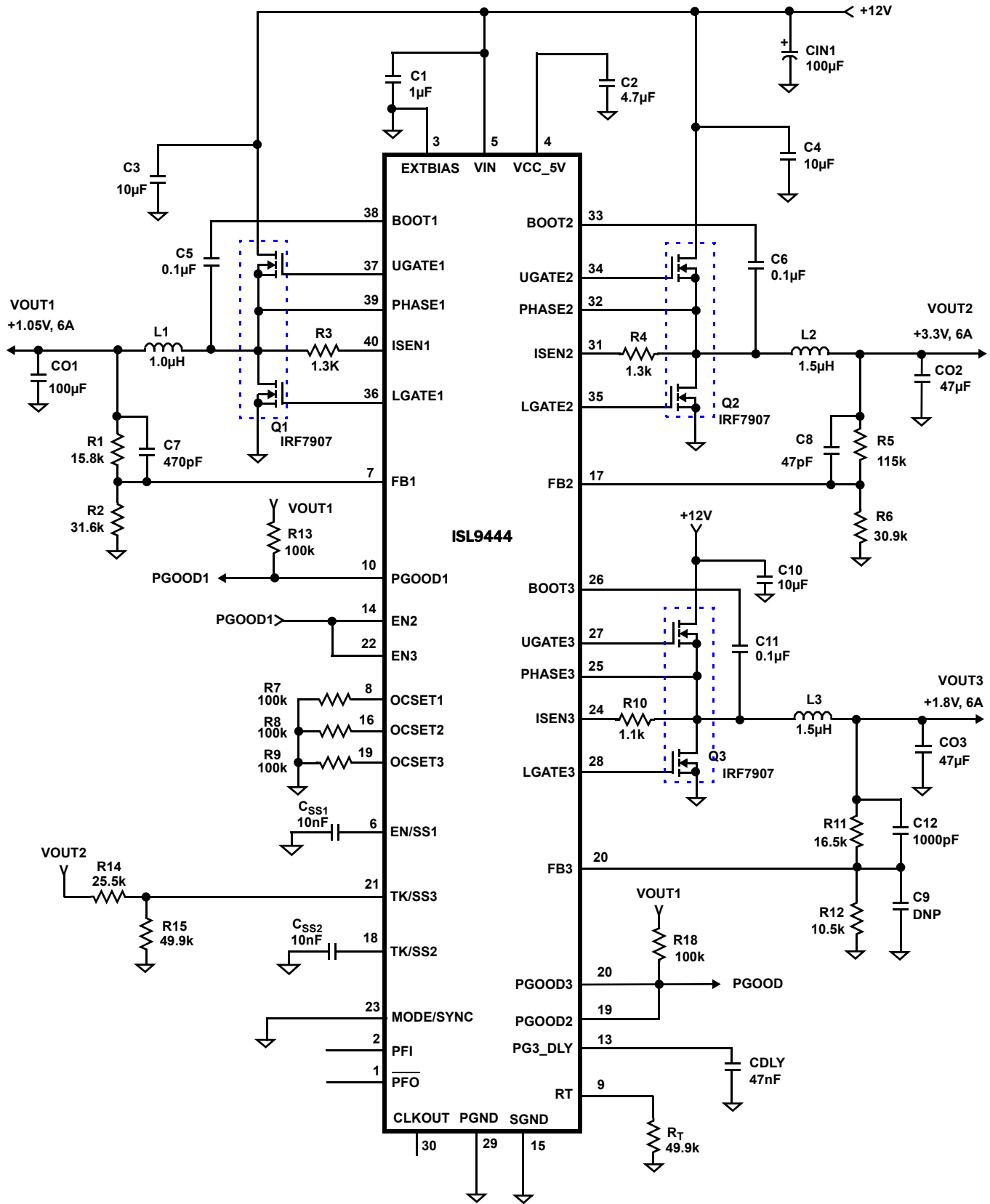
Typical Application - ISL9444
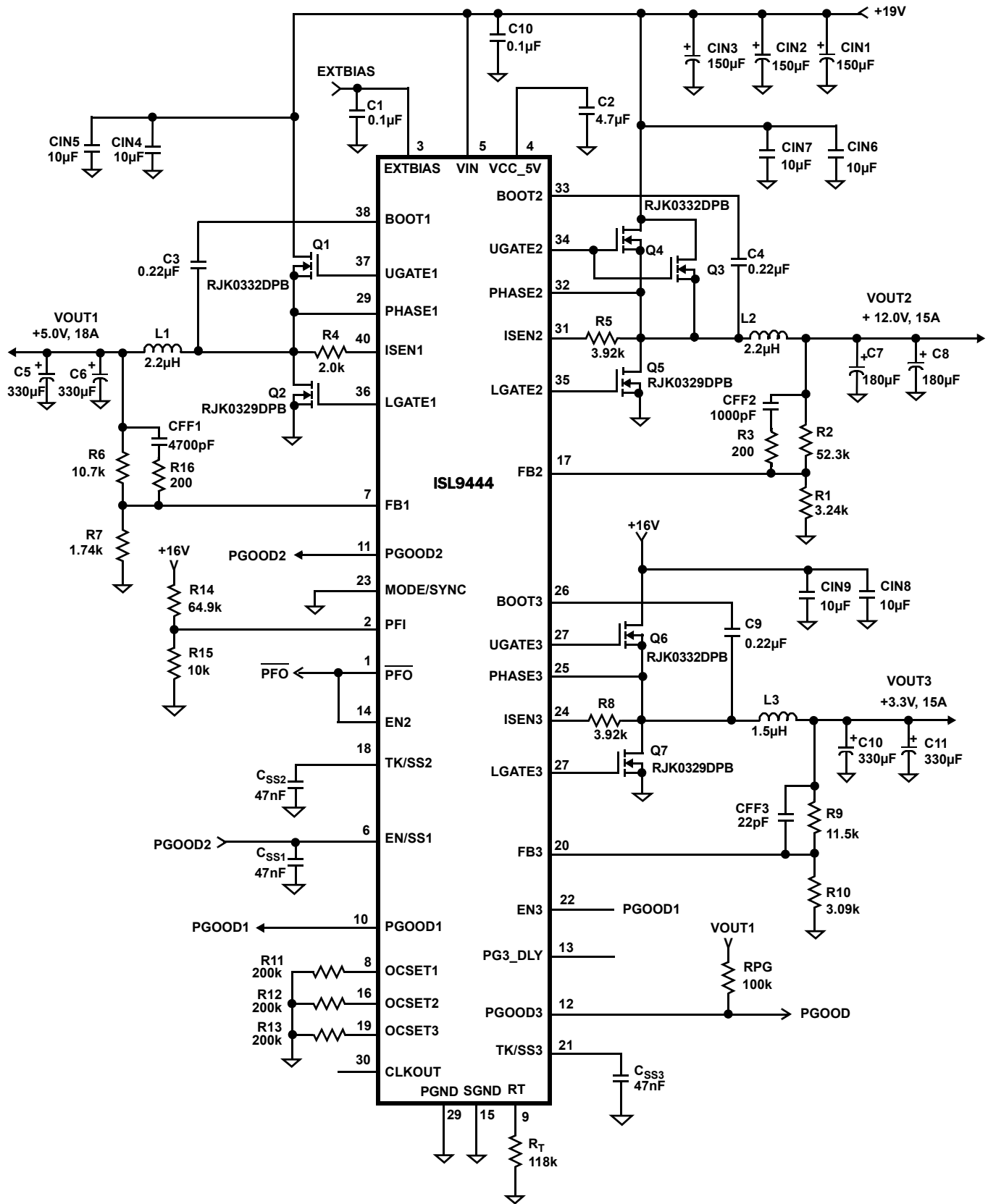
VOUT1 can be connected to EXTBIAS for lower IC power dissipation and IC self-bias.
Care must be taken to ensure VIN does not drop below EXTBIAS.

External boot diode may be added for PWM2.

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ISL9444

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Absolute Maximum Ratings

VCC_5V to GND . . . . -0.3V to +6.2V
EXTBIAS to GND . . . . -0.3V to VCC_5V+0.3V
VIN to GND. . . . .-0.3V to +30V
BOOT1,2,3/UGATE1,2,3 to PHASE1,2,3 . . . . -0.3V to VCC_5V+0.3V
PHASE1,2,3 and
    ISEN1, 2,3, to GND. . . . . -5V (<100ns, 10µJ)/-0.3V (DC) to +28V
EN/SS1, EN2, EN3, FB1, FB2, FB3, to GND . . . . . . -0.3V to VCC_5V+0.3V
OCSET1, OCSET2, OCSET3, PG3_DLY, TKSS2, TKSS3, CLKOUT,
    LGATE1, LGATE2, LGATE3, to GND . . . . -0.3V to VCC_5V+0.3V
RT, MODE/SYNC to GND . . . . -0.3V to VCC_5V+0.3V
PFI, PFO, PGOOD1, 2, 3, to GND. . . . . -0.3V to VCC_5V+0.3V
VCC_5V Short Circuit to GND Duration. 1s
ESD Rating
    Human Body Model (Tested per JESD22-A114F). 3000V
    Machine Model (Tested per JESD22-115-C) 200V
    Charge Device Model (Tested per JESD22-C110D) 2000V
Latch Up (Tested per JESD78C; Class II, Level A, +85°C) 100mA

Thermal Information

Thermal Resistance (Typical) θ_{JA}(°C/W) θ_{JC}(°C/W)
    40 Ld QFN Package (Notes 4, 5)   30   2.5
Maximum Junction Temperature . . . .-55°C to +150°C
Maximum Operating Temperature. . . . .-40°C to +85°C
Maximum Storage Temperature. . . . .-65°C to +150°C
Pb-free reflow profile . . . . see link below
    http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . .-40°C to +85°C
Supply Voltage . . . . 4.5V to 28V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram on page 5 and Typical Application Schematics on pages 6 and 7. V_{IN} = 5.0V to 28V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
V_IN SUPPLY						
V_{IN}	Input Voltage Range		**4.5**	12.0	**28.0**	V
V_IN SUPPLY CURRENT						
I_{VINQ}	Shutdown Current (Note 7)	EN/SS1 = EN2 = EN3 = 0 PGOODx are floating		32	**40**	µA
I_{VINOP}	Operating Current (Note 8)	PGOOD1, PGOOD2, PGOOD3 are floating		5	**6**	mA
VCC_5V SUPPLY (Note 6)						
V_{CC}	Operation Voltage	V_{IN} = 12V, I_L = 0mA	**5.1**	5.4	**5.7**	V
	Internal LDO Output Voltage	V_{IN} = 4.5V, I_L = 30mA	**4.05**	4.35		V
	Internal LDO Output Voltage	V_{IN} > 5.6V, I_L = 75mA	**4.5**	5.4		V
I_{VCC_MAX}	Maximum Supply Current of Internal LDO	V_{VCC_5V} = 0V, V_{IN} = 12V		150	**250**	mA
EXTBIAS SUPPLY (Note 6)						
V_{EXT_THR}	Switch Over Threshold Voltage, Rising	EXTBIAS Voltage	**4.5**	4.7	**4.9**	V
V_{EXT_THF}	Switch Over Threshold Voltage, Falling	EXTBIAS Voltage	**4.35**	4.5	**4.65**	V
R_{EXT}	Internal Switch On Resistance	V_{IN} = 12V		0.5	**1.0**	Ω
UNDERVOLTAGE LOCKOUT						
$V_{UVLOTHR}$	Undervoltage Lockout, Rising	VCC_5V Voltage	**3.4**	3.95	**4.45**	V
$V_{UVLOTHF}$	Undervoltage Lockout, Falling	VCC_5V Voltage	**3.05**	3.60	**4.15**	V
EN/SS1, EN2, EN3 THRESHOLD						
V_{ENSS_TH}	EN/SS1 THRESHOLD		**1.10**	1.30	**1.5**	V
V_{EN_THR}	EN2, EN3 Logic Threshold, Rising		**1.40**	1.7	**2.00**	V
V_{EN_THF}	EN2, EN3 Logic Threshold, Falling		**1.10**	1.25	**1.40**	V

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Electrical Specifications
Recommended operating conditions unless otherwise noted. Refer to Block Diagram on page 5 and Typical Application Schematics on pages 6 and 7. V_{IN} = 5.0V to 28V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
SOFT-START CURRENT						
I_{SS}	EN/SS1, TK/SSx Soft-Start Charge Current	VEN/SS1 = VTK/SSx = 0V	**1.05**	1.55	**2.05**	µA
DEFAULT INTERNAL MINIMUM SOFT-STARTING						
t_{SS_MIN}	Default Internal Output Ramping Time		**1.3**	2.1	**2.9**	ms
POWER-FAIL MONITOR						
V_{PFI_REF}	PFI Input Threshold Voltage, Rising		**1.16**	1.22	**1.28**	V
V_{PFI_FAL}	PFI Input Threshold Voltage, Falling		**1.05**	1.12	**1.19**	V
V_{PFO_L}	$\overline{PFO}$ Output Voltage Low	I_SINK = 1mA			0.3	V
V_{PFO_H}	$\overline{PFO}$ Output Voltage High	I_SOURCE = 1mA	**VCC_5V -0.3**			V
POWER-GOOD MONITORS						
V_{PGOV}	PGOODx Upper Threshold, PWM 1, 2 and 3		**105.5**	111	**115.5**	%
V_{PGUV}	PGOODx Lower Threshold, PWM 1, 2 and 3		**85**	89	**94**	%
V_{PGLOW}	PGOODx Low Level Voltage	I_SINK = 2mA			0.3	V
I_{PGLKG}	PGOODx Leakage Current	PGOODx = 5V		1	**150**	nA
	PGOOD Rise Time	RPULLUP = 10k to 3.3V		0.05		µs
	PGOOD Fall Time	RPULLUP = 10k to 3.3V		0.05		µs
PGOOD1, PGOOD2 TIMING						
t_{PGR}	VOUT Rising Threshold to PGOOD Rising		**0.7**	1.1	**1.5**	ms
t_{PGF}	VOUT Falling Threshold to PGOOD Falling		**40**	75	**110**	µs
	EN2, EN3 Falling Threshold to PGOOD Falling			1.2	**1.7**	µs
PGOOD3 TIMING						
	PG3_DLY Charge Current	V_{PG3_DLY} = 1.2V	**1.2**	1.9	**2.6**	µA
	PG3_DLY Threshold Voltage (Note 9)		**1.16**	1.195	**1.23**	V
REFERENCE SECTION						
V_{REF}	Internal Reference Voltage			0.700		V
	Reference Voltage Accuracy	T_A = 0°C to +85°C	-1.0		+1.0	%
		T_A = -40°C to +85°C	**-1.15**		+1.0	%
I_{FBLKG}	FB Bias Current (Note 9)				**100**	nA
PWM CONTROLLER ERROR AMPLIFIERS						
	DC Gain (Note 9)			88		dB
GBW	Gain-BW Product (Note 9)			15		MHz
SR	Slew Rate (Note 9)			2.0		V/µs
PWM REGULATOR						
t_{OFF_MIN}	Minimum Off Time	RFS = 169kΩ	**95**	125	**155**	ns
DV_{RAMP}	Peak-to-Peak Saw-tooth Amplitude (Note 9)	V_{IN} = 12V		1.2		V
		V_{IN} = 5.0V		0.55		V
	Ramp Offset			1		V

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Electrical Specifications
Recommended operating conditions unless otherwise noted. Refer to Block Diagram on page 5 and Typical Application Schematics on pages 6 and 7. V_{IN} = 5.0V to 28V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
SWITCHING FREQUENCY (Note 9)						
F_{SW}	Switching Frequency	R_T = 20.5kΩ	**1080**	1200	**1320**	kHz
	Switching Frequency	R_T = 169kΩ	**168**	198	**228**	kHz
	Switching Frequency	R_T = 49.9kΩ	**540**	600	**660**	kHz
V_{RT}	RT Voltage	R_T = 49.9kΩ	**485**	500	**515**	mV
CLOCK OUTPUT AND SYNCHRONIZATION						
V_{CLKH}	CLKOUT Output High	ISOURCE = 1mA	**VCC_5V - 0.3**			V
V_{CLKL}	CLKOUT Output Low	ISINK = 1mA			**0.3**	V
F_{CLK}	CLKOUT Frequency	R_T = VCC_5V	**1080**	1200	**1320**	kHz
F_{SYNC}	SYNC Synchronization Range	R_T = 49.9kΩ	**1020**		**1380**	kHz
LIGHT LOAD EFFICIENCY MODE						
$V_{MODETHH}$	MODE/SYNC Threshold High		**1.3**	1.6	**1.9**	V
$V_{MODETHL}$	MODE/SYNC Threshold Low		**1.1**	1.4	**1.7**	V
V_{CROSS}	Diode Emulaton Phase Threshold (Note 11)	V_{IN} = 12V		-3		mV
PWM GATE DRIVER (Note 9)						
I_{GSRC}	Source Current			800		mA
I_{GSNK}	Sink Current			2000		mA
R_{UG_UP}	Upper Drive Pull-Up	VCC_5V = 5.0V		1.5	**3**	Ω
R_{UG_DN}	Upper Drive Pull-Down	VCC_5V = 5.0V		1.1	**2.5**	Ω
R_{LG_UP}	Lower Drive Pull-Up	VCC_5V = 5.0V		1.5	**3**	Ω
R_{LG_DN}	Lower Drive Pull-Down	VCC_5V = 5.0V		0.6	**1.5**	Ω
t_{GR}	Rise Time	C_{OUT} = 1000pF		8		ns
t_{GF}	Fall Time	C_{OUT} = 1000pF		10		ns
OVERVOLTAGE PROTECTION						
V_{OVTH}	OV Trip Point		**114.5**	118.5	**123.5**	%
OVERCURRENT PROTECTION						
I_{OCSET}	Overcurrent Threshold (OCSET_) (Note 10)	ROCSET = 55kΩ		32		µA
	Full Scale Input Current (ISEN_) (Note 10)			15		µA
V_{OCSET}	Overcurrent Set Voltage (OCSET_)		**1.67**	1.74	**1.81**	V
OVER-TEMPERATURE (Note 9)						
T_{OT-TH}	Over-Temperature Shutdown			150		°C
T_{OT-HYS}	Over-Temperature Hysteresis			15		°C

NOTES:

6. In normal operation, where the device is supplied with voltage on the VIN pin, the VCC_5V pin provides a 5V output capable of 75mA (min). When the VCC_5V pin is connected to external 5V supply, the internal LDO regulator is disabled. The voltage at VCC_5V should not exceed the voltage at VIN at any time. (Refer to the"Pin Descriptions" on page 2 for more details.)

7. This is the total shutdown current with V_{IN} = 5.6V and 26V.

8. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

10. Check Note 6 for VCC_5V and VIN configurations.

11. Threshold voltage at PHASE1, PHASE2 and PHASE3 pins for turning off the bottom MOSFET during DEM.

Typical Performance Curves of ISL9444 Oscilloscope plots are taken using the ISL9444EVAL1Z

Evaluation Board, V_{IN} = 12V, VOUT1 = 1.05V, VOUT2 = 3.3V, VOUT3 = 1.8V unless otherwise noted.
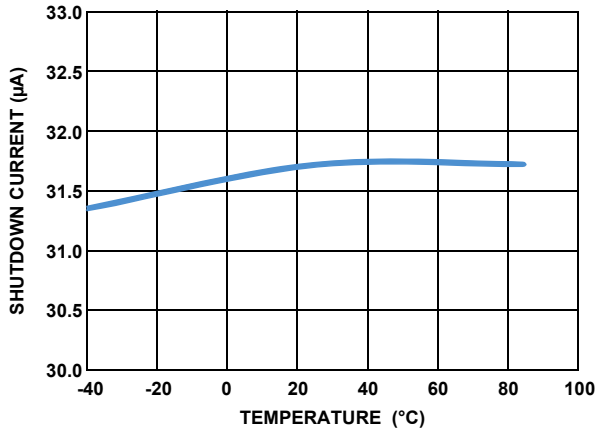

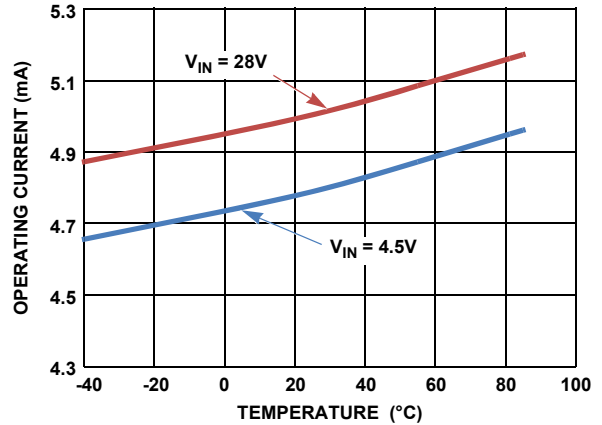FIGURE 2. SHUTDOWN CURRENT vs TEMPERATURE
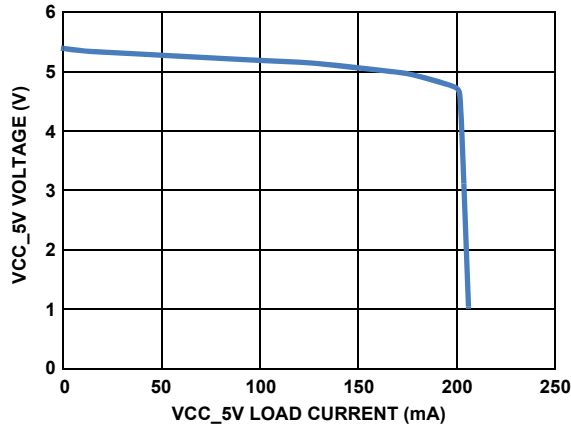

FIGURE 3. QUIESCENT CURRENT vs TEMPERATURE
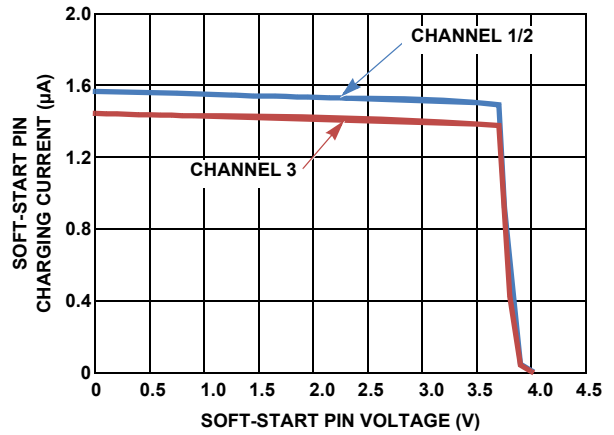

FIGURE 4. VCC_5V vs LOAD REGULATION

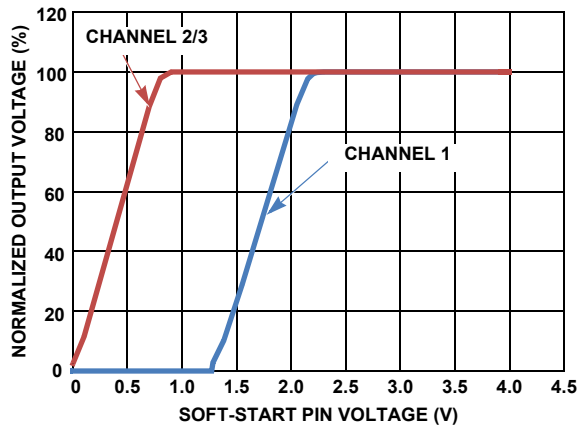FIGURE 5. SOFT-START PIN CHARGING CURRENT vs VOLTAGE ON SOFT-START PIN

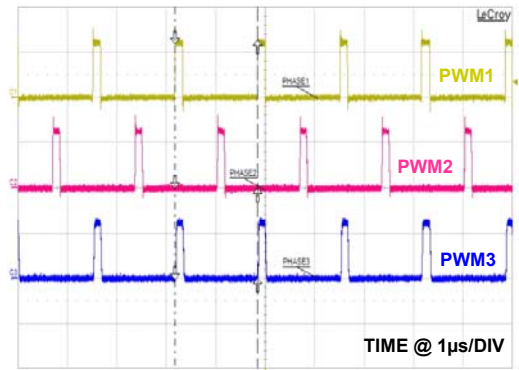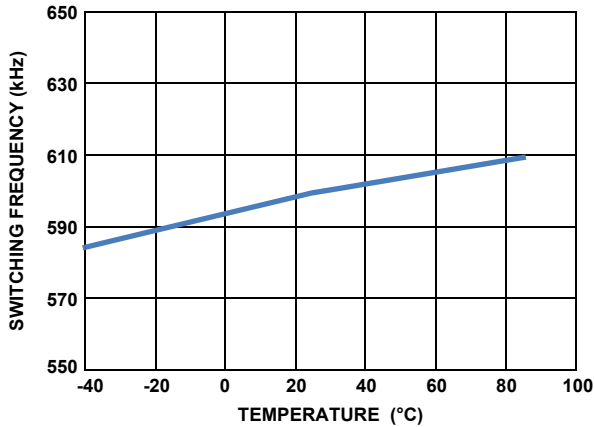FIGURE 6. NORMALIZED OUTPUT VOLTAGE vs VOLTAGE ON SOFT-START PIN

FIGURE 7. PHASE NODE WAVEFORMS. ALL OUTPUT VOLTAGES SET AT 1.05V

Typical Performance Curves of ISL9444 Oscilloscope plots are taken using the ISL9444EVAL1Z

Evaluation Board, V_{IN} = 12V, VOUT1 = 1.05V, VOUT2 = 3.3V, VOUT3 = 1.8V unless otherwise noted. **(Continued)**

FIGURE 8. SWITCHING FREQUENCY vs TEMPERATURE (R_T = 49.9kΩ)
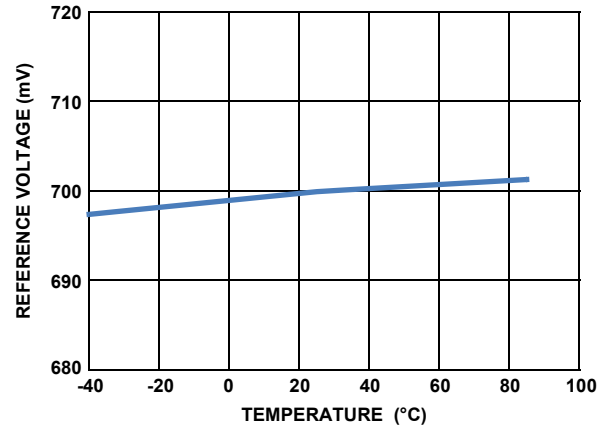
FIGURE 9. REFERENCE VOLTAGE vs TEMPERATURE
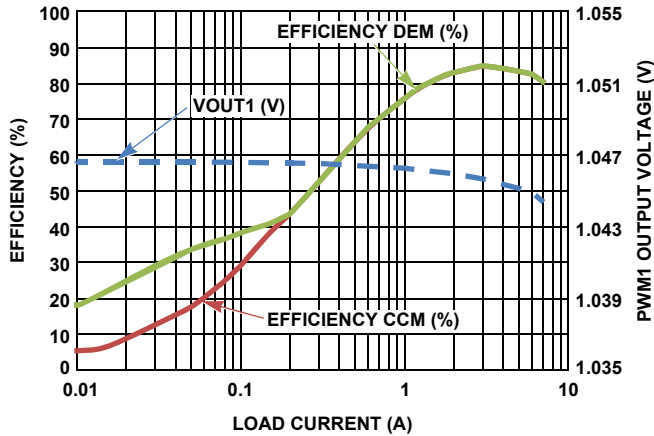
FIGURE 10. PWM1 EFFICIENCY AND LOAD REGULATION
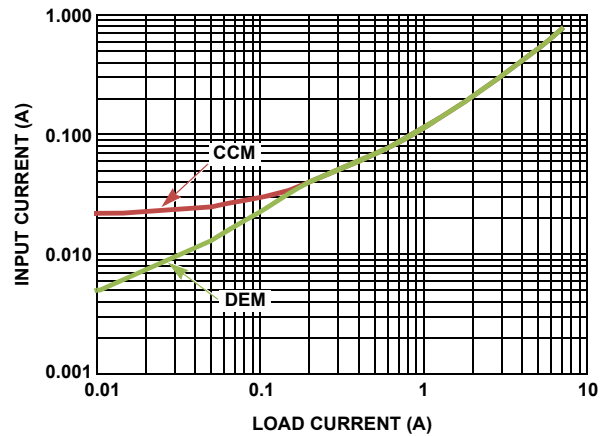
FIGURE 11. PWM1 INPUT CURRENT COMPARISON WITH MODE = CCM/DEM
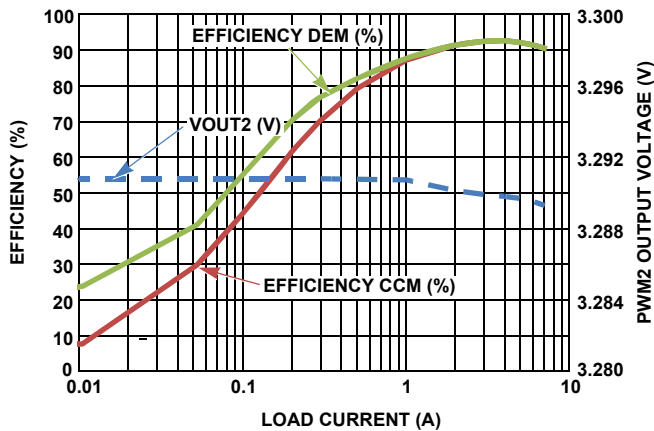
FIGURE 12. PWM2 EFFICIENCY AND LOAD REGULATION
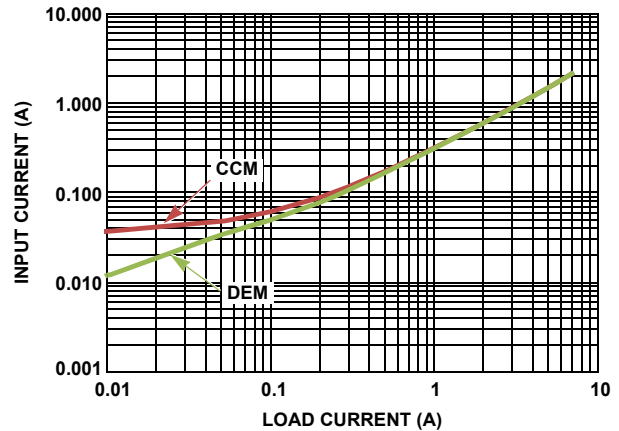
FIGURE 13. PWM2 INPUT CURRENT COMPARISON WITH MODE = CCM/DEM

Typical Performance Curves of ISL9444 Oscilloscope plots are taken using the ISL9444EVAL1Z

Evaluation Board, V_{IN} = 12V, VOUT1 = 1.05V, VOUT2 = 3.3V, VOUT3 = 1.8V unless otherwise noted. **(Continued)**
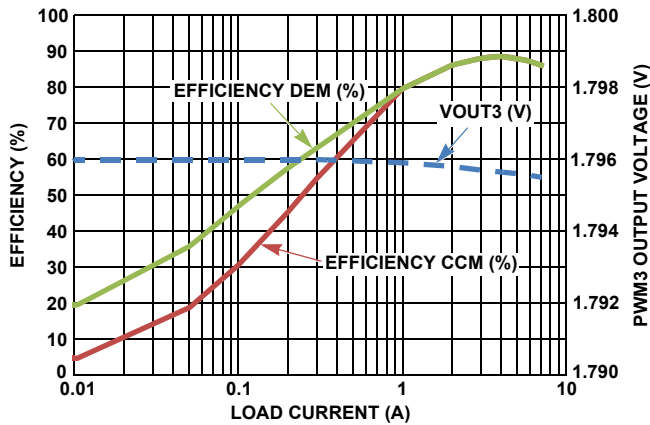
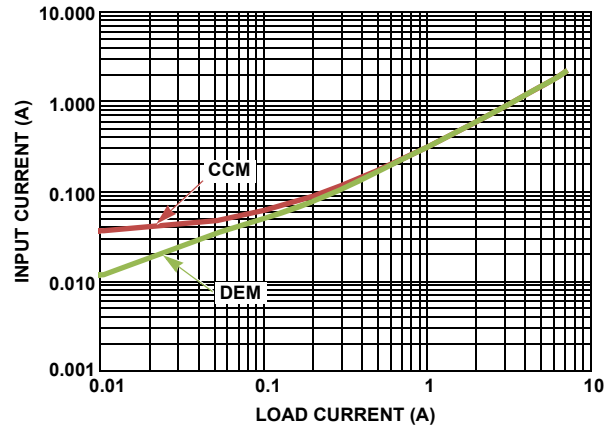FIGURE 14. PWM3 EFFICIENCY AND LOAD REGULATION

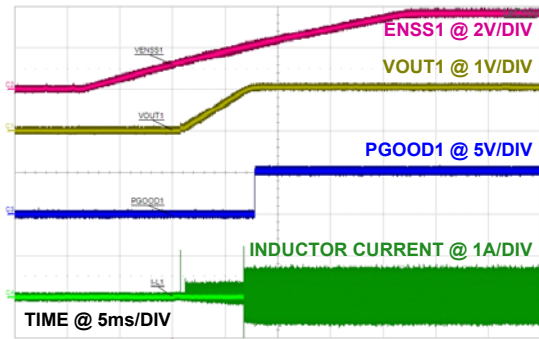FIGURE 15. PWM3 INPUT CURRENT COMPARISON WITH MODE = CCM/DEM

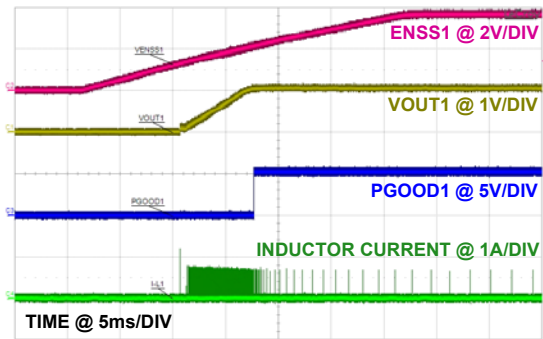FIGURE 16. PWM1 START-UP. MODE = CCM, LOAD = 0A

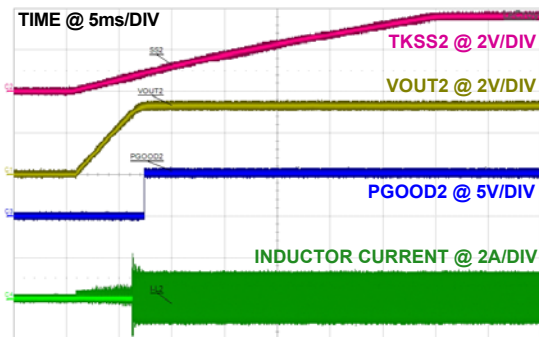FIGURE 17. PWM1 START-UP. MODE = DEM, LOAD = 0A

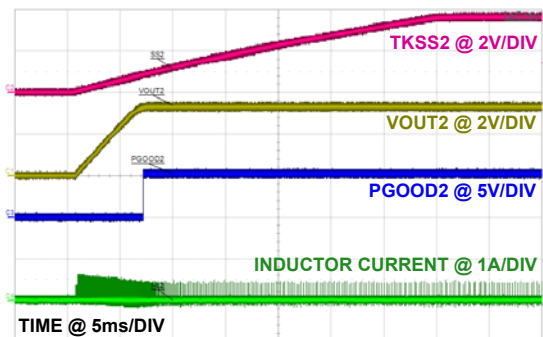FIGURE 18. PWM2 START-UP. MODE = CCM, LOAD = 0A

FIGURE 19. PWM2 START-UP. MODE = DEM, LOAD = 0A

Typical Performance Curves of ISL9444 Oscilloscope plots are taken using the ISL9444EVAL1Z

Evaluation Board, V_{IN} = 12V, VOUT1 = 1.05V, VOUT2 = 3.3V, VOUT3 = 1.8V unless otherwise noted. **(Continued)**
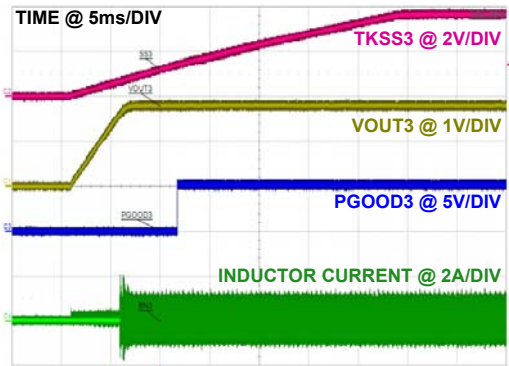
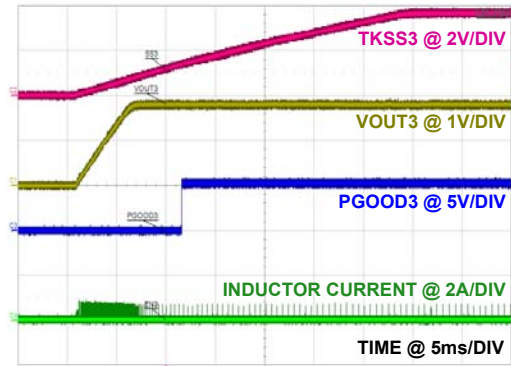FIGURE 20. PWM3 START-UP. MODE = CCM, LOAD = 0A
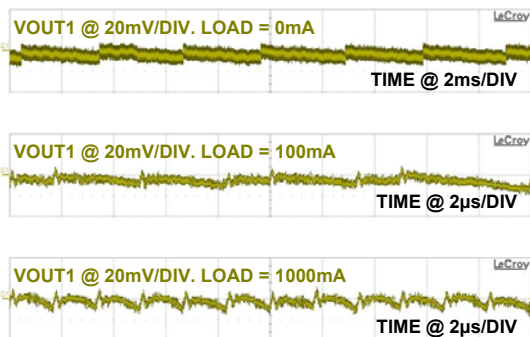
FIGURE 21. PWM3 START-UP. MODE = DEM, LOAD = 0A

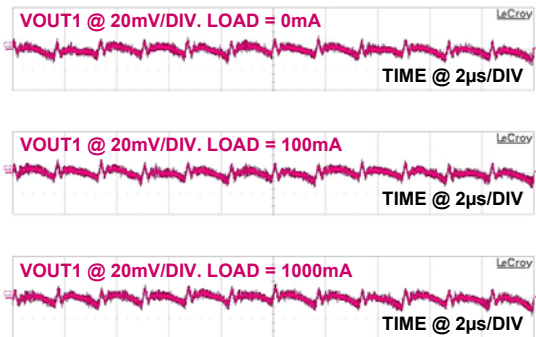FIGURE 22. PWM1 OUTPUT RIPPLE, MODE = 0V (DEM)
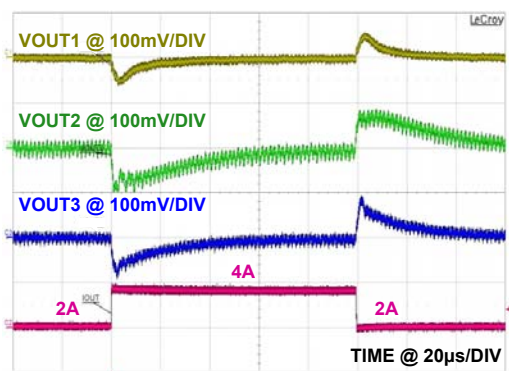
FIGURE 23. PWM1 OUTPUT RIPPLE, MODE = 5V (CCM)

FIGURE 24. PWM LOAD TRANSIENT RESPONSE

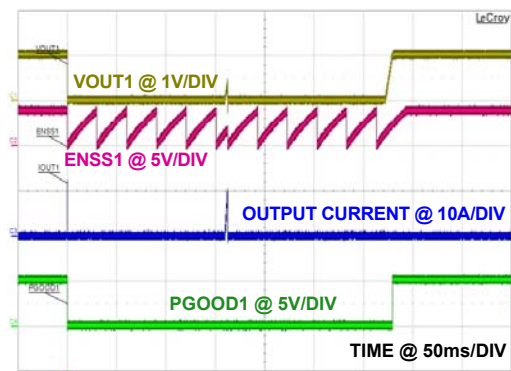FIGURE 25. PWM1 OCP RESPONSE. OUTPUT SHORT-CIRCUITED TO GROUND AND RELEASED.

intersil

Functional Description

General Description

The ISL9444 integrates control circuits for three synchronous buck converters. The three synchronous bucks operate out-of-phase to substantially reduce the input ripple and thus reduce the input filter requirements.

Each part has 3 independent enable/disable control lines (EN/SS1, EN2 and EN3), which provide flexible power-up sequencing. The soft-start time is programmable individually by adjusting the soft-start capacitors connected from EN/SS1, TK/SS2 and TK/SS3, respectively.

The valley current mode control scheme with input voltage feed-forward ramp simplifies loop compensation and provides excellent rejection to input voltage variation.

Input Voltage Range

The ISL9444 is designed to operate from input supplies ranging from 4.5V to 28V.

The input voltage range can be effectively limited by the available minimum PWM off time.

$$V_{IN(min)} = \left(\frac{V_{OUT} + V_{d1}}{1 - t_{OFF(min)} \times Frequency} \right) + V_{d2} - V_{d1} \qquad \text{(EQ. 2)}$$

where,
V_{d1} = sum of the parasitic voltage drops in the inductor discharge path, including the lower FET, inductor and PC board.
V_{d2} = sum of the voltage drops in the charging path, including the upper FET, inductor and PC board resistances.

The maximum input voltage and minimum output voltage is limited by the minimum on-time ($t_{ON(min)}$).

$$V_{IN(max)} \leq V_{OUT} \times \left(\frac{V_{OUT}}{t_{ON(min)} \times Frequency} \right) \qquad \text{(EQ. 3)}$$

Where $t_{ON(min)}$ = 100ns.

Internal 5V Linear Regulator (VCC_5V) and External VCC Bias Supply (EXTBIAS)

All ISL9444 functions can be internally powered from an on-chip, low dropout 5V regulator or an external 5V bias voltage via the EXTBIAS pin. Bypass the linear regulator's output (VCC_5V) with a 4.7µF capacitor to the power ground. The ISL9444 also employs an undervoltage lockout circuit which disables all regulators when VCC_5V falls below 3.6V.

The internal LDO can source over 75mA to supply the IC, power the low side gate drivers and charge the boot capacitors. When driving large FETs at high switching frequency, little or no regulator current may be available for external loads.

For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA). Also, at higher input voltages with larger FETs, the power dissipation across the internal 5V will increase. Excessive dissipation across this regulator must be avoided to prevent junction temperature rise. Thermal protection may be triggered if die temperature increases above +150°C due to excessive power dissipation.

When large MOSFETs are used, an external 5V bias voltage can be applied to EXTBIAS pin to alleviate excessive power dissipation. Voltage at the EXTBIAS pin must always be lower than the voltage at the VIN pin to prevent biasing of the power stage through EXTBIAS and VCC_5V. An external UVLO circuit might be necessary to guarantee smooth soft-starting.

The internal LDO has an overcurrent limit of typically 150mA. For better efficiency, connect VCC_5V to VIN for 5V ±10% input applications.

Enable Signals and Soft-Start Operation

Typical applications for the ISL9444 use programmable analog soft-start or the TK/SSx pins for tracking. The soft-start time can be set by the value of the soft-start capacitors connected from the EN/SS1 for PWM1 to ground and from TK/SSx pins to ground for PWM2 and PWM3. Inrush current during start-up can be alleviated by adjusting the soft-starting time.

After the VCC_5V pin reaches the UVLO threshold, the ISL9444 PWM1 soft-start circuitry becomes active. The internal 1.55µA charge current begins charging up the soft-start capacitor connected from the EN/SS1 pin to GND. The PWM1 output remains inactive until voltage on the EN/SS1 pin reaches 1.3V. As the voltage on the EN/SS1 pin rises from 1.3V to 2V, the PWM1 reference voltage is clamped to the voltage on the EN/SS1 pin minus 1.3V. PWM1 output voltage thus rises from 0V to regulation as EN/SS1 rises from 1.3V to 2V. Charging of the soft-start capacitor continues until the voltage on the EN/SS1 pin reaches 3.5V.

Power sequencing can be achieved by using the PGOODx and ENx pins. When the ENx pin is pulled high, the internal 1.55µA charge current begins charging up the soft-start capacitor connected from the TK/SSx pin to GND. The respective reference voltage is clamped to the voltage on the TK/SSx pin. Thus, PWM2 and PWM3 output voltages ramp from 0V to regulation as voltage on TK/SS2 and TK/SS3 goes up from 0V to 0.7V. Charging of the soft-start capacitors continues until the voltage on the TK/SSx reaches 3.5V.

The typical soft-start time is set according to Equation 4:

$$t_{SSx} = 0.7V \left(\frac{C_{SSx}}{1.55\mu A} \right) \qquad \text{(EQ. 4)}$$

For PWM2 and PWM3, when the soft-starting time set by external C_{SS} or tracking is less than 2ms, an internal soft-start circuit of 2ms takes over the soft-start. There is no internal soft-start for PWM1.

PGOODx will toggle to high when the corresponding output is up and in regulation.

Pulling the ENx low disables the corresponding PWM channel. The TK/SSx pin will also be discharged to GND by internal MOSFETs.

Output Voltage Programming

The ISL9444 provides a precision internal reference voltage to set the output voltage. Based on this internal reference, the output voltage can thus be set from 0.7V up to a level determined by the input voltage, the maximum duty cycle, and the conversion efficiency of the circuit.

A resistive divider from the output to ground sets the output voltage of any PWM channel. The center point of the divider shall be connected to the FBx pin. The output voltage value is determined by Equation 5.

$$V_{OUTx} = 0.7V \left(\frac{R1 + R2}{R2} \right)$$ (EQ. 5)

Where R1 is the top resistor of the feedback divider network and R2 is the bottom resistor connected from FBx to ground.

Tracking Operation

The PWM2 and PWM3 of the ISL9444 can be independently set up to track the output of another PWM or an external supply. In the following discussion, we refer to the voltage rail to be tracked as the master rail while we refer to the voltage rail that follows the master as the slave rail. To implement tracking, an additional resistive divider is connected between the master rail and ground. The center point of the divider shall be connected to the TK/SSx pin of the slave PWM. The resistive divider ratio sets the ramping ratio between the two voltage rails. To implement coincident tracking, set the tracking resistive divider ratio exactly the same as the slave rail output resistive divider given by Equation 5. Make sure that the voltage at TK/SSx is greater than 0.7V when the master rail reaches regulation.

To minimize the impact of the 1.55μA soft-start current on the tracking function, it is recommended to use resistors of less than 10kΩ for the tracking resistive dividers.

When overcurrent protection (OCP) is triggered for the slave PWM channel, the internal minimum soft-start circuit determines the OCP soft-start hiccup.

Light Load Efficiency Enhancement

When MODE/SYNC is tied to GND, the ISL9444 operates in high efficiency diode emulation mode and pulse skipping mode in light load condition. The inductor current is not allowed to reverse (discontinuous operation). At very light loads, the converter goes into diode emulation and triggers the pulse skipping function. Here, the upper MOSFET remains off until the output voltage drops to the point the error amplifier output goes above the pulse skipping mode threshold.

The minimum t_{ON} in the pulse skipping mode is 80ns; please select frequency so that the PWM t_{ON} is greater than 80ns at maximum VIN at no load.

Pre-biased Power-up

The ISL9444 has the ability to soft-start with a pre-biased output. The output voltage would not be yanked down during pre-biased start-up. The PWM is not active until the soft-start ramp reaches the output voltage times the resistive divider ratio.

Overvoltage protection is alive during soft-starting.

Frequency Selection

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing MOSFET switching loss. To meet output ripple and load transient requirements, operation at a low switching frequency would require larger inductance and output

capacitance. The switching frequency of the ISL9444 is set by a resistor connected from the RT pin to GND according to Equation 1.

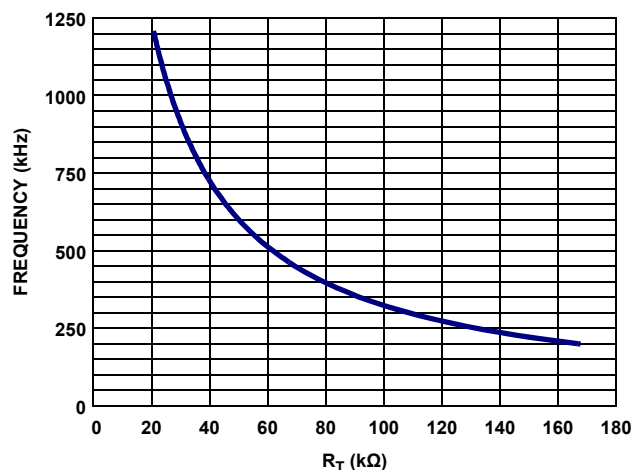Frequency setting curve shown in Figure 26 assists in selecting the correct value for R_T.

FIGURE 26. R_T vs SWITCHING FREQUENCY

Frequency Synchronization

The MODE/SYNC pin may be used to synchronize two or more ISL9444 or ISL9443 controllers. When the MODE/SYNC pin is connected to the CLKOUT pin of another ISL9444, the two controllers operate in synchronization.

When the MODE/SYNC pin is connected to an external clock, the ISL9444 will synchronize to this external clock at half of the clock frequency. For proper operation, frequency setting resistor, R_T, should be set according to Equation 1.

When frequency synchronization is in action, the controllers will enter forced continuous current mode at light load.

Out-of-Phase Operation

To reduce input ripple current, the three PWM channels operate 180° out-of-phase. This reduces the input capacitor ripple current requirements, reduces power supply-induced noise, and improves EMI. This effectively helps to lower component cost, save board space and reduce EMI.

Triple PWMs traditionally operate in-phase and turn on all three upper FETs at the same time. The input capacitor must then support the instantaneous current requirements of the three switching regulators simultaneously, resulting in increased ripple voltage and current. The higher RMS ripple current lowers the efficiency due to the power loss associated with the ESR of the input capacitor. This typically requires more low-ESR capacitors in parallel to minimize the input voltage ripple and ESR-related losses, or to meet the required ripple current specification.

With synchronized out-of-phase operation, the high-side MOSFETs turn off 180° out-of-phase. The instantaneous input current peaks of both regulators no longer overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating,

allowing fewer or less expensive capacitors, and reducing the shielding requirements for EMI. The typical operating curves show the synchronized 180° out-of-phase operation.

Power Failure Monitor

The ISL9444 has a Power-Failure Monitor that helps to monitor an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, detect a low-battery condition, or simply monitor a power supply. An external resistor divider network is needed to provide monitoring of voltages greater than 1.22V. The threshold voltage is set according to Equation 6 (see Typical Application on page 7).

$$VPFITH = 1.22V \times \frac{R14 + R15}{R15} \qquad \text{(EQ. 6)}$$

$\overline{PFO}$ goes low whenever the PFI pin voltage is less than the 1.22V threshold voltage.

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals providing amplification, level shifting and shoot-through protection. The gate drivers have circuitry that helps optimize the IC performance over a wide range of operational conditions. As MOSFET switching times can vary dramatically from type to type and with input voltage, the gate control logic provides adaptive dead time by monitoring real gate waveforms of both the upper and the lower MOSFETs. Shoot-through control logic provides a 16ns dead-time to ensure that both the upper and lower MOSFETs will not turn on simultaneously causing a shoot-through condition.

Gate Drivers

The low-side gate drivers are supplied from VCC_5V and provide a peak sink current of 2A and source current of 800mA for each PWM channel. The high-side gate drivers are also capable of delivering the same currents as the low-side gate drivers. Gate-drive voltage for the upper N-Channel MOSFETs are generated by flying capacitor boot circuits. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side MOSFET driver. To limit the peak current in the IC, an external resistor may be placed between the BOOT pin and the boot capacitor. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

At start-up, the low-side MOSFET turns on first and forces PHASE to ground in order to charge the BOOT capacitor to 5V. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. This provides the necessary gate-to-source voltage to turn on the upper MOSFET, an action that boosts the 5V gate drive signal above VIN. The current required to drive the upper MOSFET is drawn from the internal 5V regulator.

For optimal EMI performance or reducing phase node ringing, a small resistor might be placed between these pins to the positive terminal of the bootstrap capacitors.
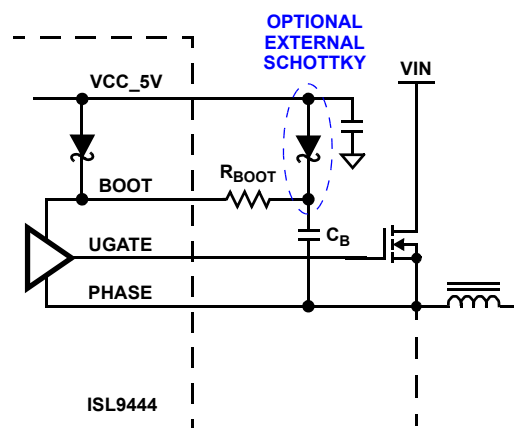

FIGURE 27. UPPER GATE DRIVER CIRCUIT

Adaptive Dead Time

The ISL9444 incorporates an adaptive dead time algorithm on the synchronous buck PWM controllers that optimizes operation with varying MOSFET conditions. This algorithm provides approximately 16ns of dead time between switching the upper and lower MOSFET's. This dead time is adaptive and allows operation with different MOSFET's without having to externally adjust the dead time using a resistor or capacitor. During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a threshold of 1V, at which time the UGATE is released to rise. Adaptive dead time circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise. It is recommended to not use a resistor between UGATE and LGATE and the respective MOSFET gates as it may interfere with the dead time circuitry.

Internal Bootstrap Diode

The ISL9444 has integrated bootstrap diodes to help reduce total cost and reduce layout complexity. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap capacitor must have a maximum voltage rating above the maximum input voltage plus 5V. The bootstrap capacitor can be chosen from Equation 7.

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \qquad \text{(EQ. 7)}$$

Where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge (QGATE) of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance of 0.22µF should be used. A good quality ceramic capacitor is recommended.

The internal bootstrap Schottky diodes have a resistance of 1.5Ω (typ) at 800mA. Combined with the resistance RBOOT, this could lead to the boot capacitor charging insufficiently in cases where the bottom MOSFET is turned on for a very short time. If such

circumstances are expected, an additional external Schottky diode may be added from VCC_5V to the positive of the boot capacitor. RBOOT may still be necessary to lower EMI due to fast turn-on of the upper MOSFET.

Power-Good Indicators

The three independent Power-good pins can be used to monitor the status of the output voltages. PGOODx will be true (open drain) when the corresponding FBx pin is within ±11% of the reference voltage.

Additionally, a capacitor from the PG3_DLY pin to the ground sets a delay time for the PGOOD3 signal. After FB3 pin enters ±11% of the reference range, a 1.9µA current begins charging the CDLY capacitor. When the PG3_DLY voltage reaches 1.2V PGOOD3 goes HIGH.

The typical delay time is set according to Equation 8:

$$t_{DLY} = 1.2V\left(\frac{C_{DLY}}{1.9\mu A}\right) \tag{EQ. 8}$$

There is no extra delay when the PGOOD3 pin is pulled LOW.

Protection Circuits

The converter outputs are monitored and protected against overload, short circuit and undervoltage conditions.

Undervoltage Lockout

The ISL9444 includes UVLO protection which keeps the device in a reset condition until a proper operating voltage is applied. It also shuts down the ISL9444 if the operating voltage drops below a pre-defined value. All controllers are disabled when UVLO is asserted. When UVLO is asserted, PGOOD1, PGOOD2 and PGOOD3 are valid and will be de-asserted.

Overcurrent Protection

All the PWM controllers use the lower MOSFET's on-resistance, $r_{DS(ON)}$, to monitor the current in the converter. The sensed voltage drop is compared with a threshold set by a resistor connected from the OCSETx pin to ground.

$$R_{OCSET} = \frac{(7)(R_{CS})}{(I_{OC})(r_{DS(ON)})} \tag{EQ. 9}$$

Where I_{OC} is the desired overcurrent protection threshold, and R_{CS} is a value of the current sense resistor connected to the ISENx pin.

If an overcurrent is detected, the upper MOSFET remains off and the lower MOSFET remains on until the next cycle. As a result, the converter will skip a pulse. When the overload condition is removed, the converter will resume normal operation.

If an overcurrent is detected for 2 consecutive clock cycles, the IC enters a hiccup mode by turning off the gate drivers and entering soft-start. The IC will cycle 5 times through soft-start before trying to restart. The IC will continue to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start so care must be taken to ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

Because of the nature of this current sensing technique, and to accommodate a wide range of $r_{DS(ON)}$ variations, the value of the overcurrent threshold should represent an overload current about 150% to 180% of the maximum operating current. If more accurate current protection is desired, place a current sense resistor in series with the lower MOSFET source.

When OCP is triggered, the EN/SS1 or TK/SSx pins are pulled to ground by an internal MOSFET. For PWM rails configured to track another voltage rail, the TK/SSx pin rises up much faster than the internal minimum soft-start ramp. The voltage reference will then be clamped to the internal minimum soft-start ramp. Thus smooth soft-start hiccup is achieved even with tracking function.

Overvoltage Protection

All switching controllers within the ISL9444 have fixed overvoltage set points. The overvoltage set point is set at 118% of the nominal output voltage, the output voltage set by the feedback resistors. In the case of an overvoltage event, the IC will attempt to bring the output voltage back into regulation by keeping the upper MOSFET turned off and modulating the lower MOSFET for 2 consecutive PWM cycles. If the overvoltage condition has not been corrected in 2 cycles and the output voltage is above 118% of the nominal output voltage, the ISL9444 will turn off both the upper MOSFET and the lower MOSFET. The ISL9444 will enter hiccup mode until the output voltage returns to 110% of the nominal output voltage.

Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +150°C is reached. Normal operation resumes when the die temperatures drops below +130°C through the initiation of a full soft-start cycle. When all three channels are disabled, thermal protection is inactive. This helps achieve a very low shutdown current of 33µA.

Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, all PWM controllers have internally compensated error amplifiers. To make internal compensation possible, several design measures were taken.

Firstly, the ramp signal applied to the PWM comparator is proportional to the input voltage provided at the VIN pin. This keeps the modulator gain constant with varying input voltages. Secondly, the load current proportional signal is derived from the voltage drop across the lower MOSFET during the $\overline{PWM}$ time interval and is subtracted from the amplified error signal on the comparator input. This creates an internal current control loop. The resistor connected to the ISEN pin sets the gain in the current feedback loop. The following expression estimates the required value of the current sense resistor depending on the maximum operating load current and the value of the MOSFET's $r_{DS(ON)}$.

$$R_{CS} \geq \frac{(I_{MAX})(r_{DS(ON)})}{30\mu A} \tag{EQ. 10}$$

Choosing R_{CS} to provide 30µA of current to the current sample and hold circuitry is recommended but values down to 2µA and

up to 100µA can be used. A higher sampling current will help to stabilize the loop.

Due to the current loop feedback, the modulator has a single pole response with -20dB slope at a frequency determined by the load.

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} \tag{EQ. 11}$$

Where R_O is load resistance and C_O is load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 28 shows a Type 2 amplifier and its response, along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 10\,kHz \tag{EQ. 12}$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 600\,kHz \tag{EQ. 13}$$

Zero frequency, amplifier high-frequency gain and modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation, plenty of phase margin is easily achieved due to zero-pole pair phase 'boost'.
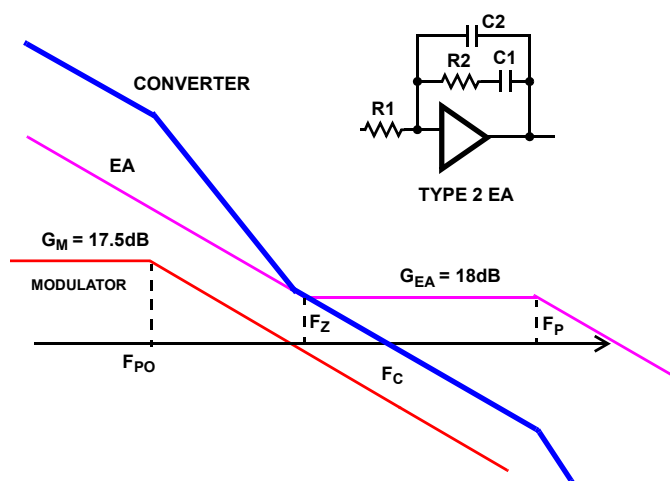

FIGURE 28. FEEDBACK LOOP COMPENSATION

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase 'boost'. Some phase boost can also be achieved by connecting capacitor C_Z in parallel with the upper resistor R_1 of the divider that sets the output voltage value. Please refer to "Input Capacitor Selection" on page 22.

Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL9444 based DC/DC converter. The ISL9444 switches at a very high frequency and therefore the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

There are three sets of critical components in a DC/DC converter using the ISL9444: The controller, the switching power components and the small signal components. The switching power components are the most critical from a layout point of view because they switch a large amount of energy so they tend to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multi-layer printed circuit board is recommended.

Layout Considerations

1. The input capacitors, upper FET, lower FET, inductor and output capacitor should be placed first. Isolate these power components on the topside of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitors very close to the MOSFETs.

2. Use separate ground planes for power ground and small signal ground. Connect the SGND and PGND together close to the IC. Do not connect them together anywhere else.

3. The loop formed by the input capacitor, the top FET and the bottom FET must be kept as small as possible.

4. Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and output capacitor are as short as possible with maximum allowable trace widths.

5. Place the PWM controller IC close to the lower FET. The LGATE connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop currents in this area.

6. Place VCC_5V bypass capacitor very close to VCC_5V pin of the IC and connect its ground to the PGND plane.

7. Place the gate drive components - optional BOOT diode and BOOT capacitors - together near controller IC.

8. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances.

9. Use copper filled polygons or wide but short trace to connect the junction of upper FET, lower FET and output inductor. Also keep the PHASE node connection to the IC short. Do not unnecessarily oversize the copper islands for PHASE node. Since the phase nodes are subjected to very high dv/dt

ISL9444

voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise.

10. Route all high speed switching nodes away from the control circuitry.

11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths including feedback resistors, current limit setting resistors, soft-starting capacitors and ENx pull-down resistors should be connected to this SGND plane.

12. Separate current sensing traces from PHASE node connections.

13. Ensure the feedback connection to the output capacitor is short and direct.

General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.
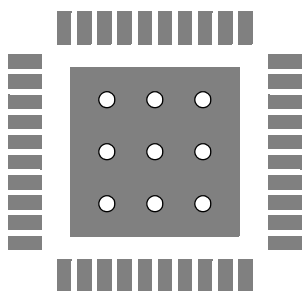

FIGURE 29. PCB VIA PATTERN

It is recommended to fill the thermal pad area with vias. A typical via array fills the thermal pad footprint such that their centers are 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated-through hole to each plane.

Component Selection Guideline

MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements. Two N-Channel MOSFETs are used in each of the synchronous-rectified buck converters for the 3 PWM outputs. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

Power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see Equations 14 and 15). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower

device turns on and off into near zero voltage. The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode.

$$P_{UPPER} = \frac{(I_O{}^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_O)(V_{IN})(t_{SW})(F_{SW})}{2} \quad \text{(EQ. 14)}$$

$$P_{LOWER} = \frac{(I_O{}^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 15)}$$

A large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFETs' switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

Output Inductor Selection

The PWM converters require output inductors. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and the output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by Equation 16:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_S)(L)(V_{IN})} \quad \text{(EQ. 16)}$$

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The ISL9444 will provide either 0% or maximum duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ. 17)}$$

Where C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input

voltage, V_O is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Equivalent Series Resistance) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by:

$$V_{RIPPLE} = \Delta I_L (ESR) \qquad \text{(EQ. 18)}$$

Where I_L is calculated in the "Input Capacitor Selection" on page 22.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. In most cases, multiple small-case electrolytic capacitors perform better than a single large-case capacitor.

The stability requirement on the selection of the output capacitor is that the 'ESR zero' (f_Z) be between 2kHz and 60kHz. This range is set by an internal, single compensation zero at 8.8kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop.

Therefore:

$$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)} \qquad \text{(EQ. 19)}$$

In conclusion, the output capacitors must meet three criteria:

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.

2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.

3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

The recommended output capacitor value for the ISL9444 is between 100µF to 680µF, to meet stability criteria with external compensation. Use of aluminum electrolytic (POSCAP) or tantalum type capacitors is recommended. Use of low ESR ceramic capacitors is possible with loop analysis to ensure stability.

Input Capacitor Selection

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load. The total RMS current supplied by the input capacitance is:

$$I_{RMS} = \sqrt{I_{RMS1}^2 + I_{RMS2}^2} \qquad \text{(EQ. 20)}$$

Where DC is duty cycle of the respective PWM.

$$I_{RMSx} = \sqrt{DC - DC^2} \cdot I_O \qquad \text{(EQ. 21)}$$

Depending on the specifics of the input power and its impedance, most (or all) of this current is supplied by the input capacitor(s). Figure 30 shows the advantage of having the PWM converters operating out-of-phase. If the converters were operating in phase, the combined RMS current would be the algebraic sum, which is a much larger value as shown. The combined out-of-phase current is the square root of the sum of the square of the individual reflected currents and is significantly less than the combined in-phase current.
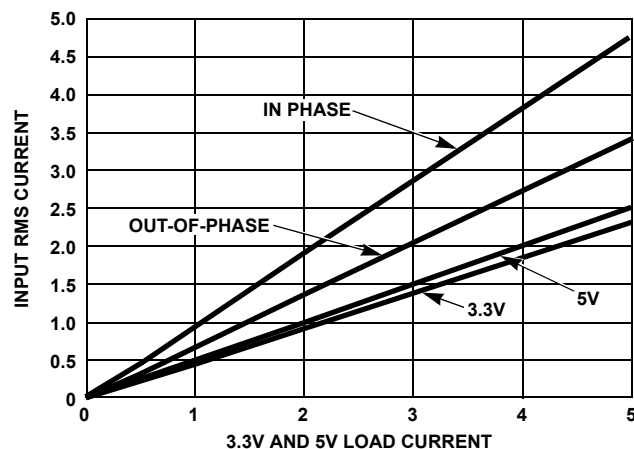

FIGURE 30. INPUT RMS CURRENT vs LOAD

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For board designs that allow through-hole components, the Sanyo OS-CON™ series offer low ESR and good temperature performance. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX is surge current tested.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 23, 2011	FN7665.0	Initial Release

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL9444

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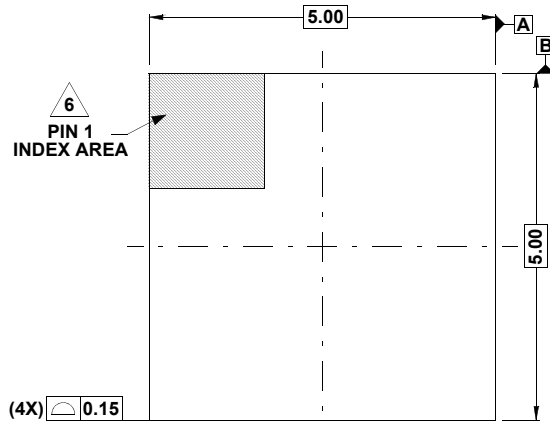
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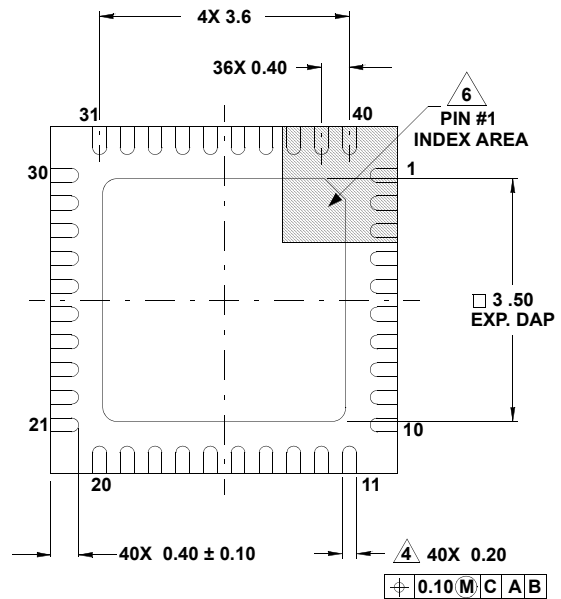May 23, 2011

Package Outline Drawing

L40.5x5B
40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
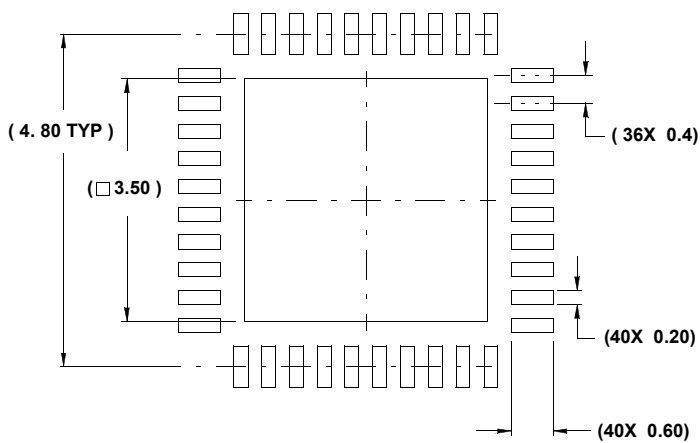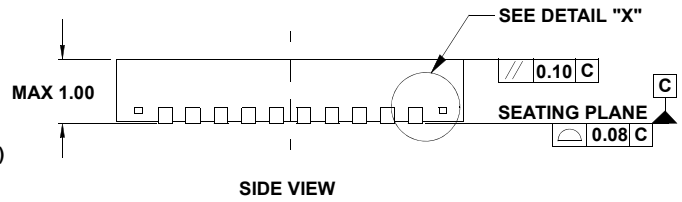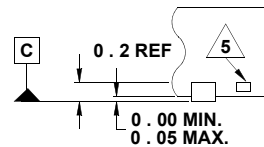**Rev 0, 5/10**

TOP VIEW

BOTTOM VIEW

TYPICAL RECOMMENDED LAND PATTERN

SIDE VIEW

DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.10

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. JEDEC reference drawing: MO220VHHE-1