Data Sheet | September 18, 2007 | FN6495.4

DC/DC Power Switching Regulator

The ISL8540 is a step down DC/DC power switching regulator which accepts 9.0V to 40V input and provides a 2A output current. The output voltage can be set in the range between 1.21V and 35V by means of an external divider. The device uses an internal power DMOS transistor with a typical $r_{DS(ON)}$ of 0.19Ω to obtain very high efficiency and high switching speed. A switching frequency in the range of 100kHz to 600kHz can be realized (the maximum power dissipation of the various packages must be observed). Notable features of this next generation of DC/DC converter include pulse-by-pulse current limit for FET protection, hiccup mode for short circuit protection, voltage feedforward regulation, Frequency SYNC, soft-start, low standby current of 60µA typical in the disabled state, and thermal shut-down. The device is available in a 20 Ld HTSSOP package.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8540IVEZ	ISL8540IVEZ	-40 to +85	20 Ld HTSSOP	MDP0048
ISL8540IVEZ-T*	ISL8540IVEZ	-40 to +85	20 Ld HTSSOP	MDP0048

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Voltage feedforward mode
- Step down DC/DC supporting up to 2A
- Input voltage range of 9.0V to 40V
- Internal reference of 1.21V ±1%
- Adjustable output voltage range of 1.21V to 35V
- Adjustable switching frequency 100kHz to 600kHz
- Frequency SYNC pin
- Zero load current operation
- Pulse by pulse mode current limit and Hiccup mode
- Low standby current of 60µA typical
- Thermal shut-down
- Load dump to 100V for 400ms
- Pb-free (RoHS compliant)

Applications

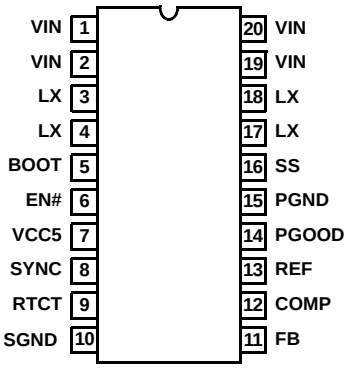
- Non-isolated telecom power supply
- Industrial and automotive power supplies
- Portable computers
- Battery chargers
- Distributed power systems

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

ISL8540
(20 LD HTSSOP)
TOP VIEW



Absolute Maximum Ratings

Input Voltage VIN . . . . . GND -0.3V to 42V
Voltage at BOOT pin . . . . . GND -0.3V to 49V
LX, RTCT . . . . . GND -0.3V to 42V
REF, FB, SS, EN#, SYNC, PGOOD pins 8V
VCC5 . . . . . GND -0.3V to 5.5V

Recommended Operating Conditions

Junction Temperature Range . . . . . -40°C to +125°C
Supply Voltage Range (Typical) . . . . . 9.0V to 40V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
HTSSOP Package	40	2.5

Maximum Power Dissipation 3W
Maximum Junction Temperature (Hermetic Package or Die) . . +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**An accidental short between VCC5 and GND may cause excessive heating and permanent damage to the device.*

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Additional heatsinking may be required to insure that junction temperature do not exceed above +125°C.

Electrical Specifications

Unless otherwise specified the specifications listed in the table are tested at T_A = +25°C and guard band for the full Temperature Range, V_{IN} = 24V, V_{OUT} = 5.0V, I_{OUT} = 0A. Typical values are at T_A = +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN SUPPLY						
Input Voltage Range			9.0	24	40	V
VIN SUPPLY CURRENT						
Shut-down Current	IDD	V_{IN} = 9V, EN = HIGH		35	60	µA
		V_{IN} = 40V, EN = HIGH		60	110	µA
Operating Current	IDD	V_{IN} = 9V, V_{FB} = 1.5V		3.6	4	mA
		V_{IN} = 40V, V_{FB} = 1.5V		6.0	8.0	mA
VCC5 SUPPLY (A 1µF cap is needed from VCC5 to GND)						
VCC5 Output Voltage		V_{IN} = 9.0V to 40V, I_L = 0mA to 5mA	4.9	5.0	5.1	V
Maximum Output Current		V_{IN} = 24V			5	mA
INPUT UV						
Rising UV Threshold			7.8		8.9	V
UV Threshold Hysteresis			0.18	0.3	0.55	V
BUCK CONVERTER						
Output Voltage (Note 3)		I_{OUT} = 2A	1.2		V_{IN} - 5	V
Maximum Duty Cycle		F = 300kHz	90	96		%
Minimum Controllable ON Time		F = 300kHz		150		ns
OSCILLATOR						
Total Variation on Set Frequency		Over the V_{IN} range with frequency set by external resistor and capacitor at RTCT		±10		%
Frequency Range (Set by RTCT)	f_{OSC}		100		600	kHz
SYNC Range	f_{OSC}		100		600	kHz
Oscillation Frequency	f_{OSC}	V_{IN} = 9V to 40V, R_T = 100kΩ, C_T = 1200pF		60		kHz
		V_{IN} = 9V to 40V, R_T = 27.4kΩ, C_T = 220pF		725		kHz

Electrical Specifications Unless otherwise specified the specifications listed in the table are tested at T_A = +25°C and guard band for the full Temperature Range, V_{IN} = 24V, V_{OUT} = 5.0V, I_{OUT} = 0A. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Max Ramp Amplitude	ΔV_{OSC}	V_{IN} = 9V		1		V_P
Modulator Gain	$V_{VIN}/\Delta V_{OSC}$			9		-
Min OFF Time				150	300	ns
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}			1.21		V
Soft-Start Current	I_{SS}		8	10	12	µA
Soft-Start Threshold	V_{SOFT}		1.0			V
ERROR AMPLIFIER						
Transconductance	g_m		3.9	5.7	7.2	mS
Gain-Bandwidth Product	GBW			15		MHz
Slew Rate	SR			6		V/µs
COMP Pin Drive	I_{COMP}			±200		µA
Internal Feedback Voltage	V_{FB}	T_A = -40°C to +85°C, V_{IN} = 9.0V to 40V	1.194	1.210	1.222	V
Internal Feedback Bias Current	I_{FB}	T_A = -40°C to +85°C, V_{FB} = 1.20V		±50	±100	nA
OVERCURRENT PROTECTION						
Dynamic Current Limit ON Time	t_{OCON}			16		Clock pulses
Dynamic Current Limit OFF Time	t_{OCOFF}			4		SS cycle
Switch Current Limit	I_{LIMIT}	T_A = +25°C	3.2	4.0	4.8	A
POWER GOOD (OPEN DRAIN)						
Power-Good Lower Threshold	V_{PG-}	Fraction of the V_{OUT} set point; ~3µs noise filter	85		89	%
	V_{PG+}	Fraction of the V_{OUT} set point; ~3µs noise filter	111		115	%
PGOOD Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V			1	µA
PGOOD Voltage Low		I_{PGOOD} = 4mA			0.5	V
MOSFET						
Switch ON Resistance	$r_{DS(ON)}$	I_{OUT} = 2A, V_{BOOT} = V_{IN} + 5.0V, Tested at wafer level		0.19	0.355	Ω
EN#						
Input HIGH Level (Asserted)	VINHIGH		2.6			V
Input LOW Level (Unasserted)	VINLOW				1.2	V
Input Current HIGH	I_{ENHIGH}	V_{IN} = 24V			25	µA
Input Current LOW	I_{ENLOW}	V_{IN} = 24V			25	µA
SYNC						
Input HIGH Level (Asserted)	VINHIGH		2.6			V
Input LOW Level (Unasserted)	VINLOW				1.2	V
Input Current HIGH	$I_{SYNCHIGH}$				0.2	µA
Input Current LOW	$I_{SYNCLOW}$				0.2	µA
THERMAL SHUT-DOWN						
Thermal Shut-down Temperature		Rising Threshold		150		°C
Thermal Shut-down Hysteresis				15		°C

Pin Descriptions

VIN (Pins 1, 2, 19, 20)

The input supply for the PWM regulator power stage. Connected to DRAIN of the high side MOSFET.

LX (Pins 3, 4, 17, 18)

There are four output pins that must be connected together externally in normal operation.

BOOT (Pin 5)

A capacitor is connected from this pin to the output pin. An internal 10V supply and an internal schottky diode provide the high side voltage to drive the gate of the internal DMOS device.

EN# (Pin 6)

The EN# input will disable the part and shut-down all function when it is held high or left OPEN. The EN# current will be 10µA typical. An internal pull-up resistor will hold the pin high. When EN# = Low, the part is enabled. Connect to GND for auto start-up.

VCC5 (Pin 7)

VCC5 is the +5.0V output pin which provides an output of an internal supply for supply filtering purposes. A 1µF capacitor should be connected from this pin to GND. Internal VDD supply is set at 5.0V (not planned that the user would use this supply).

SYNC (Pin 8)

This pin provides a digital input pin to synchronize the internal oscillator to an external signal. When the sync function is not used, this pin can be left open or tied to GND. If the sync function is used, the RTCT timing must be set to a frequency lower than the sync input frequency. The termination of the ramp is synchronized with the rising edge of the sync input signal. There are no duty cycle restrictions on the input sync signal. Input thresholds are TTL compatible.

RTCT (Pin 9)

A resistor to VIN and a capacitor to GND determine the frequency of the saw-tooth oscillator. Resistor range, R = 20k to 100k. Capacitor range, C = 470pF to 1.2nF. The oscillator amplitude will vary from approximately 0.9V to 10V as V_{IN} changes from 8.5V to 40V to maintain constant frequency and provide feed forward. The oscillator will have a fixed off time, which will establish the maximum on time for the regulator. This off time will be <200ns. The maximum duty cycle for a 500kHz system will therefore be approximately 90%, as the frequency of the maximum duty cycle will increase (95% for 250kHz system). The minimum duty cycle is zero.

SGND (Pin 10)

The SGND terminal of the ISL8560 provides the return path for the control and monitor portions of the IC.

FB (Pin 11)

This is the feedback pin. The feedback ratio is set by an external resistor divider connected to the load.

COMP (Pin 12)

This pin is connected to the output of the Error Amplifier and is used to compensate the loop. The Error Amplifier is a GM amplifier.

REF (Pin 13)

1.20V reference output. Bypass to GND with 1µF capacitor.

PGOOD (Pin 14)

This pin is an open drain output that is turned on when the feedback voltage is more than ±10% from the reference voltage, indicating that the output is not within 10% of set point.

PGND (Pin 15)

This pins are used as the ground connection of the power train.

SS (Pin 16)

A capacitor is connected from this pin to GND to determine the soft-start timing. The soft-start pin internal charging current is 10µA.

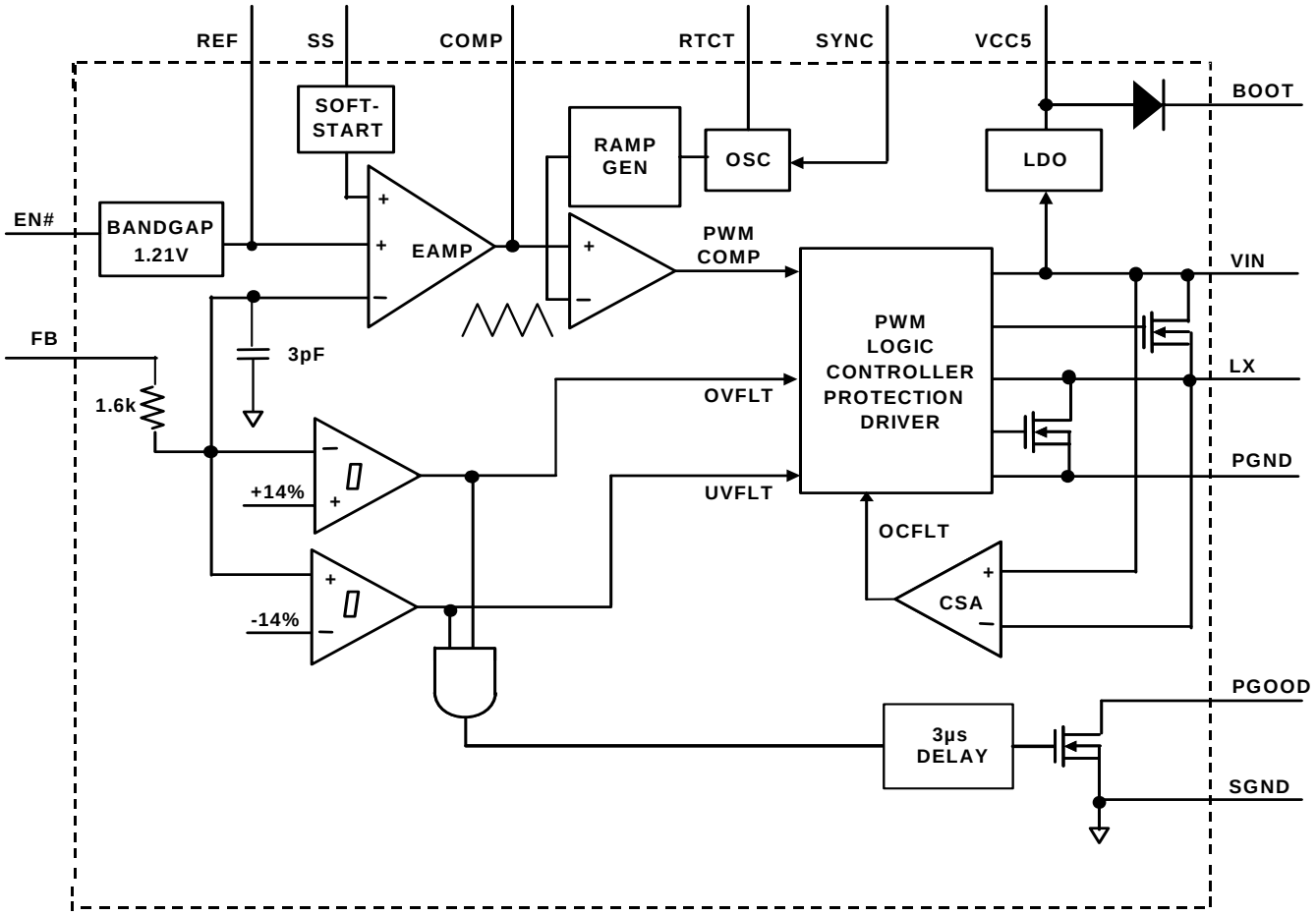


FIGURE 1. BLOCK DIAGRAM OF THE ISL8540

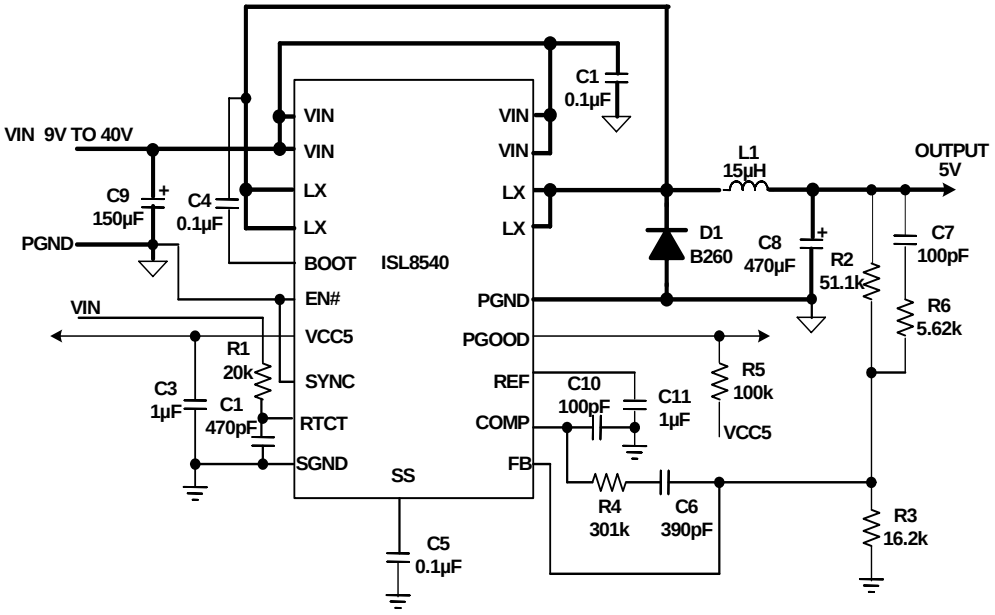


FIGURE 2. TYPICAL SCHEMATIC FOR ISL8540 (5V V_{OUT})

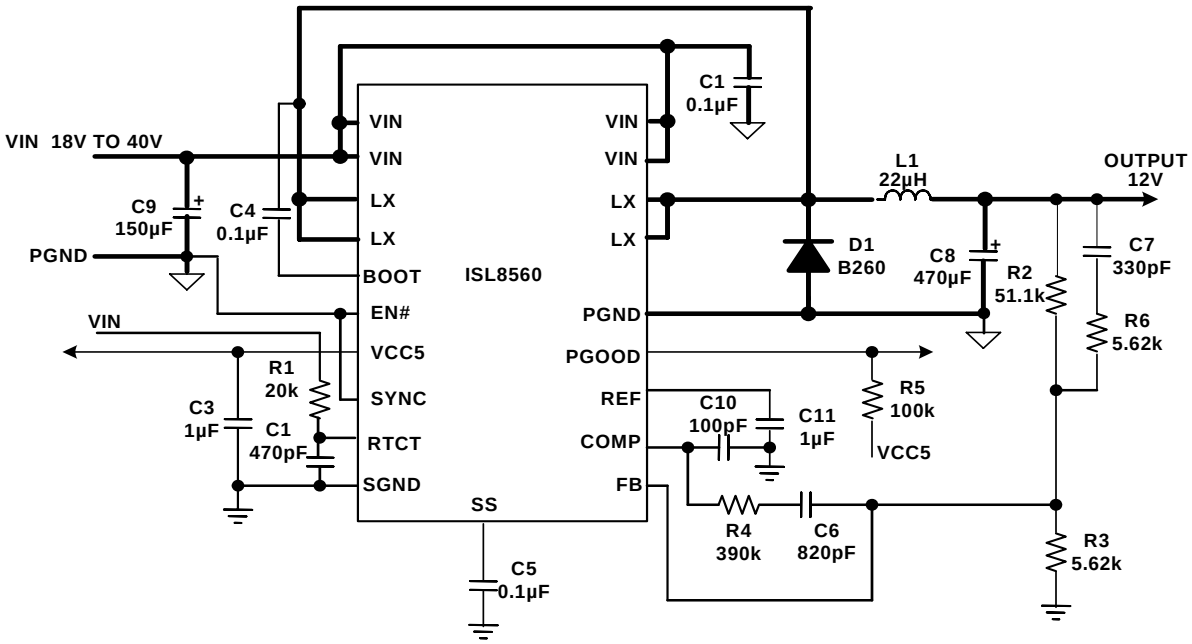


FIGURE 3. TYPICAL SCHEMATIC FOR ISL8540 (12V V_{OUT})

Typical Performance Curves

Circuit of Figure 2, V_{IN} = 24V, EN# = 0V, FS = 500KHz, V_{OUT} = 5V, unless otherwise noted. Typical values are at T_A = +25°C.

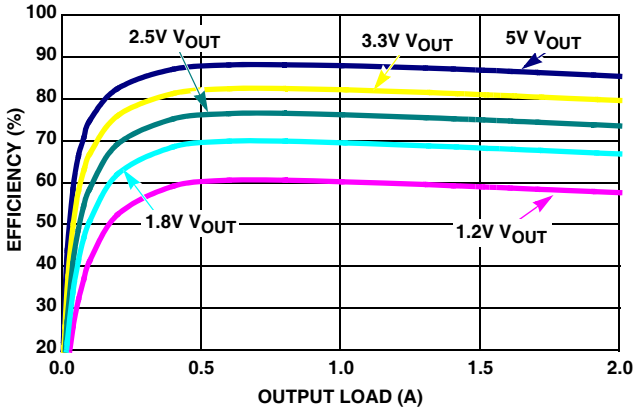


FIGURE 4. EFFICIENCY vs LOAD (12V INPUT - 500kHz)

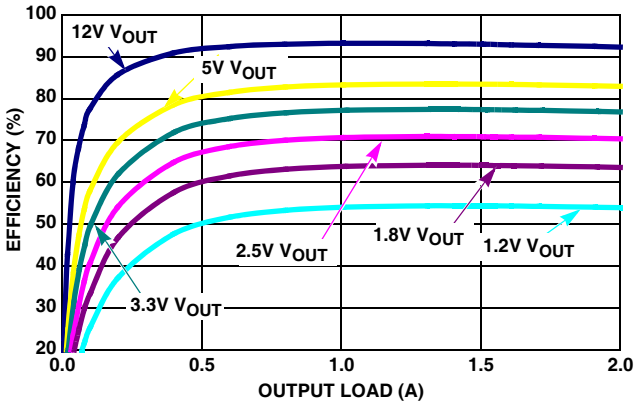


FIGURE 5. EFFICIENCY vs LOAD (24V INPUT - 500kHz)

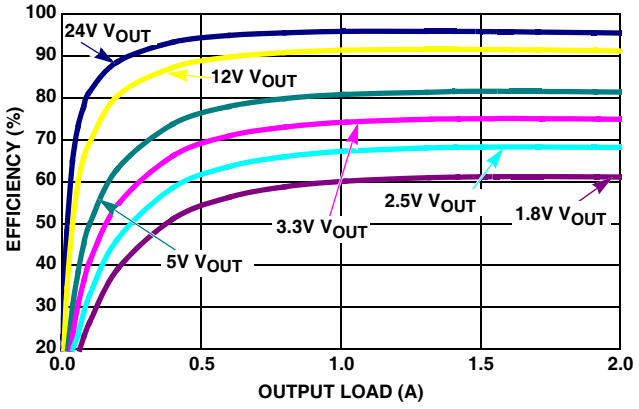


FIGURE 6. EFFICIENCY vs LOAD (36V INPUT - 500kHz)

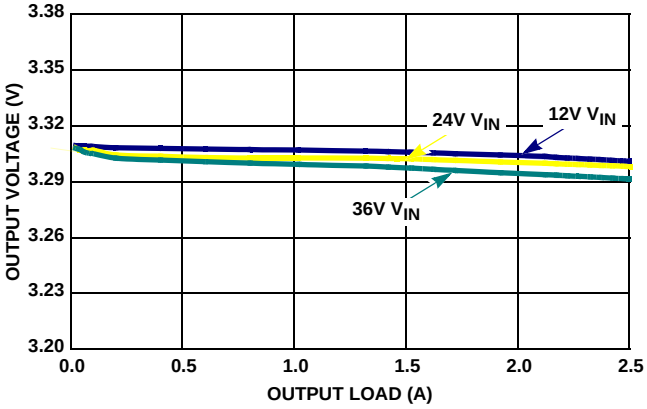


FIGURE 7. V_{OUT} REGULATION vs LOAD (V_{OUT} = 3.3V - 500kHz)

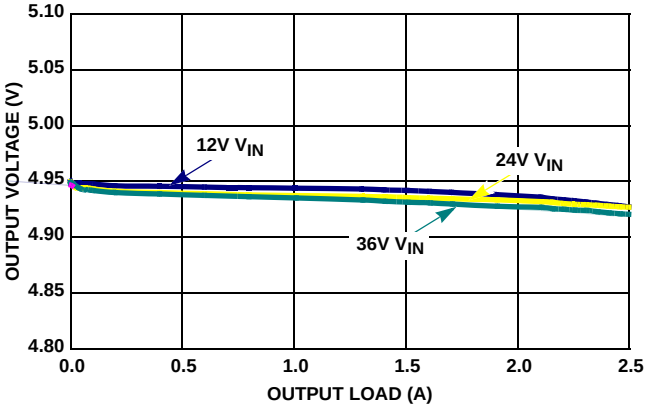


FIGURE 8. V_{OUT} REGULATION vs LOAD (V_{OUT} = 5V - 500kHz)

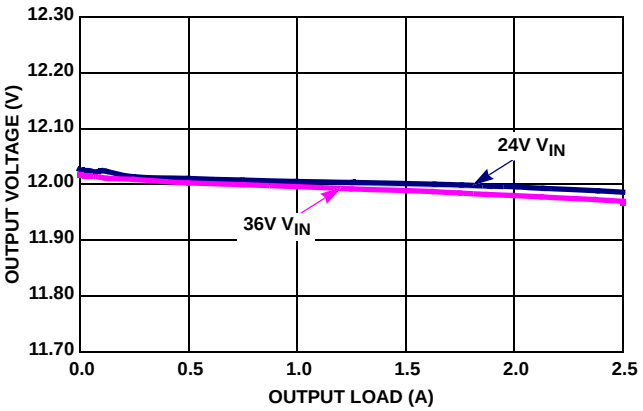


FIGURE 9. V_{OUT} REGULATION vs LOAD (V_{OUT} = 12V - 500kHz)

Typical Performance Curves

Circuit of Figure 2, V_{IN} = 24V, EN# = 0V, FS = 500KHz, V_{OUT} = 5V, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

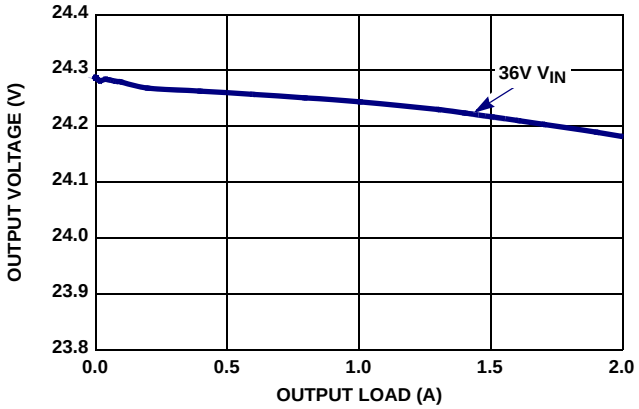


FIGURE 10. V_{OUT} REGULATION vs LOAD (V_{OUT} = 24V - 500kHz)

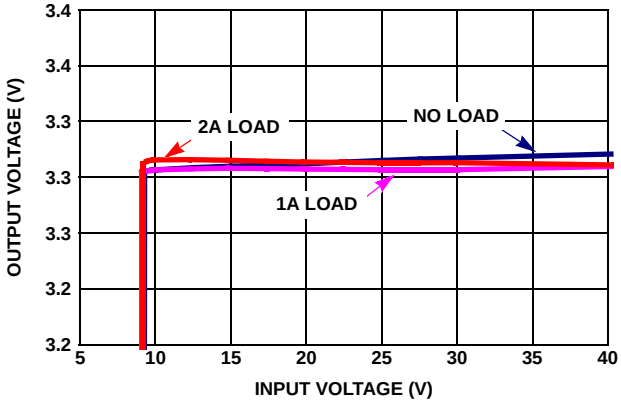


FIGURE 11. OUTPUT VOLTAGE REGULATION vs V_{IN} PWM MODE

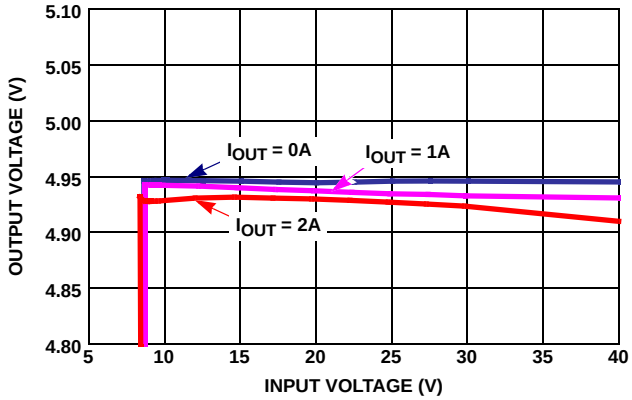


FIGURE 12. OUTPUT VOLTAGE REGULATION vs V_{IN} (V_{OUT} = 5V - 500kHz)

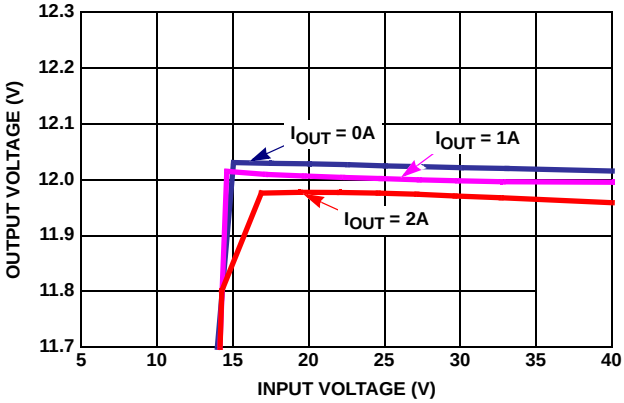


FIGURE 13. OUTPUT VOLTAGE REGULATION vs V_{IN} (V_{OUT} = 5V - 500kHz)

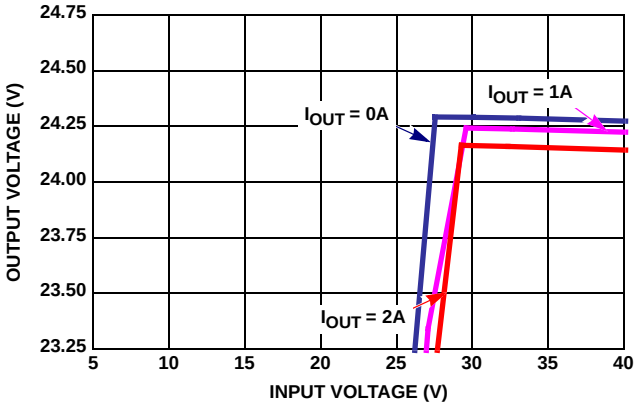


FIGURE 14. OUTPUT VOLTAGE REGULATION vs V_{IN} (V_{OUT} = 5V - 500kHz)

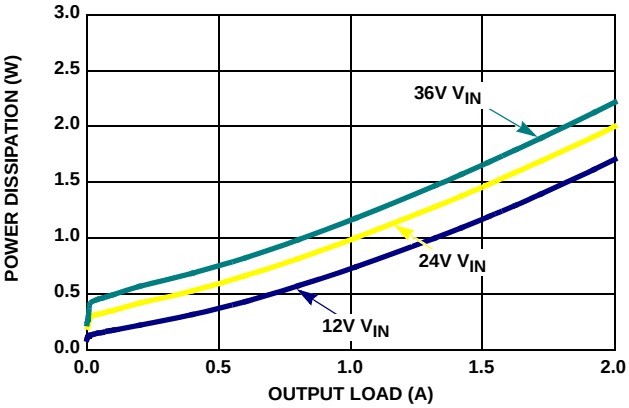


FIGURE 15. POWER DISSIPATION vs LOAD (V_{OUT} = 3.3V - 500kHz)

Typical Performance Curves

Circuit of Figure 2, V_{IN} = 24V, EN# = 0V, FS = 500KHz, V_{OUT} = 5V, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

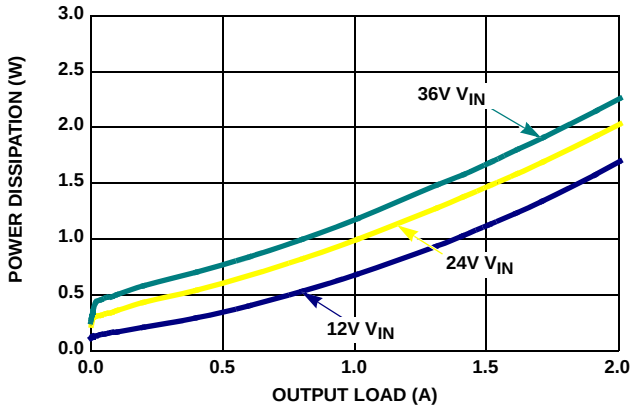


FIGURE 16. POWER DISSIPATION vs LOAD (V_{OUT} = 5V - 500kHz)

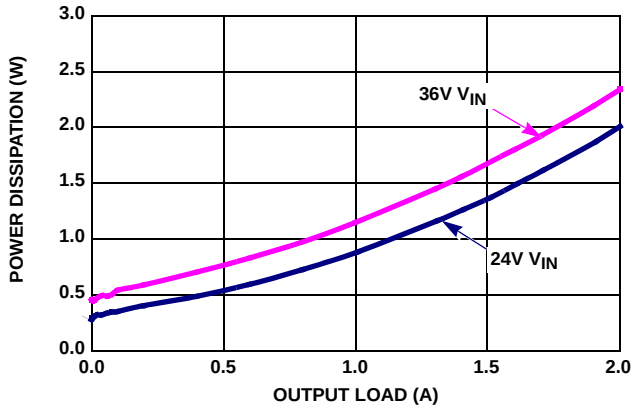


FIGURE 17. POWER DISSIPATION vs LOAD (V_{OUT} = 12V - 500kHz)

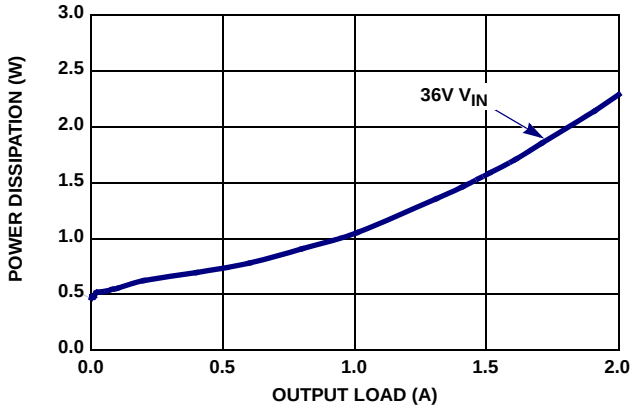


FIGURE 18. POWER DISSIPATION vs LOAD (V_{OUT} = 24V - 500kHz)

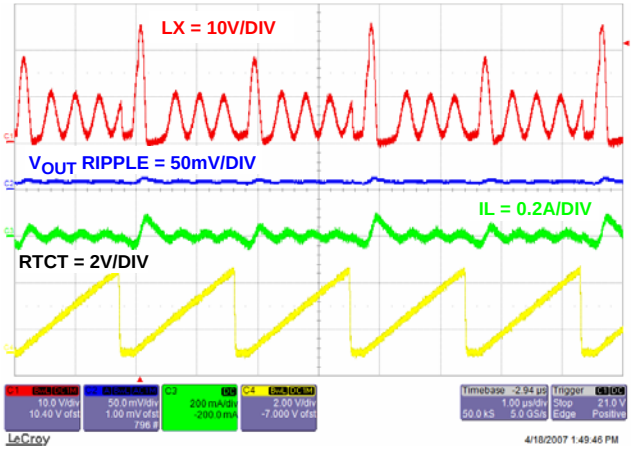


FIGURE 19. STEADY STATE OPERATION AT NO LOAD

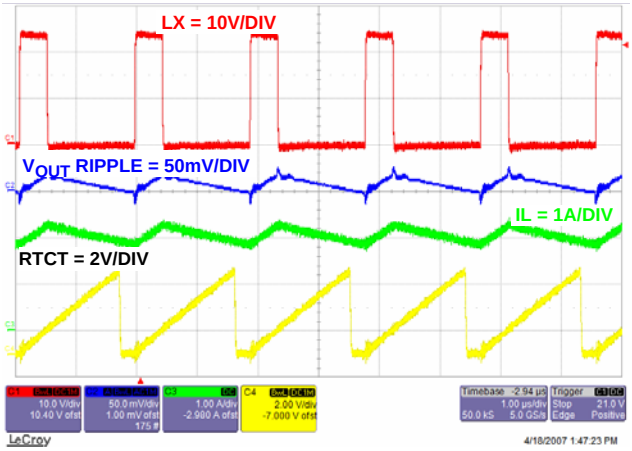


FIGURE 20. STEADY STATE OPERATION WITH FULL LOAD

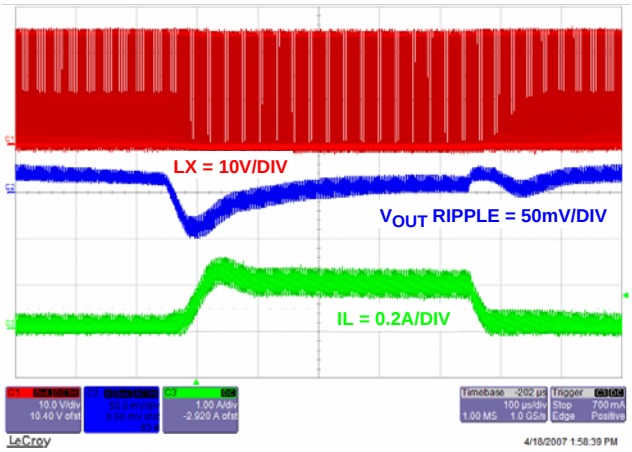


FIGURE 21. LOAD TRANSIENT

Typical Performance Curves

Circuit of Figure 2, V_{IN} = 24V, EN# = 0V, FS = 500KHz, V_{OUT} = 5V, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

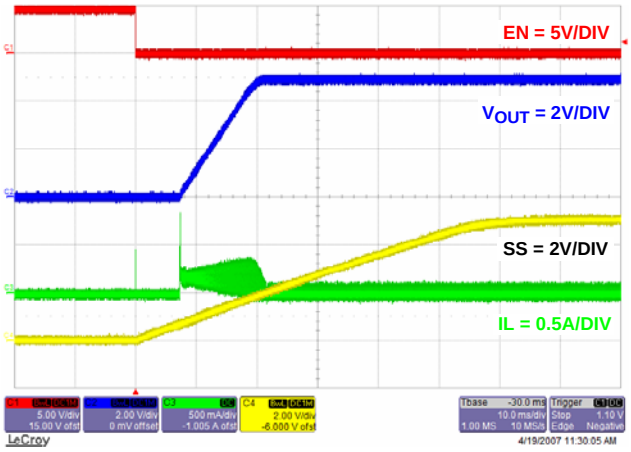


FIGURE 22. SOFT-START AT NO LOAD

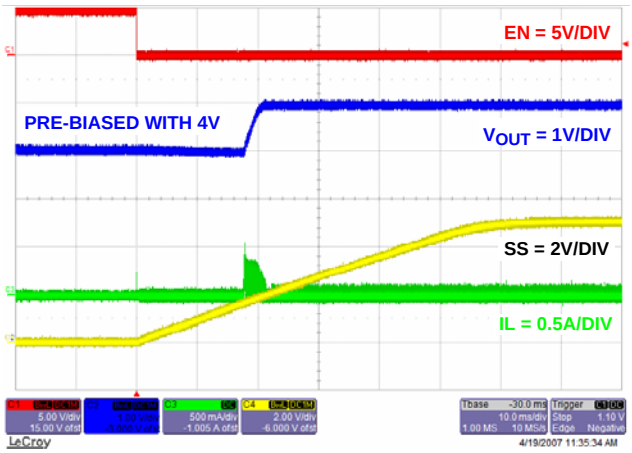


FIGURE 23. SOFT-START WITH PRE-BIASED

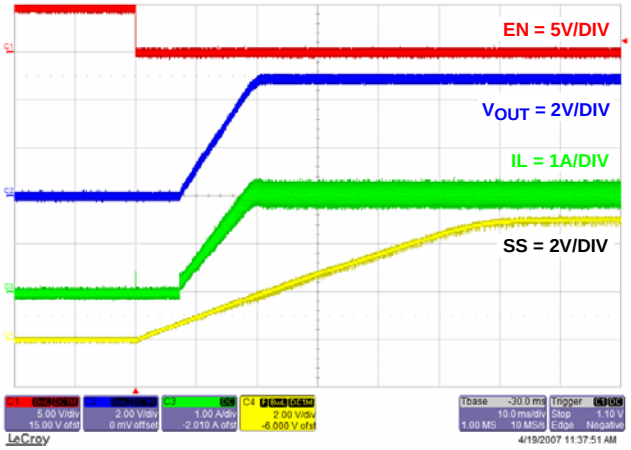


FIGURE 24. SOFT-START AT FULL LOAD

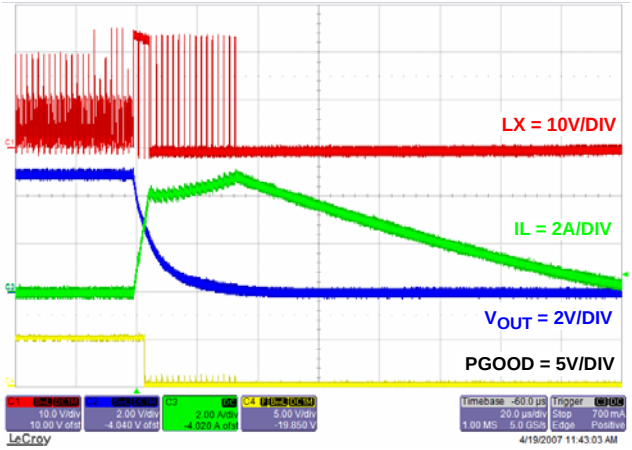


FIGURE 25. OUTPUT SHORT CIRCUIT

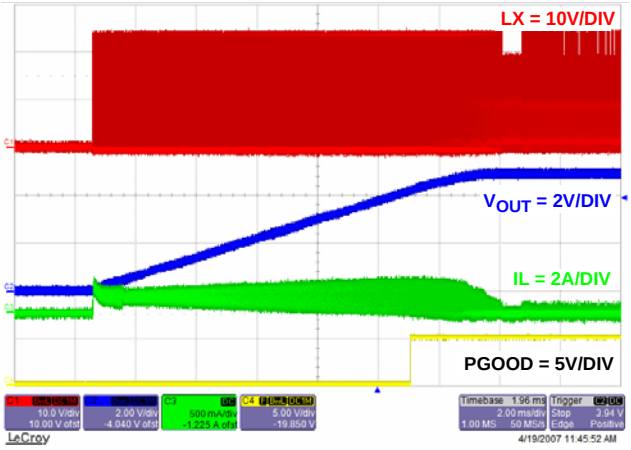


FIGURE 26. OUTPUT SHORT CIRCUIT

Applications Information

Product Description

The ISL8540 is a non-synchronous, integrated FET 2A step-down regulator which operates from an unregulated input of 9V to 40V. The output voltage is user-adjustable with a pair of external resistors. Frequency of operation is adjustable from 100kHz to 600kHz set by RTCT. An external signal with higher frequency can be injected to SYNCH to synchronize the controller.

The buck controller drives an internal N-Channel MOSFET and requires an external diode to deliver load current up to 2A. A Schottky diode is recommended for improved efficiency and performance over a standard diode. The converter output is regulated down to 1.21V from an input source. These features make the ISL8540 ideally suited for telecommunication power applications.

The PWM control loop uses a single output voltage loop with input voltage feed forward which simplifies feedback loop compensation and rejects input voltage variation. External feedback loop compensation allows flexibility in output filter component selection.

The buck regulator is equipped with a lossless current limit scheme. The current limit in the buck regulator is achieved by monitoring the drain-to-source current of the internal switching power MOSFET. The current limit threshold is internally set at 4.5A peak. Additional feature includes programable soft-start to support proper start up of wide output capacitance range.

Start-Up and Shut-Down

When the EN# pin is connected to a logic high, the ISL8540 is in the shut-down mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 110µA.

When the EN# pin is tied to GND, and V_{IN} reaches approximately 9V, the regulator begins to switch. The output voltage is gradually increased to ensure proper soft-start operation.

When the EN# reaches logic LOW, the regulator repeats the start-up procedure, including the soft-start function. Connect a capacitor from SS pin to ground. This capacitor, along with an internal 10µA current source sets the soft-start interval of the converter, T_{SS}.

$$C_{SS}[\mu F] \approx 8.3 \cdot T_{SS}[s] \quad \text{(EQ. 1)}$$

Operating Frequency

The ISL8540 can operate at switching frequencies from 100kHz to 600kHz. A resistor tied from the RTCT pin to VIN and a capacitor from RTCT to GND are used to program the switching frequency through the following equation.

$$C_1[nF] = \frac{6.25}{R[k\Omega]}\left(\frac{1000}{f_{OSC}[kHz]} - 0.3\right) \quad \text{(EQ. 2)}$$

Caution: When the ISL8540 is in disabled state, the voltage across RTCT pin will reach V_{IN} voltage. Make sure that the voltage rating of the RTCT capacitor is rated as high as the input voltage.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 28.

The output voltage programming resistor, R_3, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 1kΩ and 10kΩ.

$$R_3 = \frac{R_2 \times 1.21V}{V_{OUT} - 1.21V} \quad \text{(EQ. 3)}$$

If the output voltage desired is 1.21V, then R_3 is left unpopulated.

Fault Protection

The ISL8540 monitors the output of the regulator for overcurrent and undervoltage events. The ISL8540 also provides protection from excessive junction temperatures.

Overcurrent Protection

The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1 and the overcurrent condition flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are sixteen sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result with the regulator attempting to restart in a hiccup mode with the delay between restarts being 4 soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC fault counter reaching a count of four, the overcurrent condition flag will set back to LOW.

If the overcurrent condition flag is HIGH and the overcurrent fault counter is less than four and an undervoltage event is detected, the regulator will be shut down immediately.

Undervoltage Protection

If the voltage detected on the FB pin falls 14% below the internal reference voltage and the overcurrent condition flag is LOW, then the regulator will be shut down immediately under an undervoltage fault condition. An undervoltage fault condition will result with the regulator attempting to restart in a hiccup mode with the delay between restarts being 4 soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset and soft-start is attempted again.

Thermal Protection

If the ISL8540 IC junction temperature reaches a nominal temperature of +150°C, the regulator will be disabled. The ISL8540 will not re-enable the regulator until the junction temperature drops below +135°C.

Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

The shape of the output voltage waveform during a load transient that represents the worst case loading conditions will ultimately determine the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the Equivalent Series Resistance (ESR).

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

During the removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. This hump, as with the sag, can be attributed to the total amount of capacitance on the output. Figure 27 shows a typical response to a load transient.

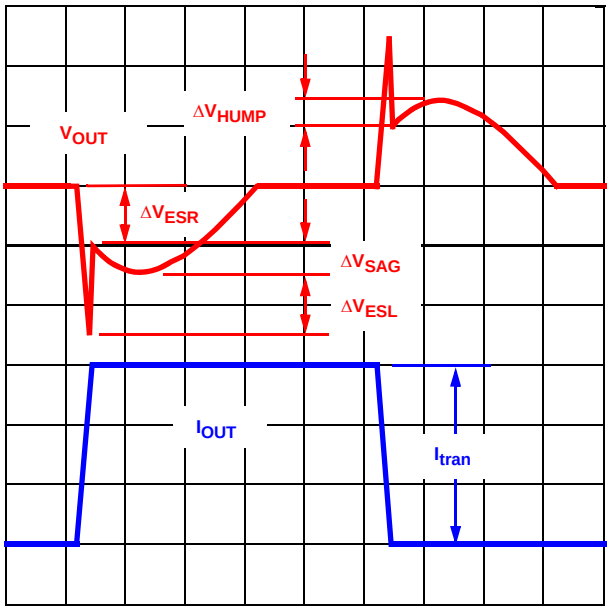


FIGURE 27. TYPICAL TRANSIENT RESPONSE

The amplitudes of the different types of voltage excursions can be approximated by using the formulas in Equation 4:

$$\Delta V_{ESR} = ESR \bullet I_{tran} \qquad \Delta V_{ESL} = ESL \bullet \frac{dI_{tran}}{dt}$$

$$\Delta V_{SAG} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet (V_{in} - V_{out})}$$

$$\Delta V_{HUMP} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet V_{out}} \qquad \text{(EQ. 4)}$$

where

I_{tran} = Output Load Current Transient

C_{out} = Total Output Capacitance

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and the ESL are typically the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using the following equation that relates the ESR and ESL of the capacitors to the transient load step and the voltage limit (ΔV_O):

$$\text{Number of Caps} = \frac{\frac{ESL \bullet dI_{tran}}{dt} + ESR \bullet I_{tran}}{\Delta V_o} \qquad \text{(EQ. 5)}$$

If ΔV_{SAG} and/or ΔV_{HUMP} are found to be too large for the output voltage limits, then the amount of capacitance may need to be increased. In this situation, a trade off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in Equations 4 and 5, is not usually listed in databooks.

Practically, it can be approximated if an impedance vs frequency curve is given for a specific capacitor (C):

$$ESL = \frac{1}{C(2 \bullet \pi \bullet f_{res})^2} \quad \text{(EQ. 6)}$$

where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency).

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 7:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient. Use ΔI of approximately 30% of I_{OUT} is a good compromise.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL8540 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 8 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 8)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Rectifier Selection

Current circulates from ground to the junction of the MOSFET and the inductor when the high-side switch is off. As a consequence, the polarity of the switching node is negative with respect to ground. This voltage is approximately -0.5V (a Schottky diode drop) during the off time. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor. The power dissipation is:

$$P_D[W] = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(EQ. 9)}$$

where V_D is the voltage of the Schottky diode = 0.5V to 0.7V

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the VIN's pin. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the VIN and PGND pins.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current through the input capacitors may be closely approximated through Equation 10:

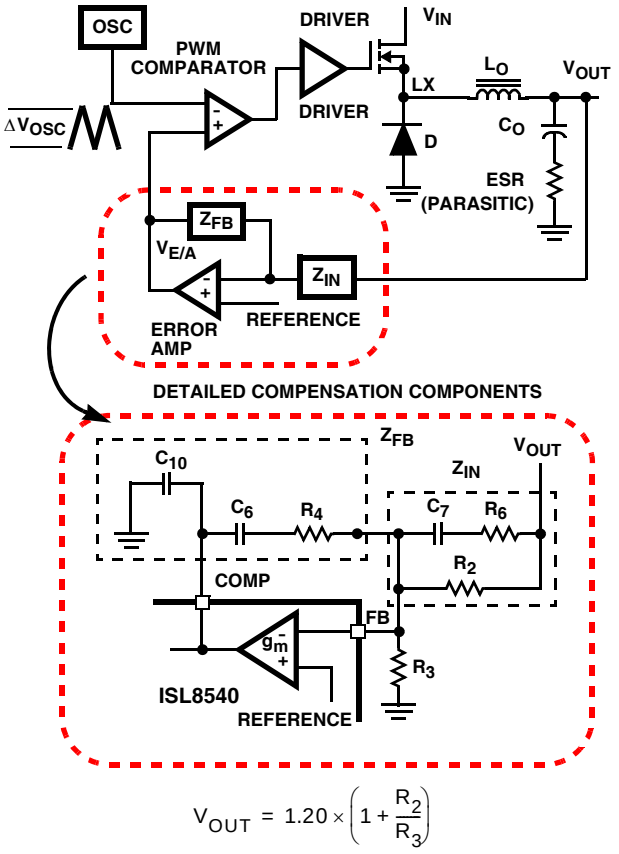
$$\sqrt{\frac{V_{OUT}}{V_{IN}} \times \left({I_{OUT_{MAX}}}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_{OSC}} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \right)} \quad \text{(EQ. 10)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Feedback Compensation

Figure 28 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the LX node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at f_{LC} and a zero at f_{ESR}. The DC Gain of



$$V_{OUT} = 1.20 \times \left(1 + \frac{R_2}{R_3}\right)$$

FIGURE 28. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}. The ISL8540 incorporates a feed forward loop that accounts for changes in the input voltage. This maintains a constant modulator gain.

Modulator Break Frequency Equations

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad f_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \qquad \text{(EQ. 11)}$$

The compensation network consists of the transconductance amplifier (internal to the ISL8540) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The equations in the following section relate the compensation network's poles, zeros and gain to the components (R_2, R_3, R_4, R_6, C_{10}, C_6, and C_7) in Figure 28. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain ($R_3 gm/(R_2+R_3)$) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% f_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error transconductance's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$f_{Z1} = \frac{1}{2\pi \cdot \frac{(R_4 \cdot g_m + 1)}{g_m} \cdot C_6} \qquad f_{P1} = \frac{1}{2\pi R_6 \cdot C_7} \qquad \text{(EQ. 12)}$$

$$f_{Z2} = \frac{1}{2\pi R_2 \cdot C_7} \qquad f_{P2} = \frac{1}{2\pi R_4 \cdot C_{10}}$$

Assumption: R6<<R2, R6<<R3, and C10<<C6.

Figure 29 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 29. Using the guidelines on page 13 should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 29 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

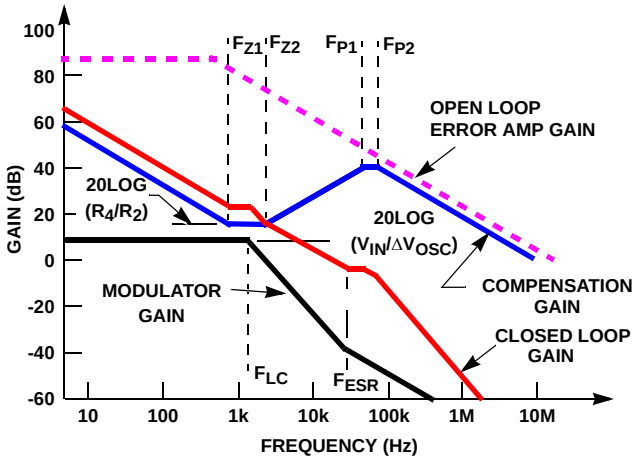


FIGURE 29. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A more detailed explanation of voltage mode control of a buck regulator can be found in Tech Brief TB417, titled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators."

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently

between 100kHz and 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the control MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the freewheeling Schottky diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL8540 switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

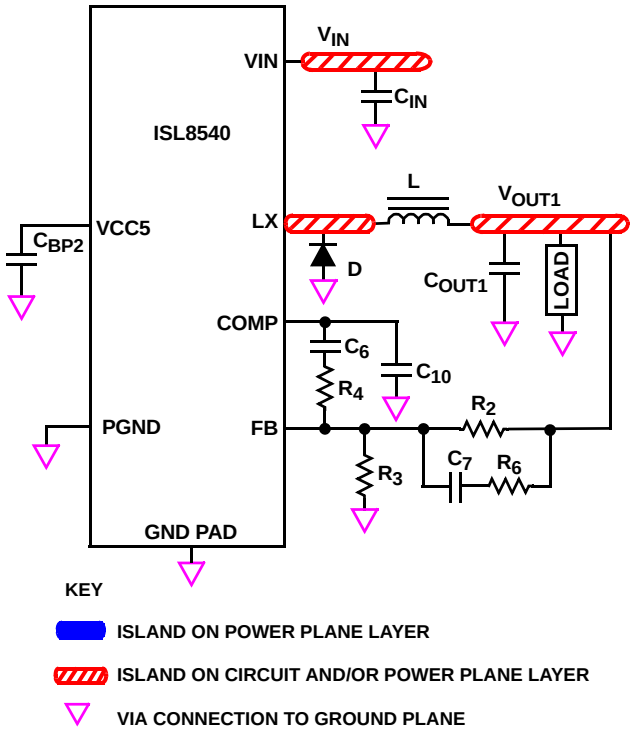


FIGURE 30. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

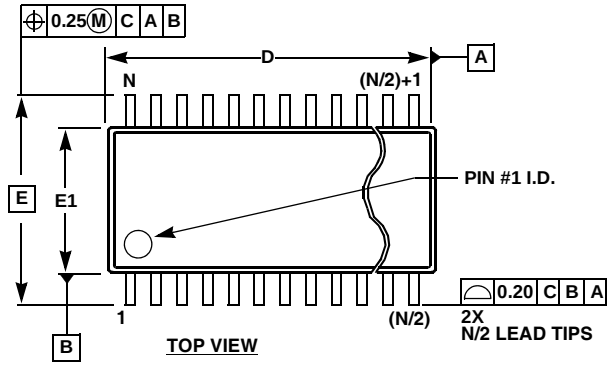
A multi-layer printed circuit board is recommended. Figure 30 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the LX terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the LX nodes. Use the remaining printed circuit layers for small signal wiring.

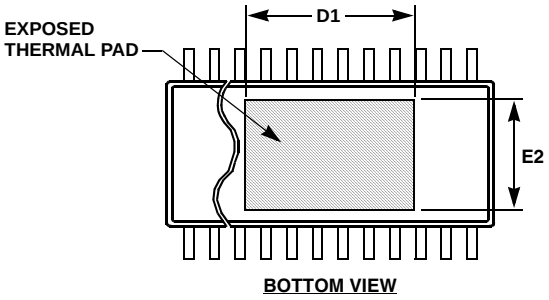
In order to dissipate heat generated by the internal LDO and other power components, the ground pad at the bottom of the device should be connected to the ground plane through at least nine vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

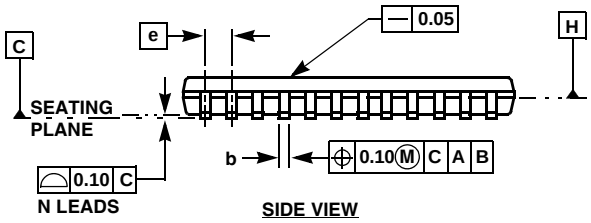
The switching components should be placed close to the ISL8540 first. Minimize the length of the connections between the input capacitors, C_{IN}. Make the PGND and the output capacitors as short as possible.

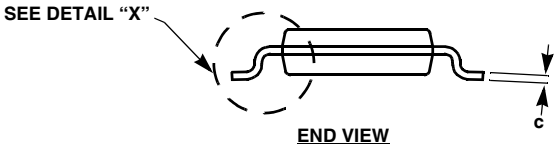
NOTE: It is recommended that any applications with input voltage greater than 30VDC should be polymer coated to meet Intersil's IPC-2221 creepage and clearance specification.

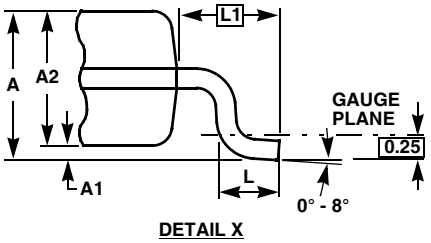
HTSSOP (Heat-Sink TSSOP) Family











MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.