ISL28005

Micropower, Rail-to-Rail Input Current Sense Amplifier with Voltage Output

ISL28005

The ISL28005 is a micropower, uni-directional high-side and low-side current sense amplifier featuring a proprietary rail-to-rail input current sensing amplifier. The ISL28005 is ideal for high-side current sense applications where the sense voltage is usually much higher than the amplifier supply voltage. The device can be used to sense voltages as high as 28V when operating from a supply voltage as low as 2.7V. The micropower ISL28005 consumes only 50µA of supply current when operating from a 2.7V to 28V supply.

The ISL28005 features a common-mode input voltage range from 0V to 28V. The proprietary architecture extends the input voltage sensing range down to 0V, making it an excellent choice for low-side ground sensing applications. The benefit of this architecture is that a high degree of total output accuracy is maintained over the entire 0V to 28V common mode input voltage range.

The ISL28005 is available in fixed (100V/V, 50V/V and 20V/V) gains in the space saving 5 Ld SOT-23 package. The parts operate over the extended temperature range from -40°C to +125°C.

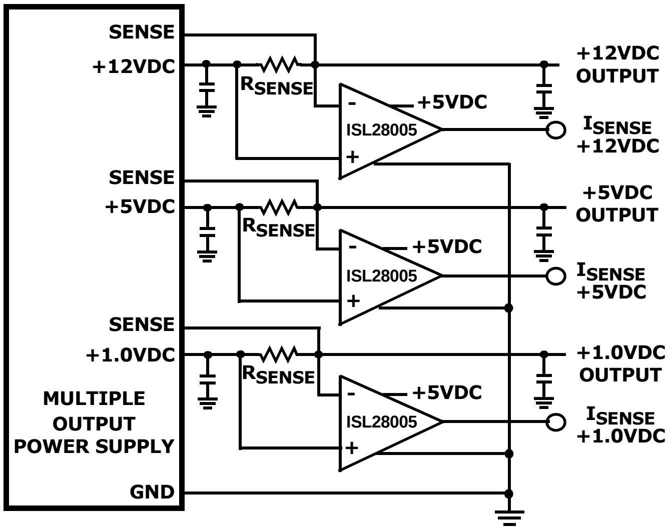
Features

- Low Power Consumption 50µA,Typ
- Supply Range. . . . . 2.7V to 28V
- Wide Common Mode Input . . . . 0V to 28V
- Fixed Gain Versions
  - ISL28005-100. . . . . 100V/V
  - ISL28005-50. . . . . 50V/V
  - ISL28005-20. . . . . 20V/V
- Operating Temperature Range . . -40°C to +125°C
- Package . . . . .5 Ld SOT-23

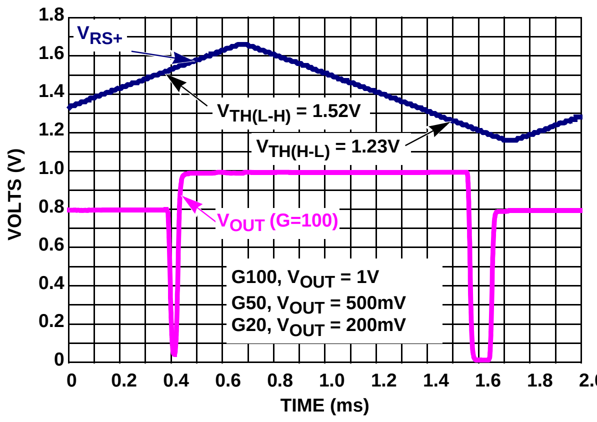
Applications* (see page 13)

- Power Management/Monitors
- Power Distribution and Safety
- DC/DC, AC/DC Converters
- Battery Management /Charging
- Automotive Power Distribution

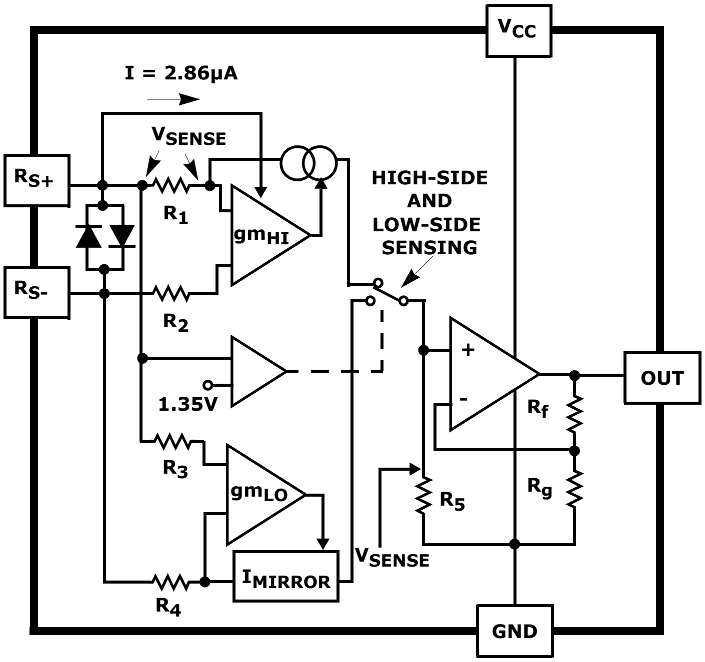
Typical Application



High-Side And Low-Side Threshold Voltage

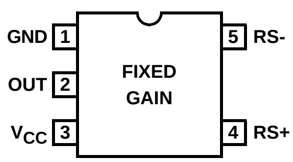


Block Diagram



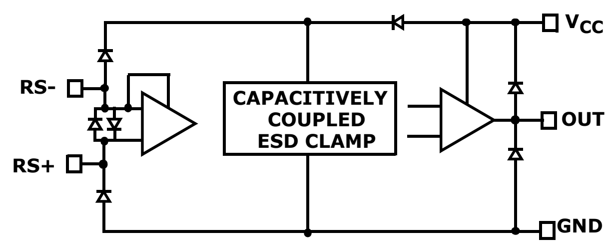
Pin Configuration

ISL28005
(5 LD SOT-23)
TOP VIEW



Pin Descriptions

ISL28005 (5 LD SOT-23)	PIN NAME	DESCRIPTION
1	GND	Power Ground
2	OUT	Amplifier Output
3	V_{CC}	Positive Power Supply
4	RS+	Sense Voltage Non-inverting Input
5	RS-	Sense Voltage Inverting Input



Ordering Information

PART NUMBER (Notes 1, 2, 3)	GAIN	PART MARKING	PACKAGE Tape & Reel (Pb-Free)	PKG. DWG. #
ISL28005FH100Z-T7	100V/V	BDEA	5 Ld SOT-23	MDP0038
ISL28005FH50Z-T7	50V/V	BDDA	5 Ld SOT-23	MDP0038
ISL28005FH20Z-T7	20V/V	BDCA	5 Ld SOT-23	MDP0038

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28005. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Max Supply Voltage 28V
Max Differential Input Current 20mA
Max Differential Input Voltage . . . .±0.5V
Max Input Voltage (RS+, RS-).................. GND-0.5V to 30V
Max Input Current for Input Voltage <GND -0.5V . . .±20mA
Output Short-Circuit Duration . . . . Indefinite
ESD Rating
Human Body Model 4kV
Machine Model 200V
Charged Device Model 1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 (Notes 4, 5)	190	90

Maximum Storage Temperature Range . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . +150°C
Pb-Free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range(T_A) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θJC, the “case temp” location is taken at the package top center.

Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage (Notes 7, 8)	V_{CC} = V_{RS}+ = 12V, V_S = 20mV to = 100mV	-500 **-500**	60	500 **500**	µV
		V_{CC} = 12V, V_{RS}+ = 0.2V, V_S = 20mV, V_S = 100mV	-3 **-3.3**	-1.2	3 **3.3**	mV
I_{RS}+, I_{RS} -	Leakage Current	V_{CC} = 0V, V_{RS+} = 28V		0.041	1.2 **1.5**	µA
I_{RS}+	Gain = 100 + Input Bias Current	V_{RS}+ = 2V, V_{SENSE} = 5mV		4.7	6 **7**	µA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-500 **-600**	-425		nA
	Gain = 50, Gain = 20 +Input Bias Current	V_{RS}+ = 2V, V_{SENSE} = 5mV		4.7	6 **8**	µA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-700 **-840**	-432		nA
I_{RS} -	Input Bias Current	V_{RS}+ = 2V, V_{SENSE} = 5mV		5	50 **75**	nA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-125 **-130**	-45		nA
CMRR	Common Mode Rejection Ratio	V_{RS}+ = 2V to 28V	**105**	**115**		dB
PSRR	Power Supply Rejection Ratio	V_{CC} = 2.7V to 28V, V_{RS}+ = 2V	**90**	**105**		dB
VF_S	Full-scale Sense Voltage	V_{CC} = 28V, V_{RS}+ = 0.2V, 12V	200			mV
G	Gain (Note 7)	ISL28005-100		100		V/V
		ISL28005-50		50		V/V
		ISL28005-20		20		V/V

Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
G_A	Gain = 100 Gain Accuracy (Note 9)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-2 **-3**		2 **3**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV		-0.25		%
	Gain = 50, Gain = 20 Gain Accuracy (Note 9)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-2 **-3**		2 **3**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV	-3 **-4**	-0.31	3 **4**	%
V_{OA}	Gain = 100 Total Output Accuracy (Note 10)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-2.5 **-2.7**		2.5 **2.7**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV		-1.25		%
	Gain = 50, Gain = 20 Total Output Accuracy (Note 10)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-2.5 **-2.7**		2.5 **2.7**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV	-6 **-7**	-1.41	6 **7**	%
V_{OH}	Output Voltage Swing, High V_{CC} - V_{OUT}	I_O = -500µA, V_{CC} = 2.7V V_{SENSE} = 100mV V_{RS}+ = 2V		39	50	mV
V_{OL}	Output Voltage Swing, Low V_{OUT}	I_O = 500µA, V_{CC} = 2.7V V_{SENSE} = 0V, V_{RS}+ = 2V		30	50	mV
R_{OUT}	Output Resistance	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV I_{OUT} = 10µA to 1mA		6.5		Ω
I_{SC+}	Short Circuit Sourcing Current	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		4.8		mA
I_{SC-}	Short Circuit Sinking Current	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		8.7		mA
I_S	Gain = 100 Supply Current	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	59 **62**	µA
	Gain = 50, 20 Supply Current	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	62 **63**	µA
V_{CC}	Supply Voltage	Guaranteed by PSRR	**2.7**		**28**	V
SR	Gain = 100 Slew Rate	Pulse on RS+ pin, V_{OUT} = 8V_{P-P} (see Figure 15)	0.58	0.76		V/µs
	Gain = 50 Slew Rate	Pulse on RS+ pin, V_{OUT} = 8V_{P-P} (see Figure 15)	0.58	0.67		V/µs
	Gain = 20 Slew Rate	Pulse on RS+ pin, V_{OUT} = 3.5V_{P-P} (see Figure 15)	0.50	0.67		V/µs
BW_{-3dB}	Gain = 100 -3dB Bandwidth	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		110		kHz
	Gain = 50 -3dB Bandwidth	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		160		kHz
	Gain = 20 -3dB Bandwidth	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		180		kHz

Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
t_S	Output Settling Time to 1% of Final Value	V_{CC} = V_{RS}+ = 12V, V_{OUT} = 10V step, V_{SENSE} >7mV		15		µs
		V_{CC} = V_{RS}+ = 0.2V, V_{OUT} = 10V step, V_{SENSE} >7mV		20		µs
	Capacitive-Load Stability	No sustained oscillations		300		pF
t_S Power-up	Power-Up Time to 1% of Final Value	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV		15		µs
		V_{CC} = 12V, V_{RS}+ = 0.2V V_{SENSE} = 100mV		50		µs
	Saturation Recovery Time	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV, overdrive		10		µs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. DEFINITION OF TERMS:
   - $V_{SENSE}A$ = V_{SENSE} @100mV
   - $V_{SENSE}B$ = V_{SENSE} @20mV
   - $V_{OUT}A$ = V_{OUT}@$V_{SENSE}A$=100mV
   - $V_{OUT}B$ = V_{OUT}@$V_{SENSE}B$=20mV
   - $G = GAIN = \left(\frac{V_{OUT}A - V_{OUT}B}{V_{SENSE}A - V_{SENSE}B}\right)$
8. V_{OS} is extrapolated from the gain measurement. $V_{OS} = V_{SENSE}A - \frac{V_{OUT}A}{G}$
9. % Gain Accuracy = $G_A = \left(\frac{G_{MEASURED} - G_{EXPECTED}}{G_{EXPECTED}}\right) \times 100$
10. Output Accuracy % $V_{OA} = \left(\frac{VOUT_{MEASURED} - VOUT_{EXPECTED}}{VOUT_{EXPECTED}}\right) \times 100$ where V_{OUT} = V_{SENSE} X GAIN and V_{SENSE} = 100mV

Typical Performance Curves V_{CC} = 12V, R_L = 1M, unless otherwise specified.

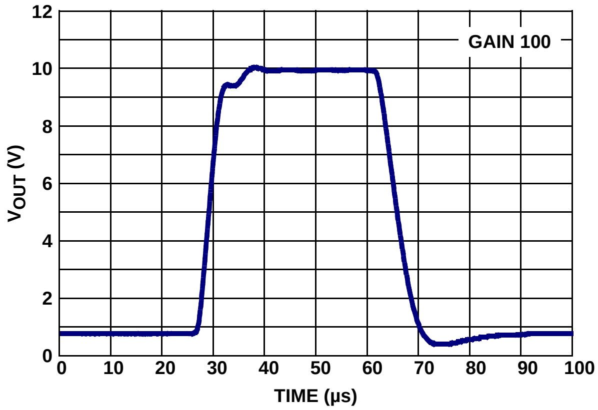


FIGURE 1. LARGE SIGNAL TRANSIENT RESPONSE V_{RS+} = 0.2V, V_{SENSE} = 100mV

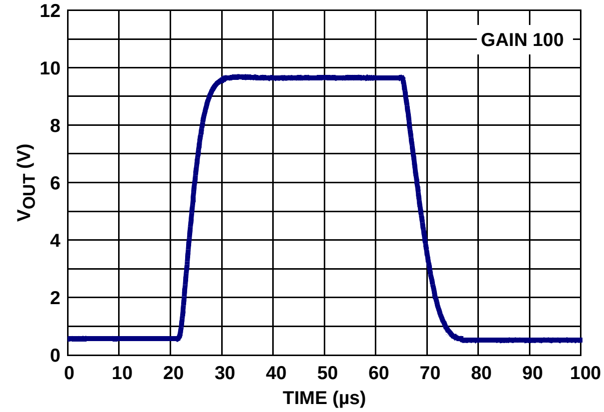


FIGURE 2. LARGE SIGNAL TRANSIENT RESPONSE V_{RS+} =12V, V_{SENSE} = 100mV

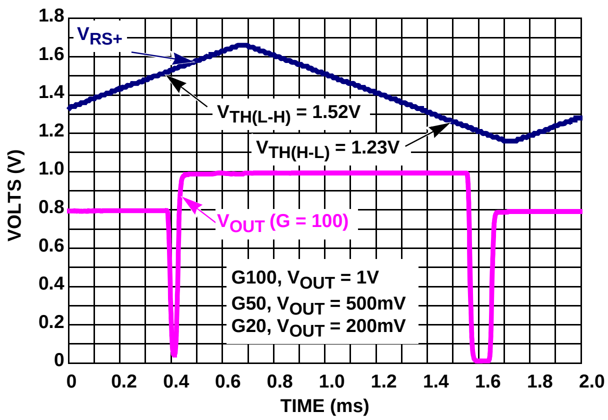


FIGURE 3. HIGH-SIDE and LOW-SIDE THRESHOLD VOLTAGE $V_{RS+(L-H)}$ and $V_{RS+(H-L)}$, V_{SENSE} = 10mV

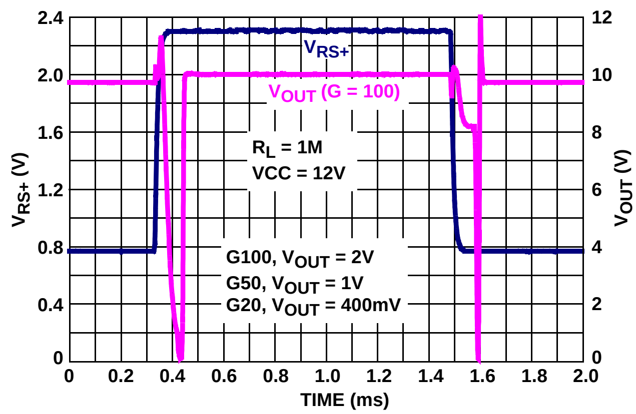


FIGURE 4. V_{OUT} vs V_{RS+}, V_{SENSE} = 20mV TRANSIENT RESPONSE

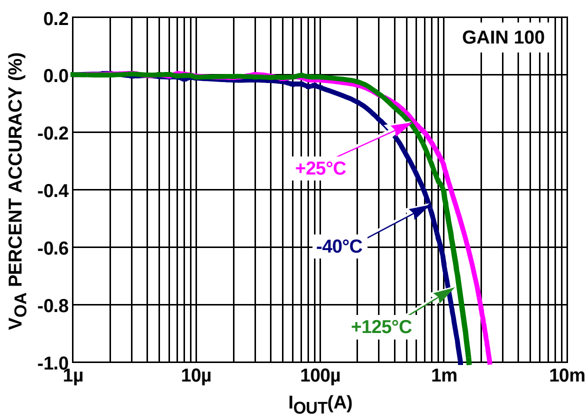


FIGURE 5. NORMALIZED V_{OA} vs I_{OUT}

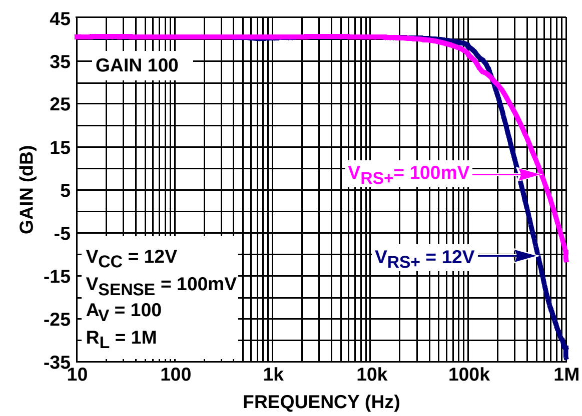


FIGURE 6. GAIN vs FREQUENCY V_{RS+}= 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV$_{P-P}$

Typical Performance Curves V_{CC} = 12V, R_L = 1M, unless otherwise specified. (Continued)

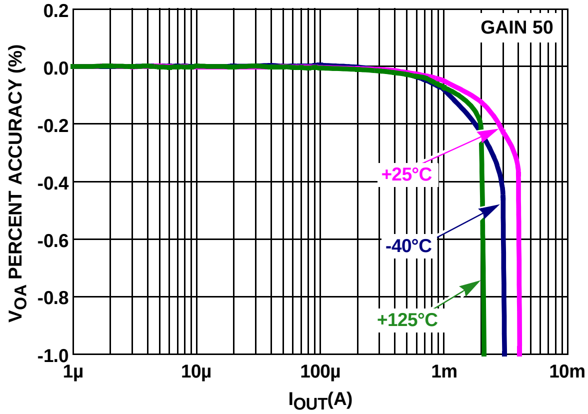


FIGURE 7. NORMALIZED V_{OA} vs I_{OUT}

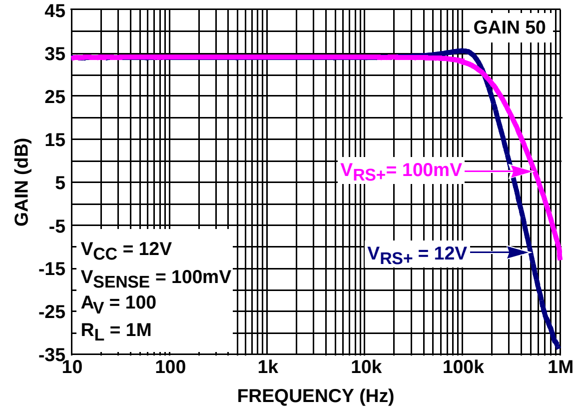


FIGURE 8. GAIN vs FREQUENCY V_{RS+}=100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV_{P-P}

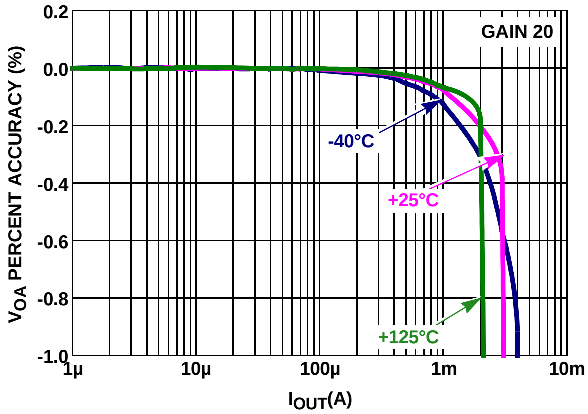


FIGURE 9. NORMALIZED V_{OA} vs I_{OUT}

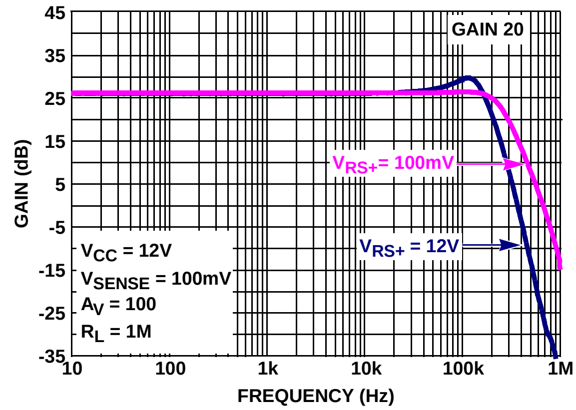


FIGURE 10. GAIN vs FREQUENCY V_{RS+}=100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV_{P-P}

Test Circuits and Waveforms

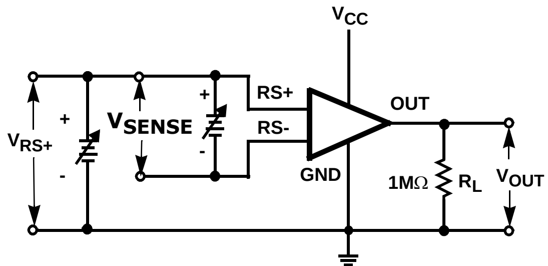


FIGURE 11. I_S, V_{OS}, V_{OA}, CMRR, PSRR, GAIN ACCURACY

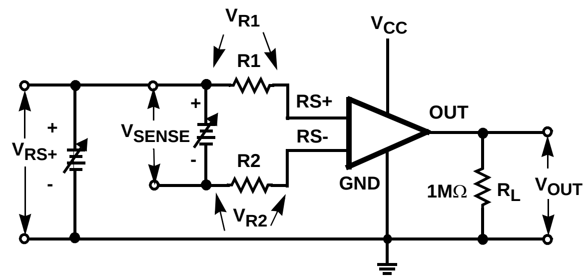


FIGURE 12. INPUT BIAS CURRENT, LEAKAGE CURRENT

Test Circuits and Waveforms (Continued)

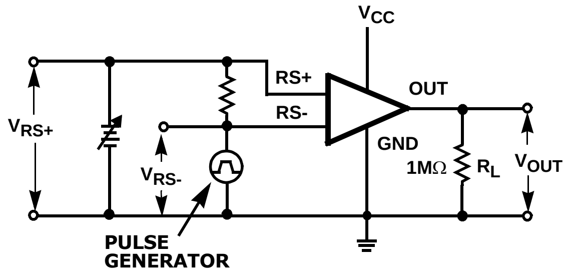


FIGURE 13. SLEW RATE, t_S, SATURATION RECOVERY TIME

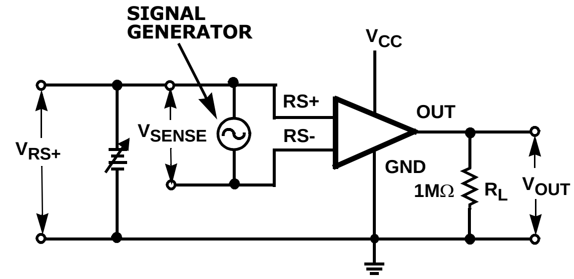


FIGURE 14. GAIN vs FREQUENCY

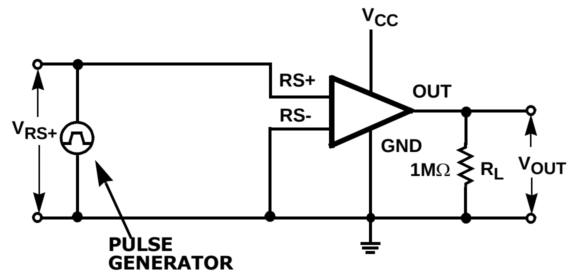


FIGURE 15. SLEW RATE

Applications Information

Functional Description

The ISL28005-20, ISL28005-50 and ISL28005-100 are single supply, uni-directional current sense amplifiers with fixed gains of 20V/V, 50V/V and 100V/V respectively.

The ISL28005 is a 2-stage amplifier. Figure 16 shows the active circuitry for high-side current sense applications where the sense voltage is between 1.35V to 28V. Figure 17 shows the active circuitry for ground sense applications where the sense voltage is between 0V to 1.35V.

The first stage is a bi-level trans-conductance amp and level translator. The gm stage converts the low voltage drop (V_{SENSE}) sensed across an external milli-ohm sense resistor, to a current (@ gm = 21.3µA/V). The trans-conductance amplifier forces a current through R_1 resulting to a voltage drop across R_1 that is equal to the sense voltage (V_{SENSE}). The current through R_1 is mirrored across R_5 creating a ground-referenced voltage at the input of the second amplifier equal to V_{SENSE}.

The second stage is responsible for the overall gain and frequency response performance of the device. The fixed gains (20, 50, 100) are set with internal resistors R_f and R_g. The only external component needed is a current sense resistor (typically 0.001Ω to 0.01Ω, 1W to 2W).

The transfer function is given in Equation 1.

$$V_{OUT} = GAIN \times (I_S R_S + V_{OS}) \qquad \text{(EQ. 1)}$$

The input gm stage derives its ~2.86µA supply current from the input source through the RS+ terminal as long as the sensed voltage at the RS+ pin is >1.35V and the gm_{HI} amplifier is selected. When the sense voltage at R_S+ drops below the 1.35V threshold, the gm_{LO} amplifier kicks in and the gm_{LO} output current reverses, flowing out of the RS- pin.

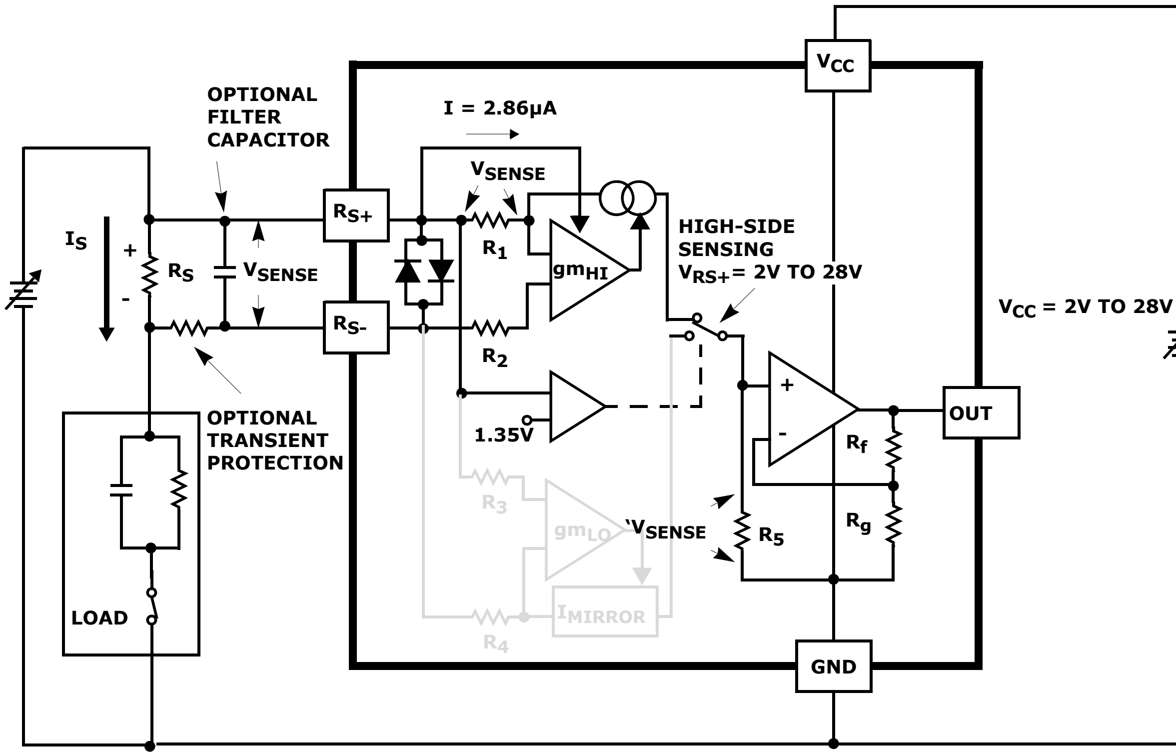


FIGURE 16. HIGH-SIDE CURRENT DETECTION

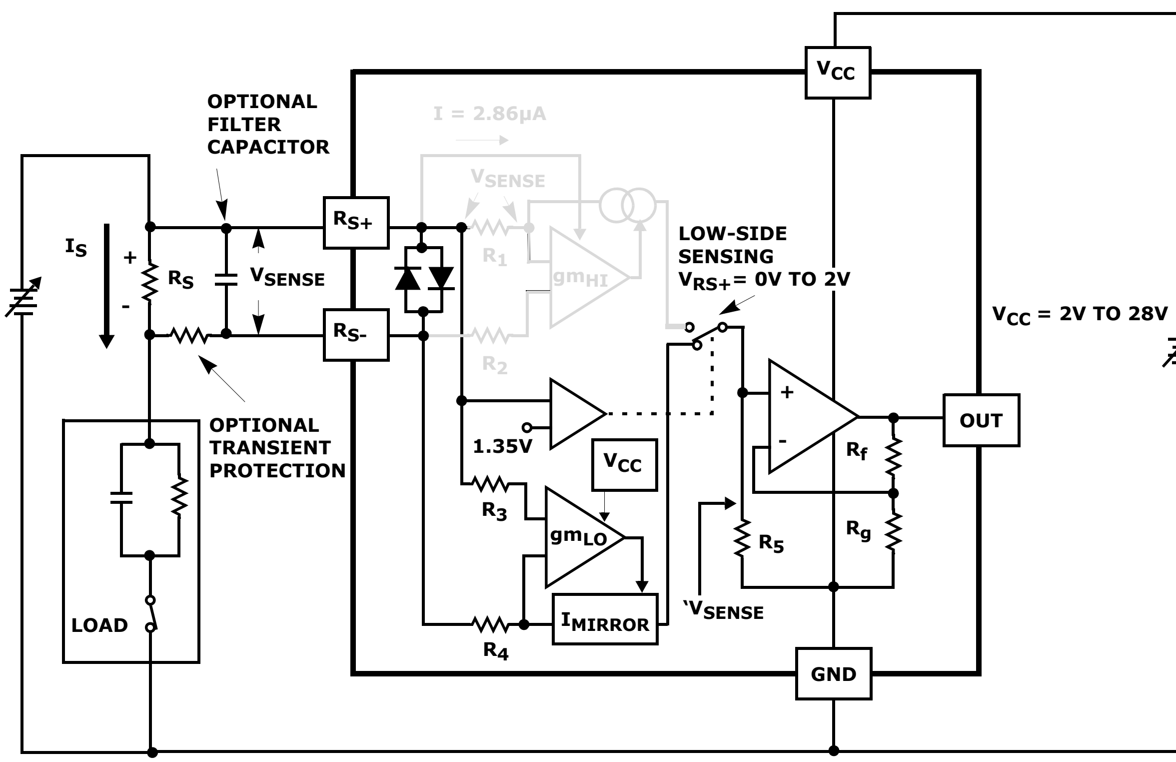


FIGURE 17. LOW-SIDE CURRENT DETECTION

Hysteretic Comparator

The input trans-conductance amps are under control of a hysteretic comparator operating from the incoming source voltage on the RS+ pin (see Figure 18). The comparator monitors the voltage on RS+ and switches the sense amplifier from the low-side gm amp to the high-side gm amplifier whenever the input voltage at R_S+ increases above the 1.35V threshold. Conversely, a decreasing voltage on the RS+ pin, causes the hysteric comparator to switch from the high-side gm amp to the low-side gm amp as the voltage decreases below 1.35V. It is that low-side sense gm amplifier that gives the ISL28005 the proprietary ability to sense current all the way to 0V. Negative voltages on the R_S+ or R_S- are beyond the sensing voltage range of this amplifier.

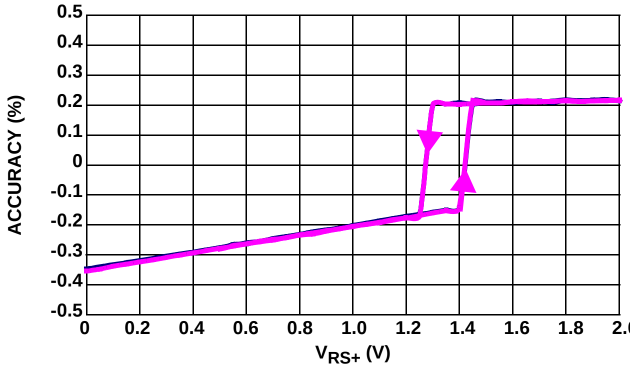


FIGURE 18. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

Typical Application Circuit

Figure 20 shows the basic application circuit and optional protection components for switched-load applications. For applications where the load and the power source is permanently connected, only an external sense resistor is needed. For applications where fast transients are caused by hot plugging the source or load, external protection components may be needed. The external current limiting resistor (R_P) in Figure 20 may be required to limit the peak current through the internal ESD diodes to < 20mA. This condition can occur in applications that experience high levels of in-rush current causing high peak voltages that can damage the internal ESD diodes. An R_P resistor value of 100Ω will provide protection for a 2V transient with the maximum of 20mA flowing through the input while adding only an additional 13µV (worse case over-temperature) of V_{OS}. Refer to the following formula:

$((R_P \times I_{RS-}) = (100\Omega \times 130nA) = 13\mu V)$

Switching applications can generate voltage spikes that can overdrive the amplifier input and drive the output of the amplifier into the rails, resulting in a long overload recovery time. Capacitors C_M and C_D filter the common mode and differential voltage spikes.

Error Sources

There are 3 dominant error sources: gain error, input offset voltage error and Kelvin voltage error (see Figure 19). The gain error is dominated by the internal resistance matching tolerances. The remaining errors appear as sense voltage errors at the input to the amplifier. They are V_{OS} of the amplifier and Kelvin voltage errors. If the transient protection resistor is added, an additional V_{OS} error can result from the IxR voltage due to input bias current. The limiting resistor should only be added to the R_S- input, due to the high-side gm amplifier (gm_{HI}) sinking several micro amps of current through the RS+ pin.

Layout Guidelines

Kelvin Connected Sense Resistor

The source of Kelvin voltage errors is illustrated in Figure 19. The resistance of 1/2 oz. copper is ~1mΩ per square with a TC of ~3900ppm/°C (0.39%/°C). When you compare this unwanted parasitic resistance with the total of 1mΩ to 10mΩ resistance of the sense resistor, it is easy to see why the sense connection must be chosen very carefully. For example, consider a maximum current of 20A through a 0.005Ω sense resistor, generating a V_{SENSE} = 0.1 and a full scale output voltage of 10V (G = 100). Two side contacts of only 0.25 square per contact puts the V_{SENSE} input about 0.5 x 1mΩ away from the resistor end capacitor. If only 10A the 20A total current flows through the kelvin path to the resistor, you get an error voltage of 10mV (10A x 0.5sq x 0.001Ω/sq. = 10mV) added to the 100mV sense voltage for a sense voltage error of 10% (0.110V - 0.1)/0.1V)x 100.

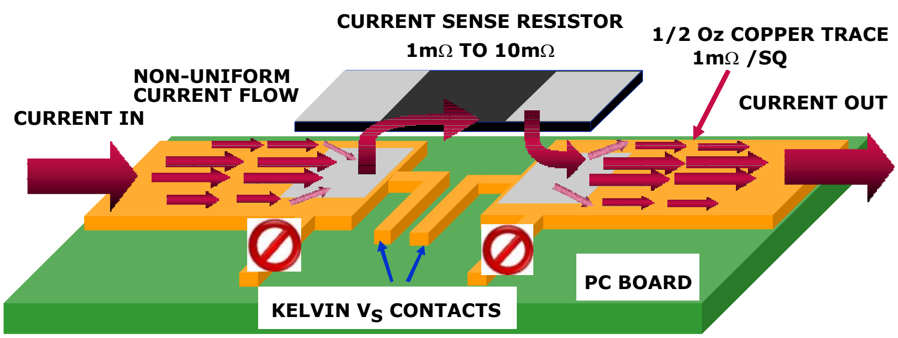


FIGURE 19. PC BOARD CURRENT SENSE KELVIN CONNECTION

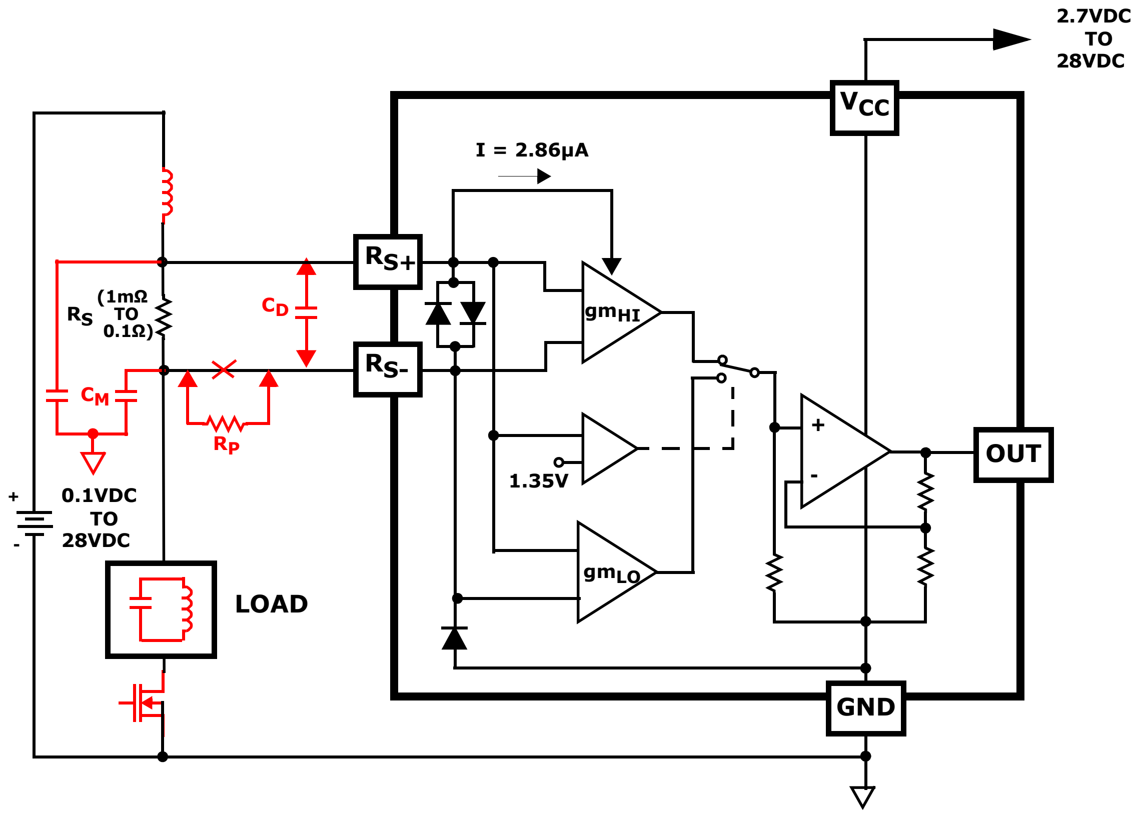


FIGURE 20. TYPICAL APPLICATION CIRCUIT

Overall Accuracy (V_{OA} %)

V_{OA} is defined as the total output accuracy Referred-to-Output (RTO). The output accuracy contains all offset and gain errors, at a single output voltage. Equation 2 is used to calculate the % total output accuracy.

$$V_{OA} = 100 \times \left(\frac{V_{OUT}\text{actual} - V_{OUT}\text{expected}}{V_{OUT}\text{expected}}\right) \quad \text{(EQ. 2)}$$

where

V_{OUT} Actual = V_{SENSE} x GAIN

Example: Gain = 100, For 100mV V_{SENSE} input we measure 10.1V. The overall accuracy (V_{OA}) is 1% as shown in Equation 3.

$$V_{OA} = 100 \times \left(\frac{10.1 - 10}{10}\right) = 1\text{percent} \quad \text{(EQ. 3)}$$

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 4:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 4)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 5:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ.5)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_{CC} = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

R_L = Load resistance

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
2/3/10	FN6973.1	-Page1: Edited last sentence of paragraph 2. Moved order of GAIN listings from 20, 50, 100 to 100, 50, 20 in the 3rd paragraph. Under Features ....removed "Low Input Offset Voltage 250µV,max" Under Features .... moved order of parts listing from 20, 50, 100 (from top to bottom) to 100, 50, 20. -Page 3: Removed coming soon on ISL28005FH50Z and ISL28005FH20Z and changes the order or listing them to 100, 50, 20. -Page 5: VOA test. Under conditions column ...deleted “20mV to”. It now reads ... Vsense = 100mV SR test. Under conditions column ..deleted what was there. It now reads ... Pulse on RS+pin, See Figure 15 -Page 6: ts test. Removed Gain = 100 and Gain = 100V/V in both description and conditions columns respectively. -Page 9 Added Figure 15 and adjusted figure numbers to account for the added figure.
12/14/09	FN6973.0	Initial Release

Products

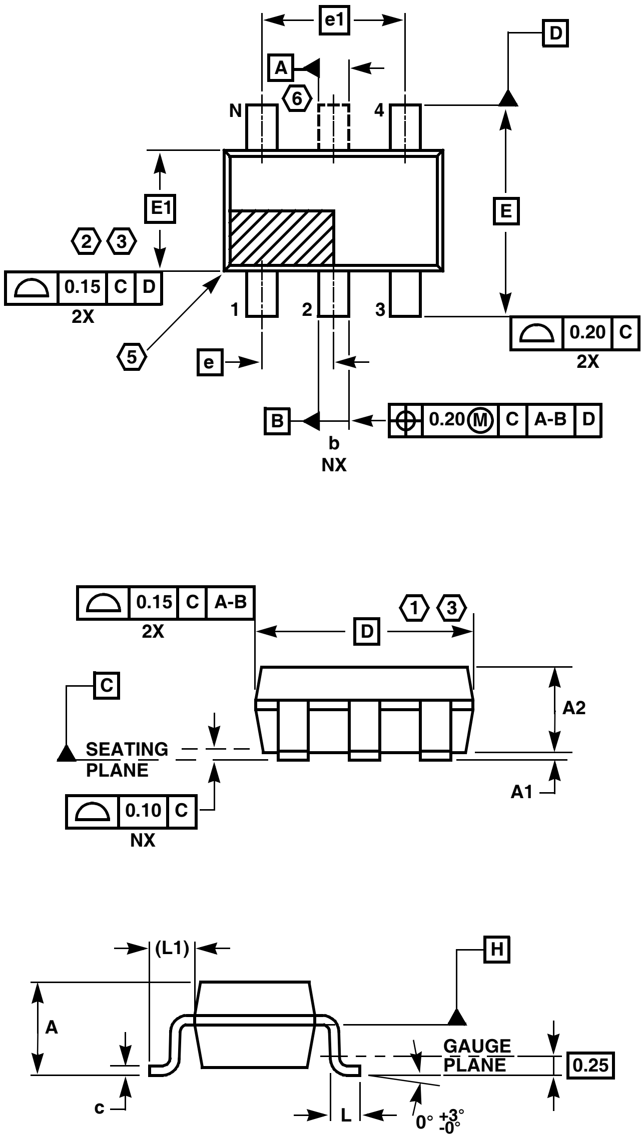
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28005

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).