ISL22323

Dual Digitally Controlled Potentiometer (XDCP™)

Data Sheet | May 31, 2007 | FN6422.0

Low Noise, Low Power, I²C® Bus, 256 Taps

The ISL22323 integrates two digitally controlled potentiometers (DCP), control logic and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. The potentiometer has an associated volatile Wiper Register (WRi) and a non-volatile Initial Value Register (IVRi) that can be directly written to and read by the user. The contents of the WRi control the position of the corresponding wiper. At power up the device recalls the contents of the DCP's IVRi to the correspondent WRi.

The ISL22323 also has 13 general purpose non-volatile registers that can be used as storage of lookup table for multiple wiper position or any other valuable information.

The ISL22323 features a dual supply, that is beneficial for applications requiring a bipolar range for DCP terminals between V- and VCC.

Each DCP can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Two potentiometers in one package
- 256 resistor taps
- I^2C serial interface
  - Two address pins, up to four devices per bus
- Non-volatile EEPROM storage of wiper position
- 13 General Purpose non-volatile registers
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- Wiper resistance: 70Ω typical @ 1mA
- Standby current <4µA max
- Shut-down current <4µA max
- Dual power supply
  - V_{CC} = 2.25V to 5.5V
  - V- = -2.25V to -5.5V
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40 to +125°C
- 14 lead TSSOP or 16 lead QFN
- Pb-free plus anneal product (RoHS compliant)

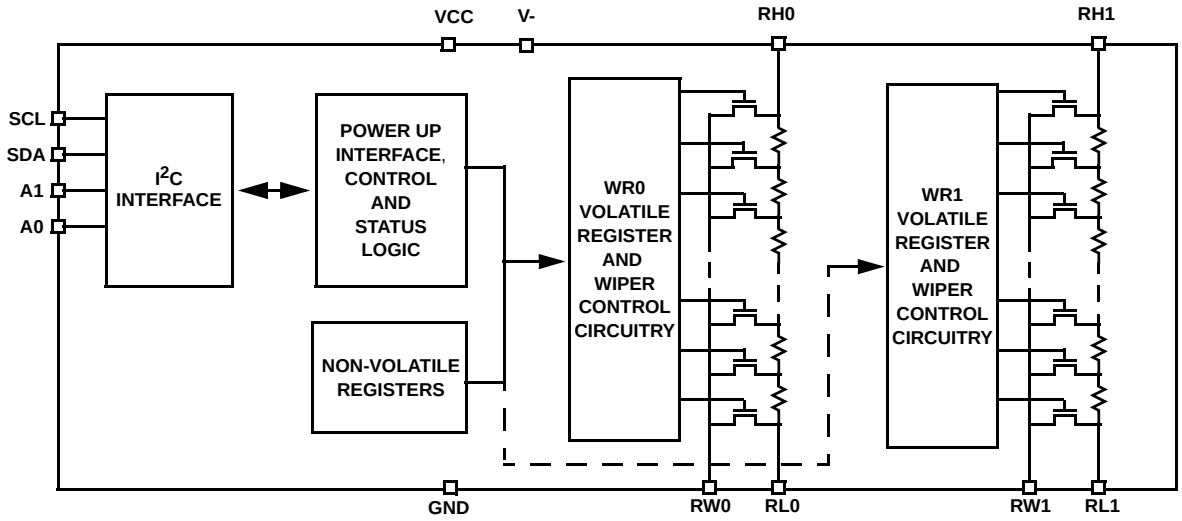
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL22323TFV14Z	22323 TFVZ	100	-40 to +125	14 Ld TSSOP	M14.173
ISL22323TFR16Z	223 23TFRZ	100	-40 to +125	16 Ld QFN	L16.4x4A
ISL22323UFV14Z	22323 UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL22323UFR16Z	223 23UFRZ	50	-40 to +125	16 Ld QFN	L16.4x4A
ISL22323WFV14Z	22323 WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173
ISL22323WFR16Z	223 23WFRZ	10	-40 to +125	16 Ld QFN	L16.4x4A

NOTES:

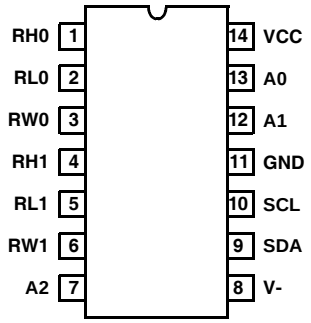
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram

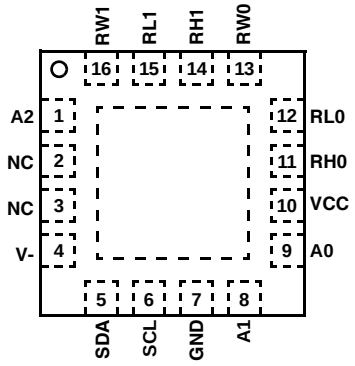


Pinouts

ISL22323
(14 LD TSSOP)
TOP VIEW



ISL22323
(16 LD QFN)
TOP VIEW



Pin Descriptions

TSSOP PIN	QFN PIN	SYMBOL	DESCRIPTION
1	11	RH0	“High” terminal of DCP0
2	12	RL0	“Low” terminal of DCP0
3	13	RW0	“Wiper” terminal of DCP0
4	14	RH1	“High” terminal of DCP1
5	15	RL1	“Low” terminal of DCP1
6	16	RW1	“Wiper” terminal of DCP1
7	1	A2	Device address input for the I^2C interface
8	4	V-	Negative power supply pin
9	5	SDA	Open drain Serial data I/O for the I^2C interface
10	6	SCL	I^2C interface clock input
11	7	GND	Device ground pin
12	8	A1	Device address input for the I^2C interface
13	9	A0	Device address input for the I^2C interface
14	10	VCC	Positive power supply pin
	2, 3	NC	No connection
	EPAD*		Exposed Die Pad internally connected to V-

* Note: PCB thermal land for QFN EPAD should be connected to V- plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf

Absolute Maximum Ratings

Storage Temperature . . . . . .-65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . .-0.3V to V_{CC}+0.3
V_{CC} . . . . . .-0.3V to +6V
V- . . . . . .-6V to 0.3V
Voltage at any DCP Pin with
respect to GND. . . . . V- to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A at +125°C
ESD
Human Body Model 3.5kV
Machine Model. 350V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
14 Lead TSSOP	105
16 Lead QFN	39

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Full Industrial) . . . . . .-40°C to +125°C
Power Rating 15mW
V_{CC} . . . . . 2.25V to 5.5V
V- . . . . . .-2.25V to -5.5V
Max Wiper Current Iw . . . . . .±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
R_{TOTAL}	RHi to RLi resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RHi to RLi resistance tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±85		ppm/°C
		U, T option		±45		ppm/°C
V_{RHi}, V_{RLi}	DCP terminal voltage	V_{RH} and V_{RL} to GND	V-		V_{CC}	V
R_W	Wiper resistance	RH - floating, V_{RL} = V-, force Iw current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$		70	250	Ω
$C_H/C_L/C_W$ (Note 18)	Potentiometer capacitance	See Macro Model below.		10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins	Voltage at pin from V- to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ RLi; V_{CC} @ RHi; measured at RWi, unloaded)						
INL (Note 9)	Integral non-linearity Monotonic over all tap positions	W option	-1.5	±0.5	1.5	LSB (Note 5)
		U, T option	-1.0	±0.2	1.0	LSB (Note 5)
DNL (Note 8)	Differential non-linearity Monotonic over all tap positions	W option	-1.0	±0.4	1.0	LSB (Note 5)
		U, T option	-0.5	±0.15	0.5	LSB (Note 5)
ZSerror (Note 6)	Zero-scale error	W option	0	1	5	LSB (Note 5)
		U, T option	0	0.5	2	
FSerror (Note 7)	Full-scale error	W option	-5	-1	0	LSB (Note 5)
		U, T option	-2	-1	0	
V_{MATCH} (Note 10, 18)	DCP to DCP matching	Wipers at the same tap position, the same voltage at all RH terminals and the same voltage at all RL terminals	-2		2	LSB (Note 5)

Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
TC_V (Note 11, 18)	Ratiometric temperature coefficient	DCP register set to 80 hex		±4		ppm/°C
f_{cutoff} (Note 18)	-3dB cut off frequency	Wiper at midpoint (80hex) W option (10k)		1000		kHz
		Wiper at midpoint (80hex) U option (50k)		250		kHz
		Wiper at midpoint (80hex) T option (100k)		120		kHz
RESISTOR MODE (Measurements between RWi and RLi with RHi not connected, or between RWi and RHi with RLi not connected)						
RINL (Note 15)	Integral non-linearity	W option	-3	±1.5	3	MI (Note 12)
		U, T option	-1	±0.4	1	MI (Note 12)
RDNL (Note 14)	Differential non-linearity	W option	-1.5	±0.5	1.5	MI (Note 12)
		U, T option	-0.5	±0.15	0.5	MI (Note 12)
Roffset (Note 13)	Offset	W option	0	1	5	MI (Note 12)
		U, T option	0	0.5	2	MI (Note 12)
R_{MATCH} (Note 16)	DCP to DCP matching	Wipers at the same tap position with the same terminal voltages	-2		2	MI (Note 12)
TC_R (Note 17, 18)	Resistance temperature coefficient	DCP register set between 32hex and FF hex		±40		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = 5.5V, f_{SCL} = 400kHz; (for I^2C Active, Read and Volatile Write states only)		0.01	0.2	mA
		V_{CC} = 2.25V, f_{SCL} = 400kHz; (for I^2C Active, Read and Volatile Write states only)		0.005	0.1	mA
I_{V-1}	V- Supply Current (volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCL} = 400kHz; (for I^2C Active, Read and Volatile Write states only)	-0.2	-0.05		mA
		V- = -2.25V, V_{CC} = 2.25V, f_{SCL} = 400kHz; (for I^2C Active, Read and Volatile Write states only)	-0.1	-0.02		mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = 5.5V, V- = 5.5V, f_{SCL} = 400kHz; (for I^2C Active, Read and Non-volatile Write states only)		1.0	2.0	mA
		V_{CC} = 2.25V, V- = -2.25V, f_{SCL} = 400kHz; (for I^2C Active, Read and Non-volatile Write states only)		0.3	1.0	mA
I_{V-2}	V- Supply Current (non-volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCL} = 400kHz; (for I^2C Active, Read and Non-volatile Write states only)	-2.0	-1.2		mA
	V- Supply Current (non-volatile write/read)	V- = -2.25V, V_{CC} = 2.25V, f_{SCL} = 400kHz; (for I^2C Active, Read and Non-volatile Write states only)	-1.0	-0.4		mA

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, I^2C interface in standby state		0.5	2.0	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, I^2C interface in standby state		1.0	4.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, I^2C interface in standby state		0.2	1.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, I^2C interface in standby state		0.5	2.0	µA
I_{V-SB}	V- Current (standby)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, I^2C interface in standby state	-3.0	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, I^2C interface in standby state	-5.0	-1.5		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, I^2C interface in standby state	-2.0	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, I^2C interface in standby state	-3.0	-0.4		µA
I_{SD}	V_{CC} Current (shut-down)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, I^2C interface in standby state		0.5	2.0	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, I^2C interface in standby state		1.0	4.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, I^2C interface in standby state		0.2	1.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, I^2C interface in standby state		0.5	2.0	µA
I_{V-SD}	V- Current (shut-down)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, I^2C interface in standby state	-3.0	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, I^2C interface in standby state	-5.0	-1.5		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, I^2C interface in standby state	-2.0	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, I^2C interface in standby state	-3.0	-0.4		µA
I_{LkgDig}	Leakage current, at pins A0, A1, SDA, and SCL	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{WRT} (Note 18)	DCP wiper response time	SCL falling edge of last bit of DCP data byte to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 18)	DCP recall time from shut-down mode	SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on recall voltage	Minimum V_{CC} at which memory recall occurs	1.9		2.1	V
VCCRamp	V_{CC} ramp rate		0.2			V/ms
t_D	Power-up delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			5	ms

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
t_{WC} (Note 19)	Non-volatile Write cycle time			12	20	ms
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, SDA, and SCL input buffer LOW voltage				$0.3*V_{CC}$	V
V_{IH}	A1, A0, SDA, and SCL input buffer HIGH voltage		$0.7*V_{CC}$			V
Hysteresis (Note 18)	SDA and SCL input buffer hysteresis		$0.05*V_{CC}$			V
V_{OL} (Note 18)	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
Cpin (Note 18)	A1, A0, SDA, and SCL pin capacitance				10	pF
f_{SCL}	SCL frequency				400	kHz
t_{sp}	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA} (Note 18)	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF} (Note 18)	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input data hold time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP condition hold time for read, or volatile only write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH} (Note 18)	Output data hold time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R (Note 18)	SDA and SCL rise time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 18)	SDA and SCL fall time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns

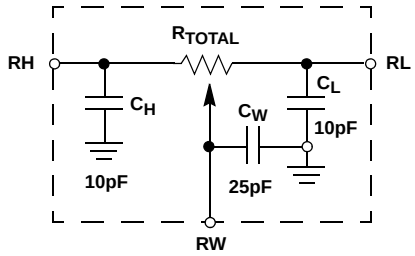
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
Cb (Note 18)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 18)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ
$t_{SU:A}$	A1 and A0 setup time	Before START condition	600			ns
$t_{HD:A}$	A1 and A0 hold time	After STOP condition	600			ns

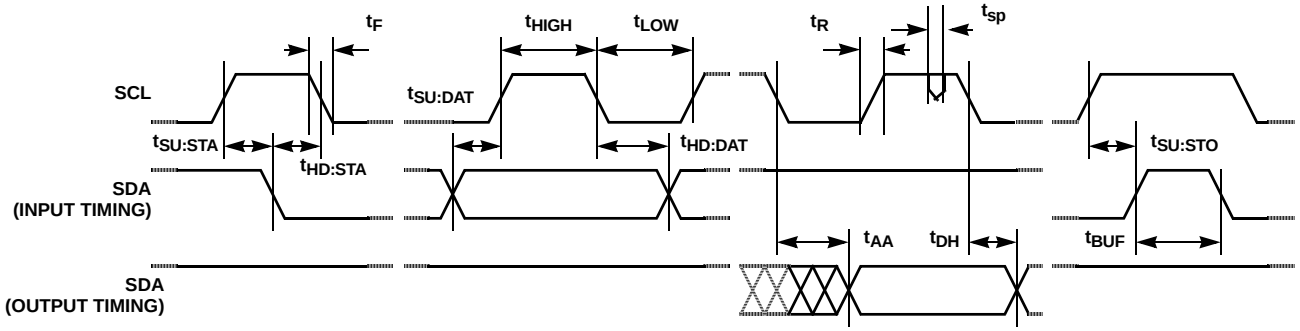
NOTES:

4. Typical values are for T_A = +25°C and 3.3V supply voltage.
5. LSB: $[V(R_W)_{255} – V(R_W)_0]/255$. $V(R_W)_{255}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
6. ZS error = $V(RW)_0$/LSB.
7. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
8. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
9. INL = $[V(RW)_i – i • LSB – V(RW)_0]$/LSB for i = 1 to 255
10. V_{MATCH}= [V(RWx)i -V(RWy)i]/LSB, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
11. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{255} – RW_0|$/255. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{255}/MI, when measuring between RW and RH.
14. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 16 to 255.
15. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 16 to 255.
16. R_{MATCH}= [(Rx)i -(Ry)i]/MI, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
17. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
18. This parameter is not 100% tested.
19. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I^2C serial interface, to the end of the self-timed internal non-volatile write cycle.

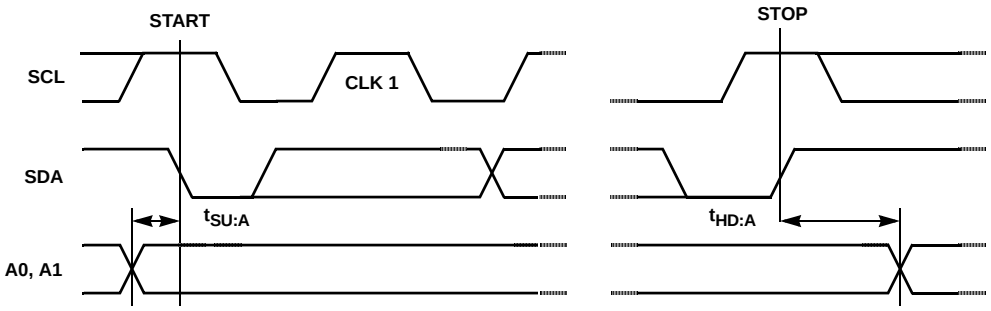
DCP Macro Model



SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

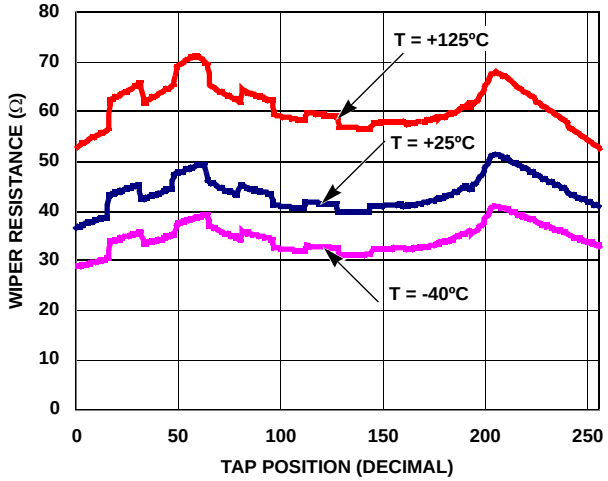


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

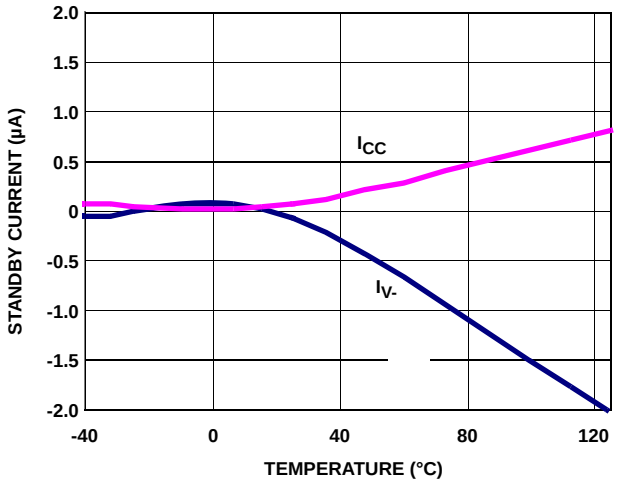


FIGURE 2. STANDBY I_{CC} and I_{V-} vs TEMPERATURE

Typical Performance Curves (Continued)

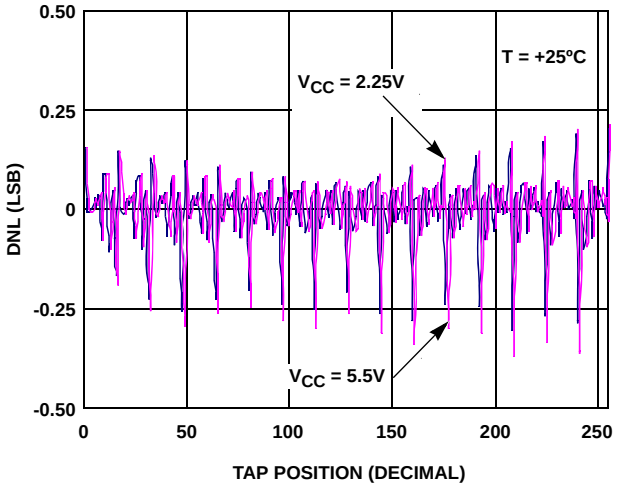


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

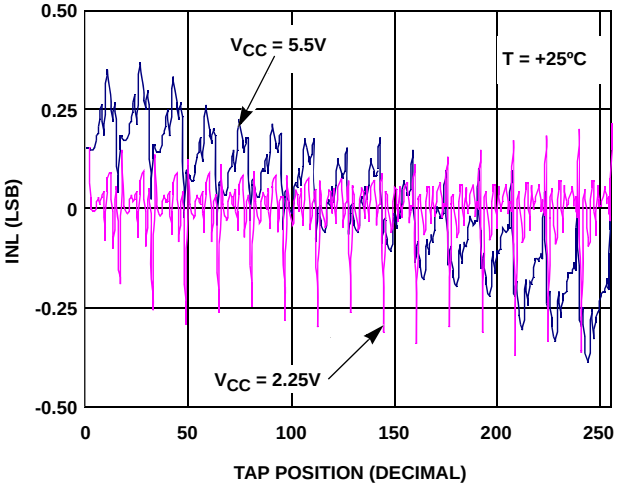


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

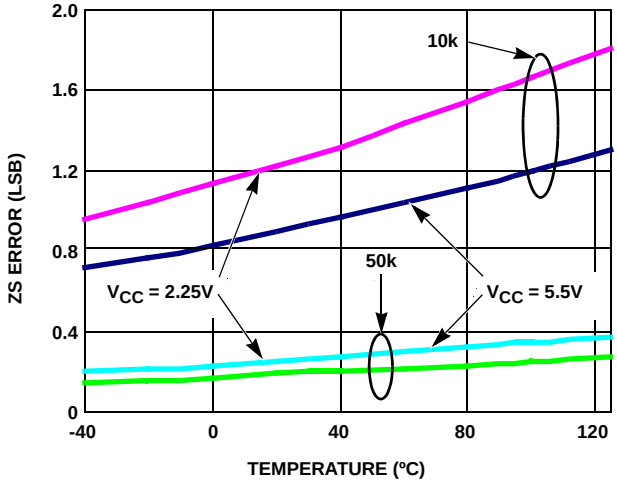


FIGURE 5. ZS ERROR vs TEMPERATURE

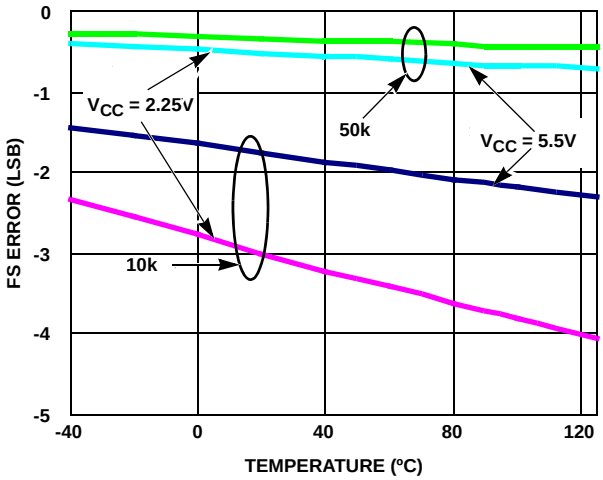


FIGURE 6. FS ERROR vs TEMPERATURE

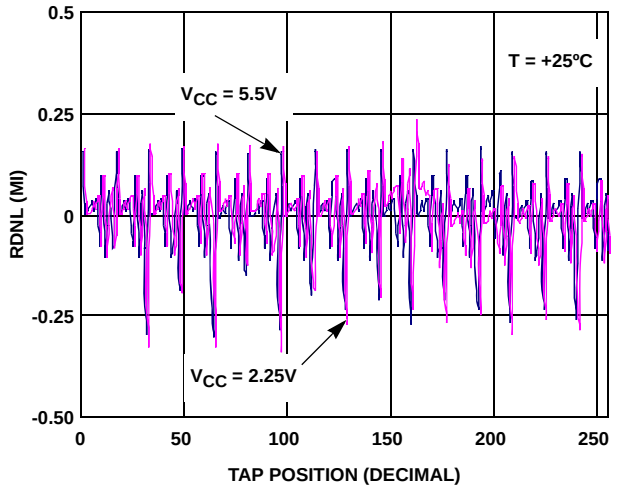


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

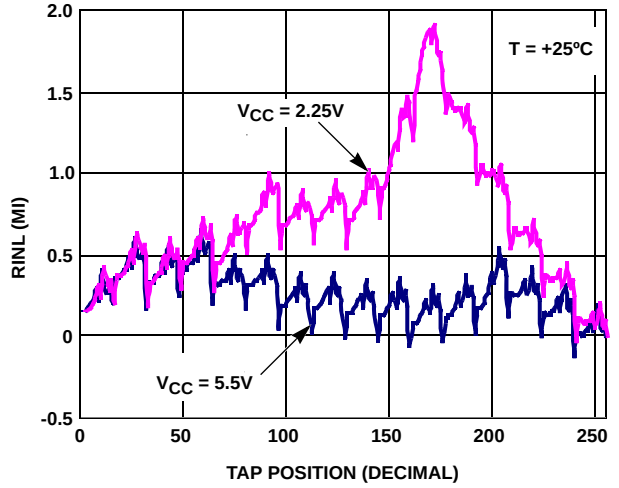


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

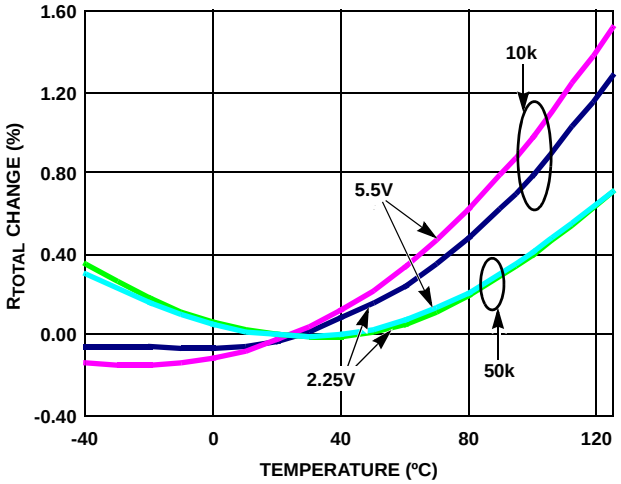


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

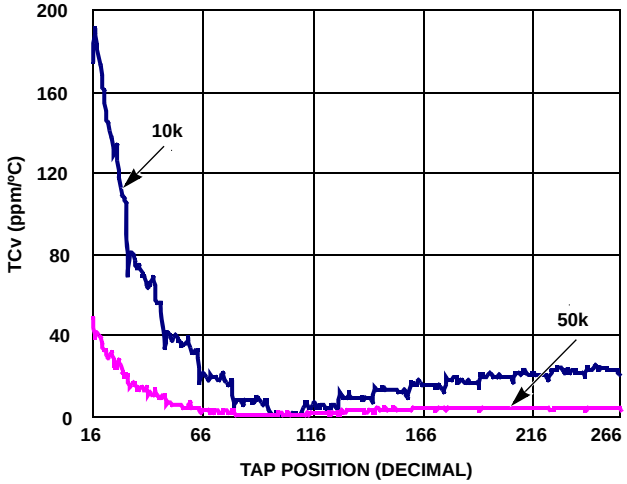


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

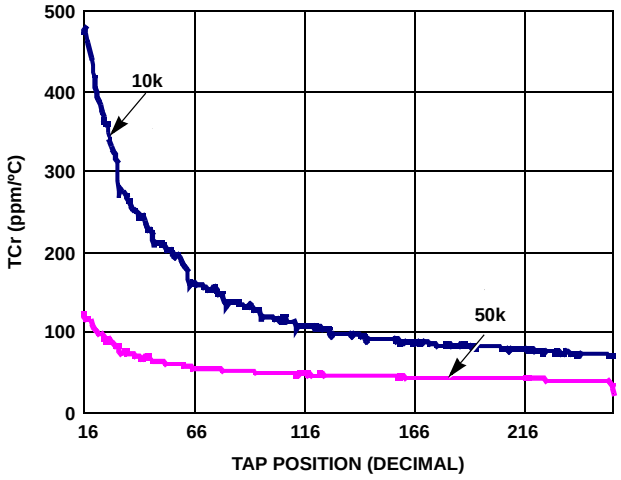


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

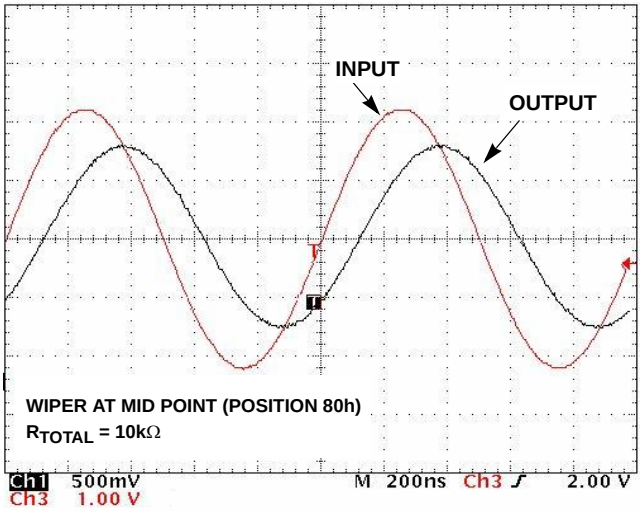


FIGURE 12. FREQUENCY RESPONSE (1MHz)

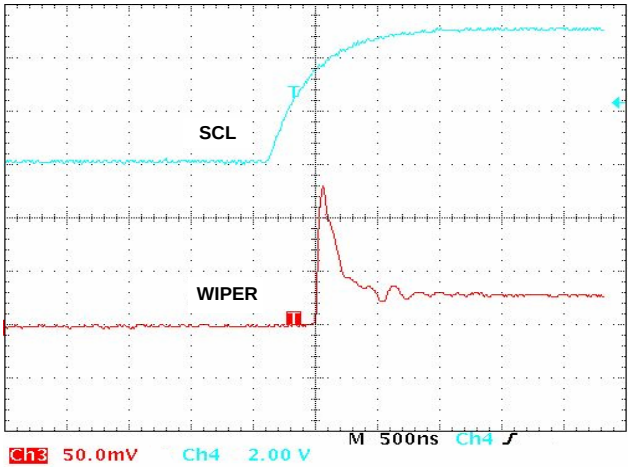


FIGURE 13. MIDSCALE GLITCH, CODE 7Fh TO 80h

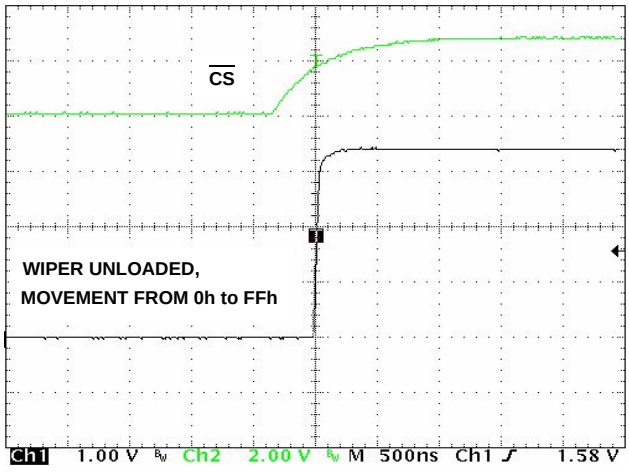


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometers Pins

RHI AND RLi

The high (RHi) and low (RLi) terminals of the ISL22323 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 255 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

RWi

RWi is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface. SCL requires an external pull-up resistor.

DEVICE ADDRESS (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22323. A maximum of four ISL22323 devices may occupy the I^2C serial bus (See Table 3).

Principles of Operation

The ISL22323 is an integrated circuit incorporating two DCPs with its associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor arrays are comprised of individual resistors connected in a series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to their initial positions.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RHi and RLi pins). The RWi pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WRi). When the WRi of a DCP contains all zeroes (WRi[7:0]= 00h), its wiper terminal (RWi) is closest to its “Low” terminal (RLi). When the WRi register of a DCP contains all ones (WRi[7:0]= FFh), its wiper terminal (RWi) is closest to its “High” terminal (RHi). As the value of the WRi increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RLi to the position closest to RHi. At the same time, the resistance between RWi and RLi increases monotonically, while the resistance between RHi and RWi decreases monotonically.

While the ISL22323 is being powered up, the WRi is reset to 80h (128 decimal), which locates RWi roughly at the center between RLi and RHi. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WRi will be reloaded with the value stored in corresponding non-volatile Initial Value Register (IVRi).

The WRi and IVRi can be read or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL22323 contains two non-volatile 8-bit Initial Value Register (IVRi), thirteen General Purpose non-volatile 8-bit registers and three volatile 8-bit registers: two Wiper Registers (WRi) and Access Control Register (ACR). Memory map of ISL22323 is in Table 1. The non-volatile registers (IVRi) at address 0 and 1, contain initial wiper position and volatile registers (WRi) contain current wiper position.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
10	N/A	ACR
F	Reserved	
E	General Purpose	N/A
D	General Purpose	N/A
C	General Purpose	N/A
B	General Purpose	N/A
A	General Purpose	N/A
9	General Purpose	N/A
8	General Purpose	N/A

TABLE 1. MEMORY MAP (Continued)

ADDRESS (hex)	NON-VOLATILE	VOLATILE
7	General Purpose	N/A
6	General Purpose	N/A
5	General Purpose	N/A
4	General Purpose	N/A
3	General Purpose	N/A
2	General Purpose	N/A
1	IVR1	WR1
0	IVR0	WR0

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WRi or initial value registers IVRi.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME	VOL	$\overline{SHDN}$	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVRi registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. Note: value is written to IVRi register also is written to the corresponding WRi. The default value of this bit is 0.

The $\overline{SHDN}$ bit (ACR[6]) disables or enables Shut-down mode. When this bit is 0, DCPs are in Shut-down mode. Default value of the $\overline{SHDN}$ bit is 1.

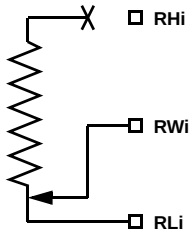


FIGURE 15. DCP CONNECTION IN SHUT-DOWN MODE

The WIP bit (ACR[5]) is a read-only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WRi or ACR while WIP bit is 1.

I²C Serial Interface

The ISL22323 supports an I^2C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22323 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 16). On power-up of the ISL22323, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22323 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 16). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 17).

The ISL22323 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22323 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 10100 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/$\overline{Write}$ bit. Its value is “1” for a Read operation and “0” for a Write operation (See Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT

LOGIC VALUES AT PINS A1 AND A0, RESPECTIVELY

1	0	1	0	0	A1	A0	R/$\overline{W}$
(MSB)							(LSB)

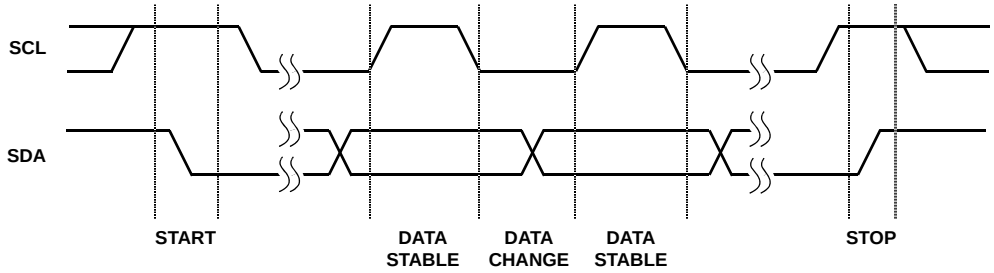


FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS

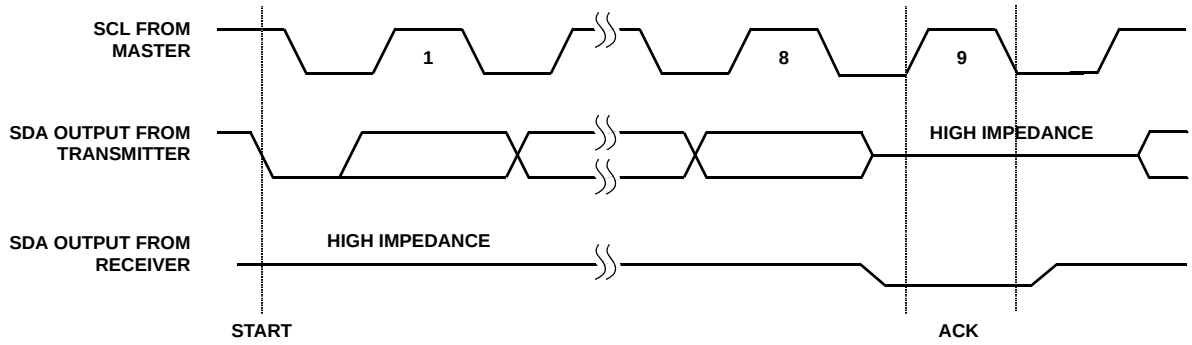


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

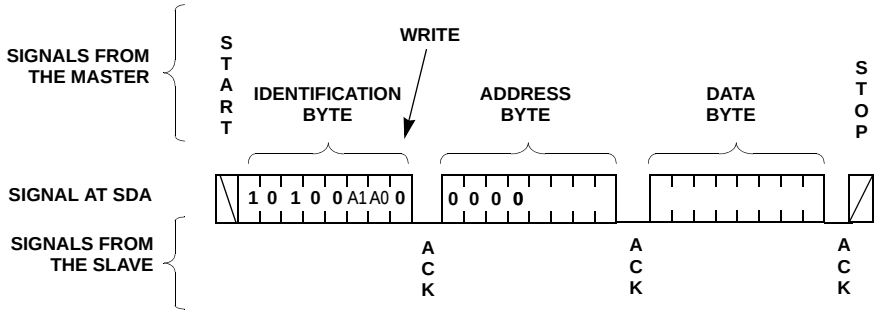


FIGURE 18. BYTE WRITE SEQUENCE

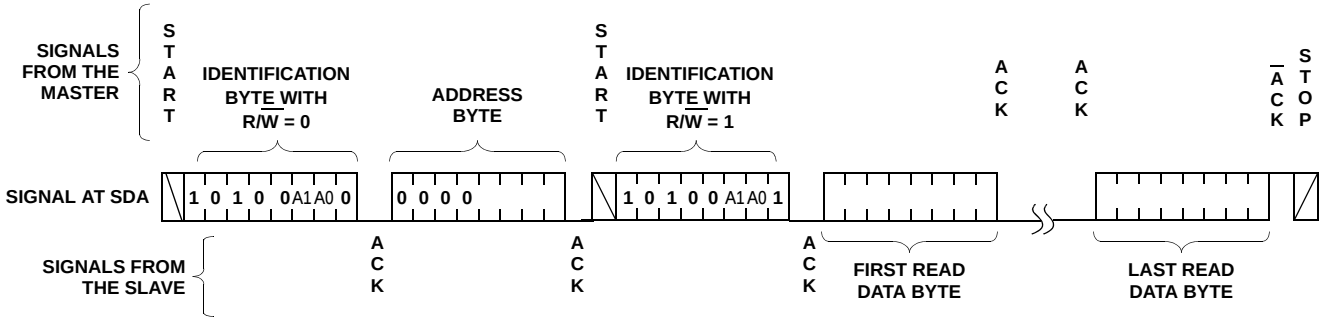


FIGURE 19. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22323 responds with an ACK. At this time, the device enters its standby state (See Figure 18).

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22323 responds with an ACK. Then the ISL22323 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The Data Bytes are from the registers indicated by an internal pointer. This pointers initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 0Fh, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.The master terminates the read operation issuing a NACK ($\overline{ACK}$) and a STOP condition following the last bit of the last Data Byte (See Figure 19).

Applications Information

Wiper transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients (or overshoot/undershoot) resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break within an extremely short period of time (<50ns). Two such code transitions are EFh to F0h, and 0Fh to 10h. Note that all switching transients will settle well within the settling time as stated on the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus this may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

Application example

Figure 20 shows an example of using ISL22323 for gain setting and offset correction in high side current measurement application. DCP0 applies a programmable offset voltage of ±25mV to the FB+ pin of the Instrumentation Amplifier EL8173 to adjust output offset to zero voltages. DCP1 programs the gain of the EL8173 from 90 to 110 with 5V output for 10A current through current sense resistor.

More application examples can be found at http://www.intersil.com/data/an/AN1145.pdf

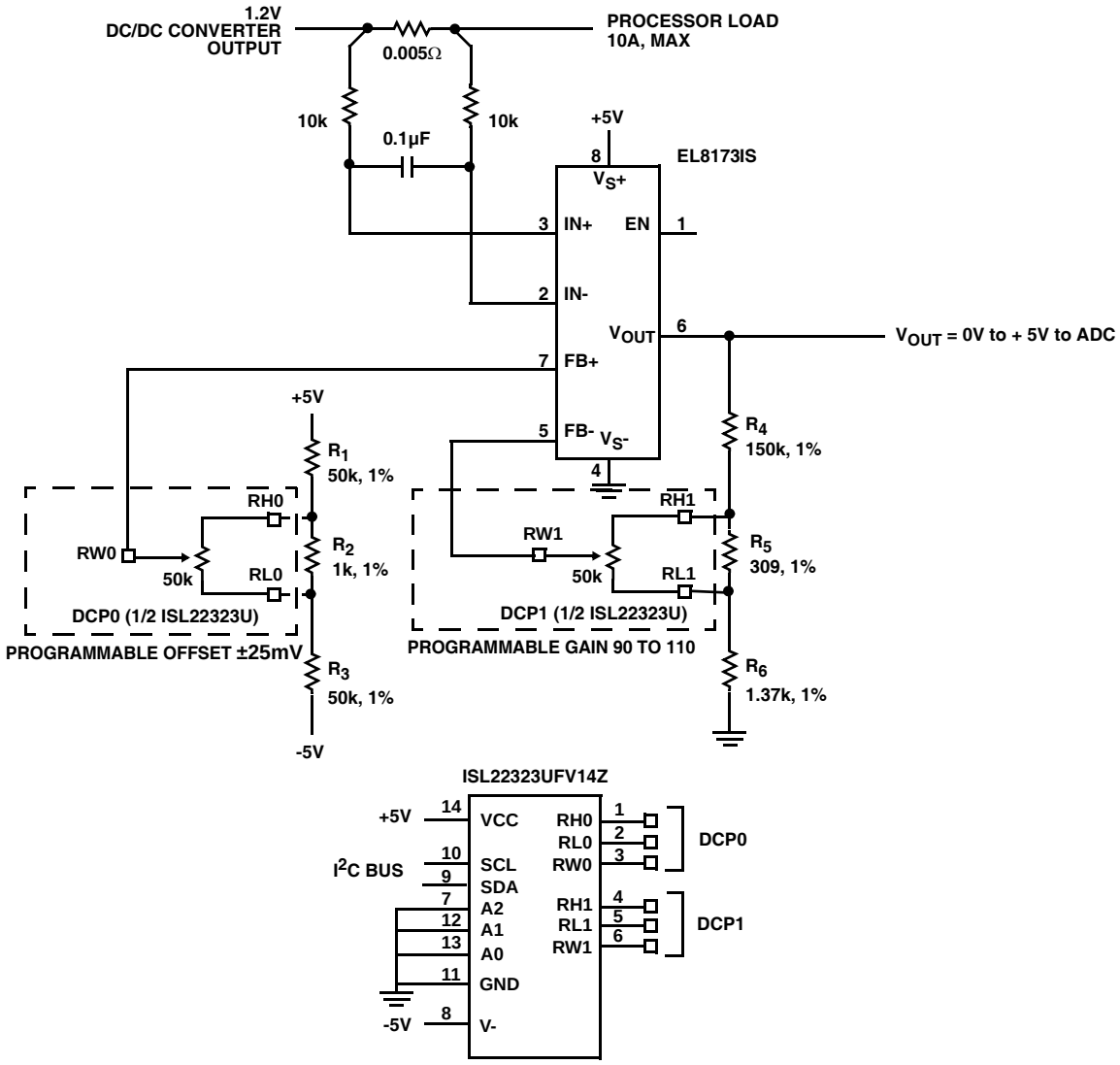
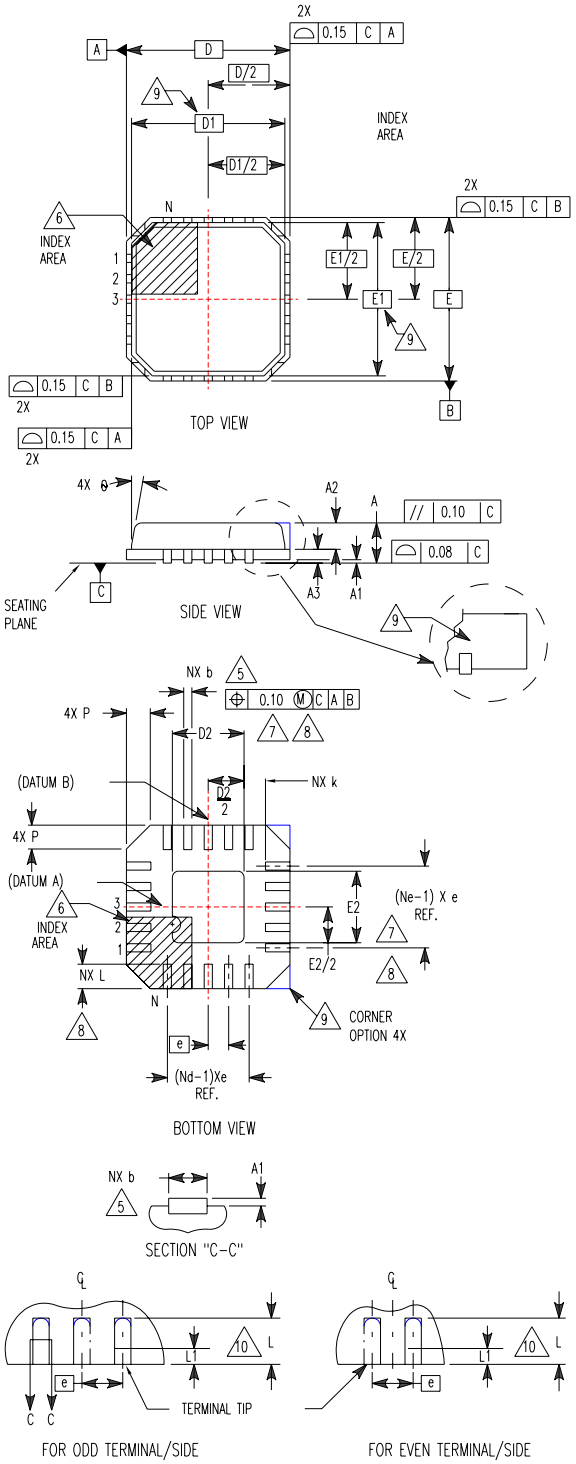


FIGURE 20. CURRENT SENSING WITH GAIN AND OFFSET CONTROL

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGD-10)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.30	2.40	2.55	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.30	2.40	2.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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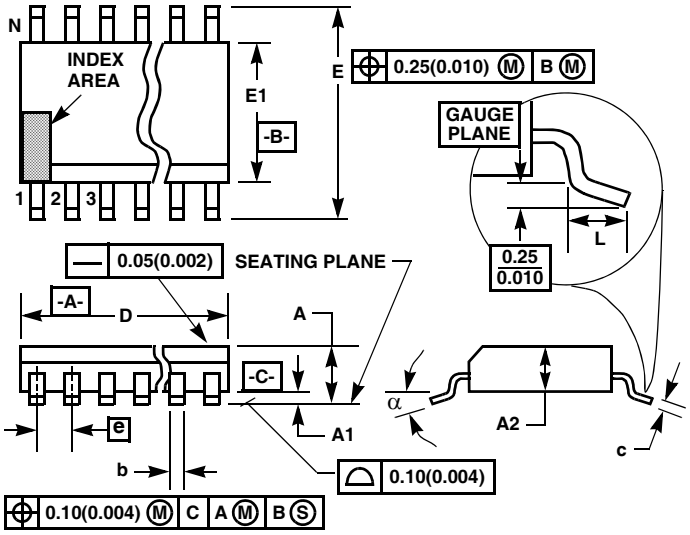
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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