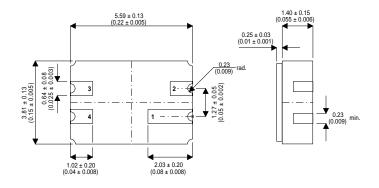




### **MECHANICAL DATA**

Dimensions in mm (inches)



# **ENHANCEMENT MODE MOSFET**

P-CHANNEL

### **FEATURES**

- B<sub>VDSS</sub> =-60V
- $I_D = -2.5A$
- $R_{DS(ON)} = 0.3\Omega$
- Hermetic Surface Mount Package
- Screening Option Available

## LCC3 PACKAGE (MO-041BA) **Underside View**

PAD 3 - Source PAD 1 - Drain **PAD 2 - N/C** PAD 4 - Gate

The SML2955CSM4 is a very low on state resistance P-Channel enhancement mode mosfet in a Ceramic Surface Mount package designed for high rel applications:

## **ABSOLUTE MAXIMUM RATINGS** (T<sub>A</sub> = 25°C unless otherwise stated)

	• • • • • • • • • • • • • • • • • • • •				
$\overline{V_{DS}}$	Drain – Source Voltage		-60V		
$V_{GS}$	Gate – Source Voltage	±20V			
$I_D$	Continuous Drain Current	@T <sub>A</sub> = 25°C	-2.5A		
$I_{DM}$	Pulsed Drain Current <sup>1</sup>		-15A		
$P_{D}$	Power Dissipation	$@T_A = 25^{\circ}C$	0.8W		
		$@T_A = 100^{\circ}C$	0.32W		
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		156°C/W		
$T_{STG}$ , $T_{J}$	Maximum Junction and Storage Temperature Range		-55 to +150°C		

NOTE:

1) Repetitive Rating: Pulse Width limited by maximum junction temperature.

Semelab PIc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

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## **SML2955CSM4**

## **ELECTRICAL RATINGS** (T<sub>A</sub> = 25°C unless otherwise stated)

	Characteristic	Test Co	Test Conditions		Тур.	Max.	Unit
	STATIC CHARACTERISTICS						
V <sub>(BR)DSS</sub>	Drain – Source Breakdown Voltage	$V_{GS} = 0V$	$I_D = -250 \mu A$	-60			V
V <sub>GS(TH)</sub>	Gate Threshold Voltage <sup>1</sup>	$V_{DS} = V_{GS}$	I <sub>D</sub> = -250μA	-2.0	-2.6	-4.0	
I <sub>GSS</sub>	Gate – Source Leakage Current	$V_{GS} = \pm 20V$	$V_{GS} = 0V$			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -60V$	$V_{GS} = 0V$			-10	μΑ
I <sub>D(ON)</sub>	On State Drain Current <sup>1</sup>	V <sub>DS</sub> = -5.0V	V <sub>GS</sub> = -10V	-12			Α
R <sub>DS(ON)</sub>	Drain Source On-State Resistance <sup>1</sup>	I <sub>D</sub> = -2.0A	$V_{GS} = -4.5V$			0.55	Ω
		$I_D = -2.5A$	$V_{GS} = -10V$			0.35	
			$T_J = 125^{\circ}C$			0.55	
9 <sub>fs</sub>	Forward Transconductance 1	V <sub>GS</sub> = -10V	I <sub>D</sub> = -2.5A		5.5		S
V <sub>SD</sub>	Diode Forward Voltage <sup>1</sup>	V <sub>GS</sub> = 0V	I <sub>D</sub> = -2.5A		-0.8	-1.2	V
	DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input capacitance	V 20V	f = 1.0MHz		601		pF
C <sub>oss</sub>	Output capacitance	$V_{DS} = -30V$			85		
C <sub>rss</sub>	Reverse transfer capacitance	$V_{GS} = 0V$			35		
	SWITCHING CHARACTERISTICS						
$Q_g$	Total Gate Charge	V 20V	I <sub>D</sub> = -2.5A		11	15	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS} = -30V$			2.4		
$Q_{gd}$	Gate-Drain Charge	$V_{GS} = -10V$			2.7		
t <sub>d(on)</sub>	Turn-on Delay Time	1.00	$V_{DD} = -30V$ $R_{GEN} = 6\Omega$		12	21	ns
t <sub>r</sub>	Rise Time	⊢ I <sub>D</sub> =-1.0A			10	20	
t <sub>d(off)</sub>	Turn-off Delay Time	V <sub>GS</sub> = -10V			19	34	
t <sub>f</sub>	Fall Time	1			6	12	

#### NOTES:

1) Pulse Test: Pulse Width =  $300\mu s$  , Duty Cycle  $\leq 2\%$ 

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