Ultra Low Noise, Precision Voltage Reference

ISL21090

The ISL21090 is a ultra low noise, high DC accuracy precision voltage reference with wide input voltage range from 4.7V to 36V. The ISL21090 uses the new Intersil Advanced Bipolar technology to achieve sub 2μV_{P-P} 0.1Hz noise with an initial voltage accuracy of 0.02%.

The ISL21090 offers a 2.5V output voltage option with 7ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld SOIC package.

The ISL21090 is ideal for high-end instrumentation, data acquisition and processing applications requiring high DC precision where low noise performance is critical.

Features

- Reference Output Voltage Option
  - 2.5V (Released)
  - 1.25V, 3.3V, 4.096V, 5V, 7V and 10V (Coming Soon)
- Initial Accuracy . . . . . .±0.02%
- Output Voltage Noise . . . . . 1.9μV_{P-P} Typ (0.1Hz to 10Hz) (2.5V Option)
- Supply Current . . . . . 930µA (Typ)
- Tempco . . . . . 7ppm/°C Max (3ppm/°C Coming Soon)
- Output Current Capability 20mA
- Line Regulation 8ppm/V
- Load Regulation 2.5ppm/mA
- Operating Temperature Range . . . . . -40°C to +125°C

Applications

- High-End Instrumentation
- Precision Voltage Sources for Data Acquisition System, Industrial Control, Communication Infrastructure
- Process Control and Instrumentations

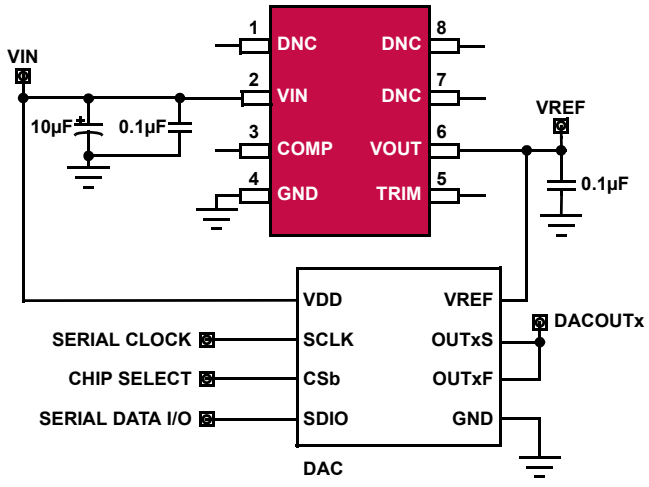


FIGURE 1. ISL21090 TYPICAL APPLICATION DIAGRAM

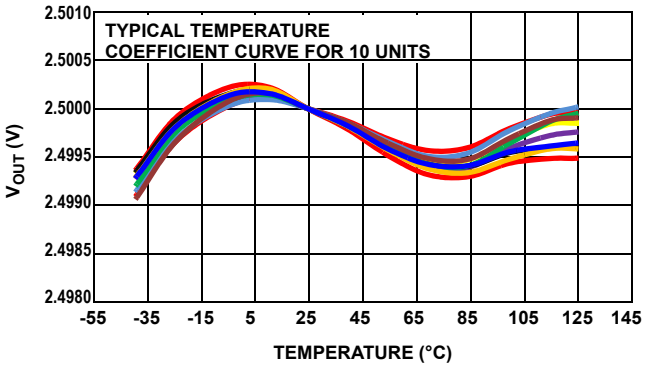
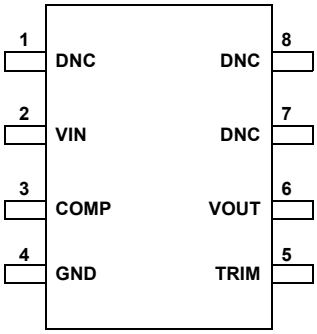


FIGURE 2. V_{OUT} vs TEMPERATURE

Pin Configuration

ISL21090
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	DNC	Do Not Connect
2	VIN	Input Voltage Connection
3	COMP	Compensation and Noise Reduction Capacitor
4	GND	Ground Connection
5	TRIM	Voltage Reference Trim input
6	VOUT	Voltage Reference Output
7	DNC	Do Not Connect
8	DNC	Do Not Connect

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} OPTION (V)	GRADE (%)	TEMPCO (ppm/°C)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-Free)	PKG. DWG. #
ISL21090BFB825Z-TK	21090 BFZ25	2.5	0.02	7	-40 to +125	8 Ld SOIC	M8.15E

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL21090. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

Max Voltage
- V_{IN} to GND ..... -0.5V to +40V
- V_{OUT} to GND (10s) ..... -0.5V to V_{OUT} + 0.5V

Voltage on any Pin to Ground ..... -0.5V to +V_{OUT} + 0.5V
Voltage on DNC pins ..... No connections permitted to these pins
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
- Human Body Model 3kV
- Machine Model 200V
- Charged Device Model 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5)	115	58

Continuous Power Dissipation (T_A = +125°C) 217mW
Maximum Junction Temperature (T_{JMAX}) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile (Note 6) ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Industrial) ..... -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. Post-reflow drift for the ISL21090 devices can exceed 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.

Electrical Specifications

V_{IN} = 5V (2.5V option), I_{OUT} = 0, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{OUT}	Output Voltage	V_{IN} = 5V		2.5		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C	All V_{OUT} options	**-0.02**		**+0.02**	%
TC V_{OUT}	Output Voltage Temperature Coefficient	ISL21090 B grade			**7**	ppm/°C
V_{IN}	Input Voltage Range (Note 9)	V_{OUT} = 2.5V	**4.7**		**36**	V
I_{IN}	Supply Current			0.930	**1.28**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 4.7V to 36V, V_{OUT} = 2.5V		8	**18**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		2.5	**17**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		2.5	**17**	ppm/mA
V_D	Dropout Voltage (Note 8)	V_{OUT} = 2.5V @ 10mA		1.1	**1.7**	V
I_{SC+}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		55		mA
I_{SC-}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-61		mA
t_R	Turn-on Settling Time	90% of final value, C_L = 1.0µF, C_C = open		150		µs
	Ripple Rejection	f = 120Hz		90		dB
e_N	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 2.5V		1.9		μV_{P-P}
V_N	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz, V_{OUT} = 2.5V		1.6		μV_{RMS}
	Noise Density	f = 1kHz, V_{OUT} = 2.5V		50		nV/√Hz
$\Delta V_{OUT}/\Delta t$	Long Term Stability	T_A = +25°C		20		ppm

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. V_{IN}-V_{OUT} measured at the point where V_{OUT} drops 1mV from the nominal measured value.
9. Coming soon: V_{IN} (MIN) = 3.7V

Typical Performance Curves (ISL21090-2.5)

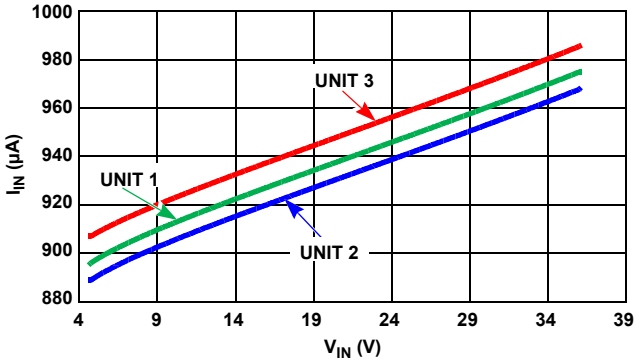


FIGURE 3. I_{IN} vs V_{IN}, THREE UNITS

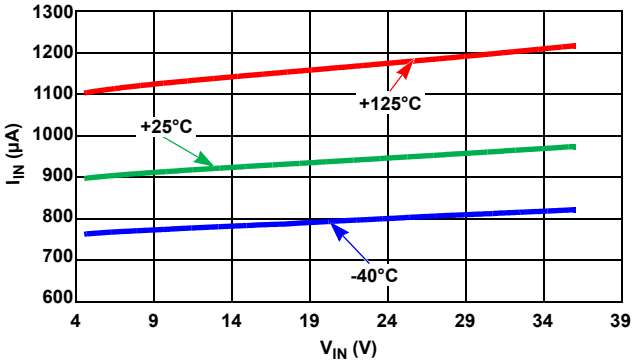


FIGURE 4. I_{IN} vs V_{IN}, THREE TEMPERATURES

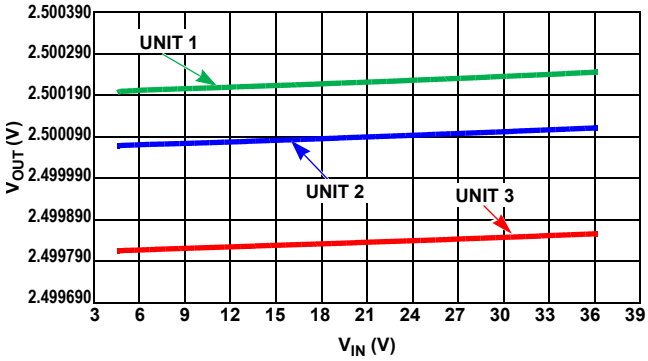


FIGURE 5. LINE REGULATION, THREE UNITS

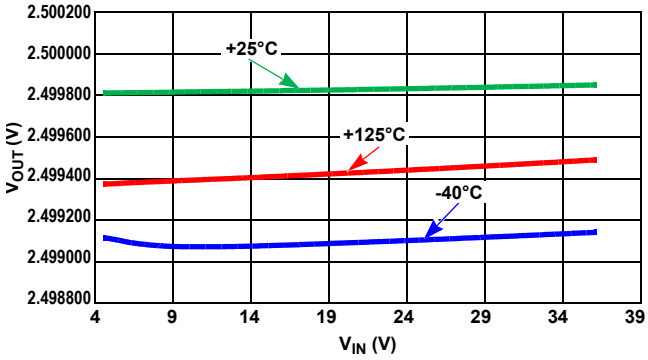


FIGURE 6. LINE REGULATION, THREE TEMPERATURES

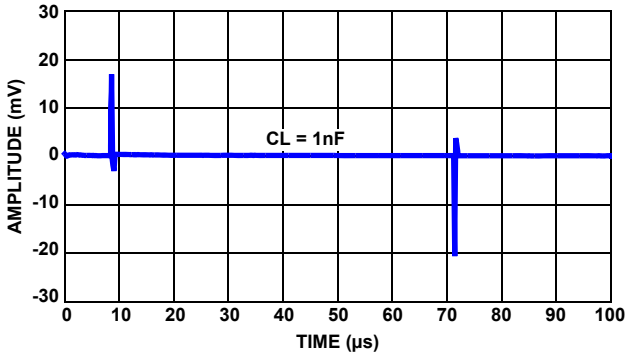


FIGURE 7. LINE TRANSIENT WITH 1nF LOAD (ΔV_{IN} = ±500mV)

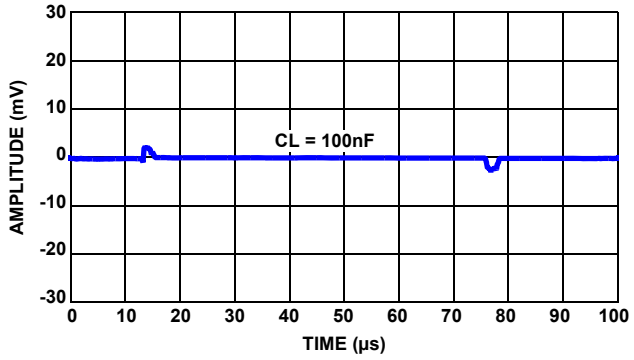


FIGURE 8. LINE TRANSIENT WITH 100nF LOAD (ΔV_{IN} = ±500mV)

Typical Performance Curves (ISL21090-2.5) (Continued)

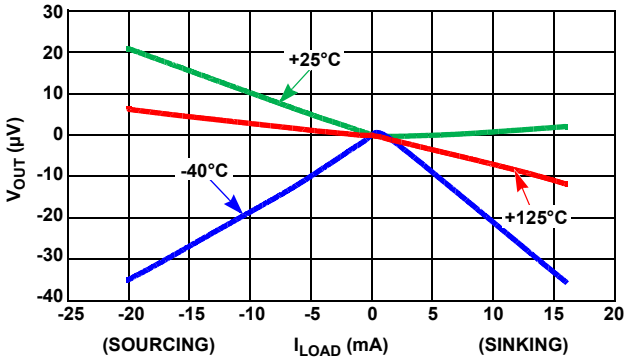


FIGURE 9. LOAD REGULATION, THREE TEMPERATURES

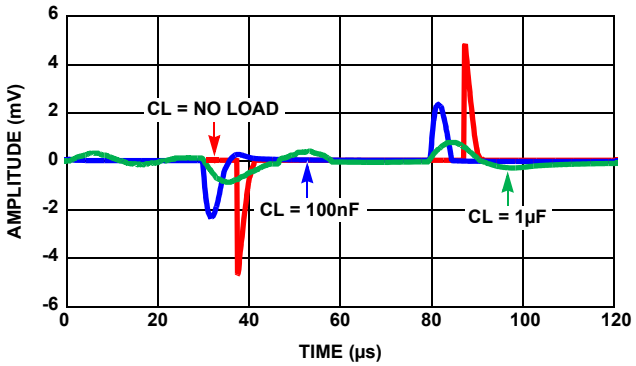


FIGURE 10. LOAD TRANSIENT (ΔV_{IN} = ±1mA)

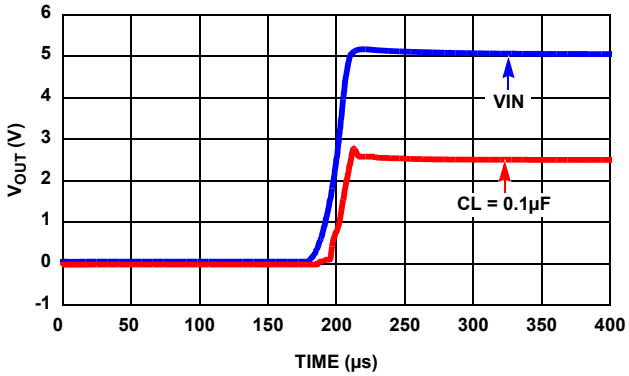


FIGURE 11. TURN-ON TIME WITH 0.1µF

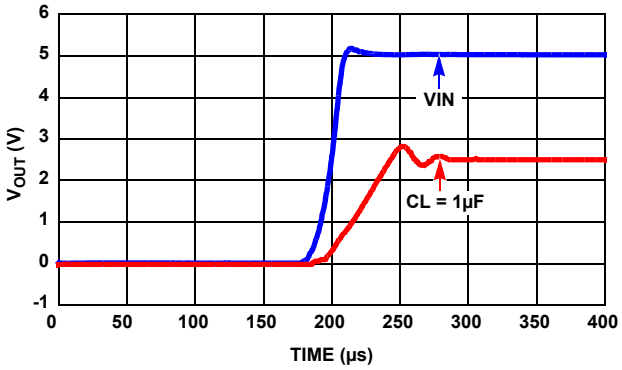


FIGURE 12. TURN-ON TIME WITH 1µF

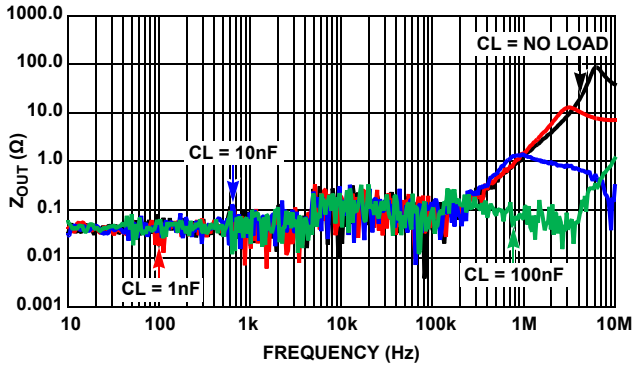


FIGURE 13. Z_{OUT} vs FREQUENCY

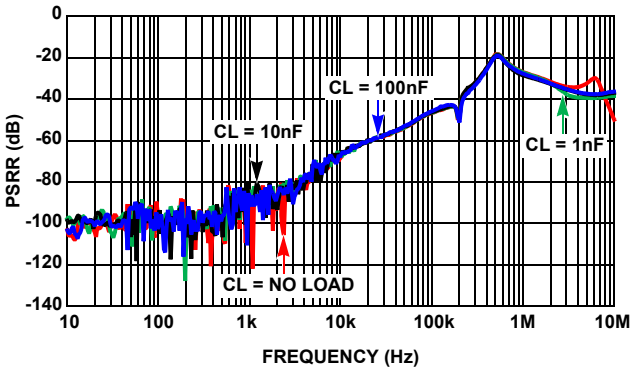


FIGURE 14. RIPPLE REJECTION AT DIFFERENT CAPACITIVE LOADS

Typical Performance Curves (ISL21090-2.5) (Continued)

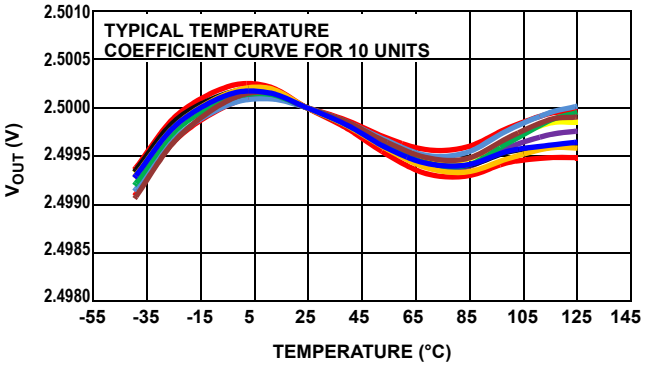


FIGURE 15. V_{OUT} vs TEMPERATURE, 10 UNITS

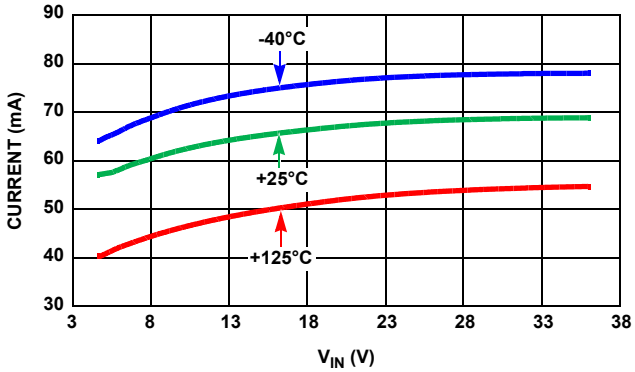


FIGURE 16. SHORT-CIRCUIT TO V_{IN}

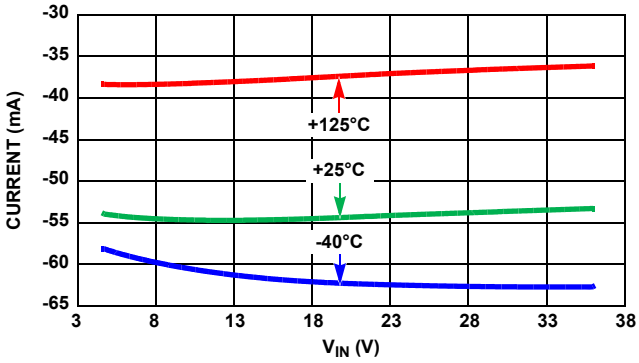


FIGURE 17. SHORT-CIRCUIT TO GND

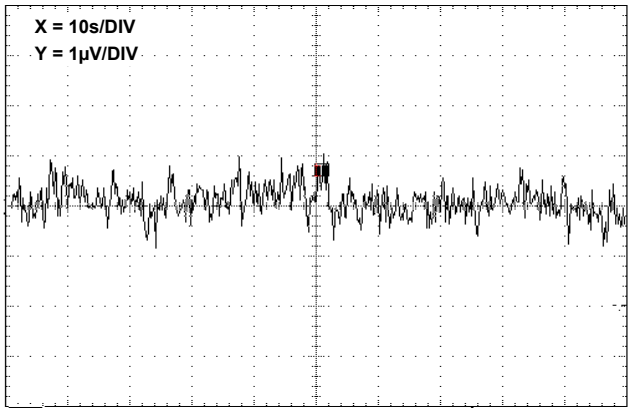


FIGURE 18. V_{OUT} vs NOISE, 0.1Hz to 10Hz

Device Operation

Bandgap Precision References

The ISL21090 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

Applications Information

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a plastic SOIC package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of 100µV to 500µV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $1.9\mu V_{P-P}$ (V_{OUT} = 2.5V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately $1.6\mu V_{RMS}$ (V_{OUT} = 2.5V), with 0.1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added but will result in only marginal improvements in output noise and transient response.

Turn-On Time

Normal turn-on time is typically 150µs, as shown in Figure 12. The circuit designer must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} - V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} - T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The positive input of the amplifier is about 1.216V, and in feedback, so will be the trim voltage. The trim terminal has a 5000Ω resistor to ground internally, and in the case of the 2.5V output version, there is a feedback resistor of approximately 5000Ω from V_{OUT} to trim.

The suggested method to adjust the output is to connect a very high value external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a much lower total resistance and whose outer terminals connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. It is important to minimize the capacitance on the trim terminal to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 8, 2011	FN6993.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL21090

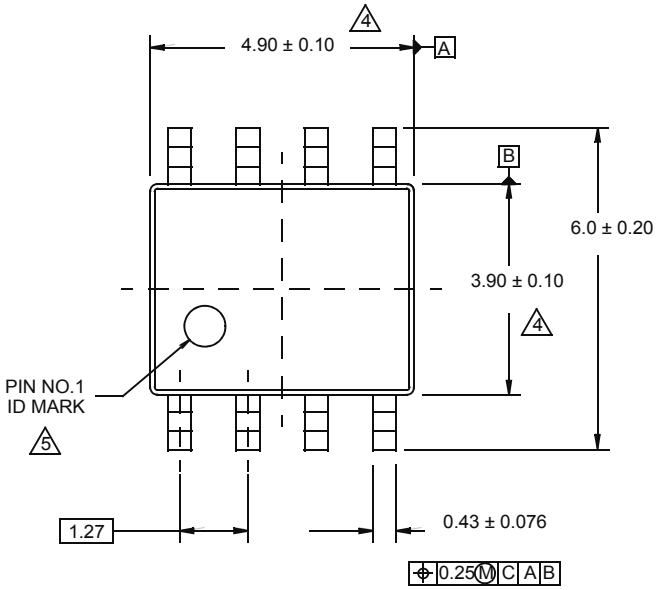
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

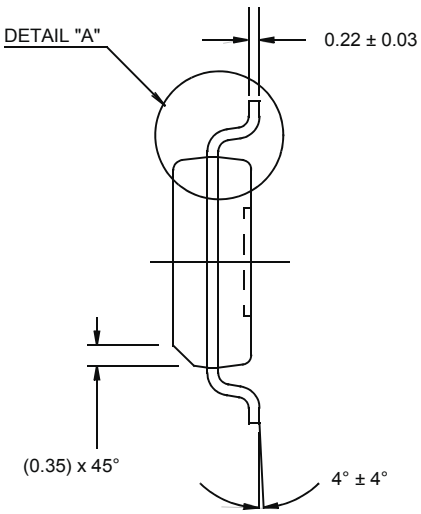
Package Outline Drawing

M8.15E

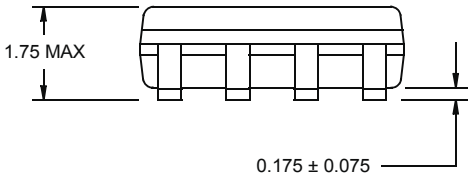
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



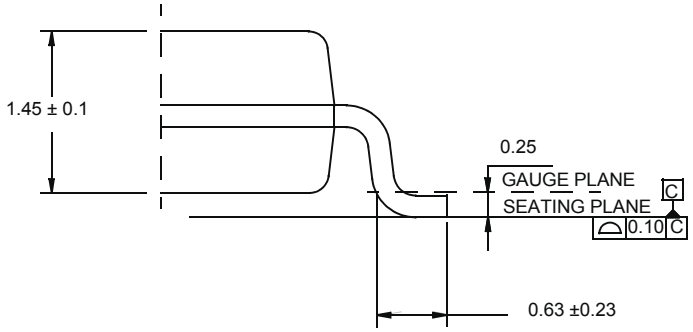
TOP VIEW



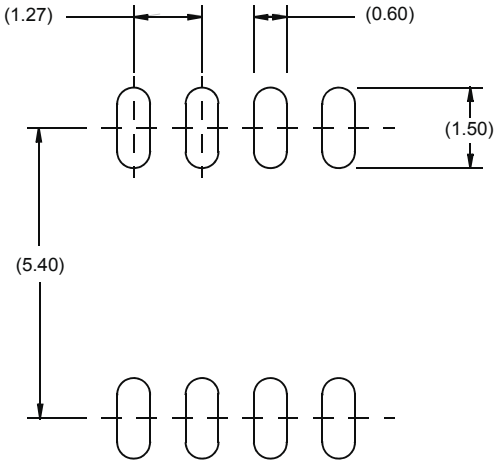
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.