Dual, 500MHz Triple, Multiplexing Amplifiers

The ISL59483 contains a gain of 1 triple 4:1 MUX amplifier (MUX1), and a second gain of 2 triple 4:1 MUX amplifier (MUX2). Each feature high slew rate and excellent bandwidth for RGB video switching. They contain separate binary coded, channel select logic inputs (S0, S1), and separate logic inputs for High Impedance output (HIZ) and power-down ($\overline{EN}$) modes. The HIZ state presents a high impedance at the output so that both RGB MUX outputs can be wired together to form an 8:1 RGB MUX amplifier or they can be used in R-R, G-G, and B-B pairs to form a 4:1 differential input/output MUX. Separate power-down mode controls ($\overline{EN1}$, $\overline{EN2}$) are included to turn off unneeded circuitry in power sensitive applications. With both $\overline{EN}$ pins pulled high, the ISL59483 enters a standby power mode, consuming just 36mW.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
ISL59483IRZ	ISL59483 IRZ	-	48 Ld Exposed Pad 7x7 QFN	L48.7x7B
ISL59483IRZ-T13	ISL59483 IRZ	13”	48 Ld Exposed Pad 7x7 QFN	L48.7x7B

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

TABLE 1. CHANNEL SELECT LOGIC TABLE ISL59483

S1-1, 2	S0-1, 2	$\overline{EN1}$, $\overline{EN2}$	HIZ1, 2	OUTPUT1, 2
0	0	0	0	IN0 (A, B, C)
0	1	0	0	IN1 (A, B, C)
1	0	0	0	IN2 (A, B, C)
1	1	0	0	IN3 (A, B, C)
X	X	1	X	Power-down
X	X	0	1	High Z

Features

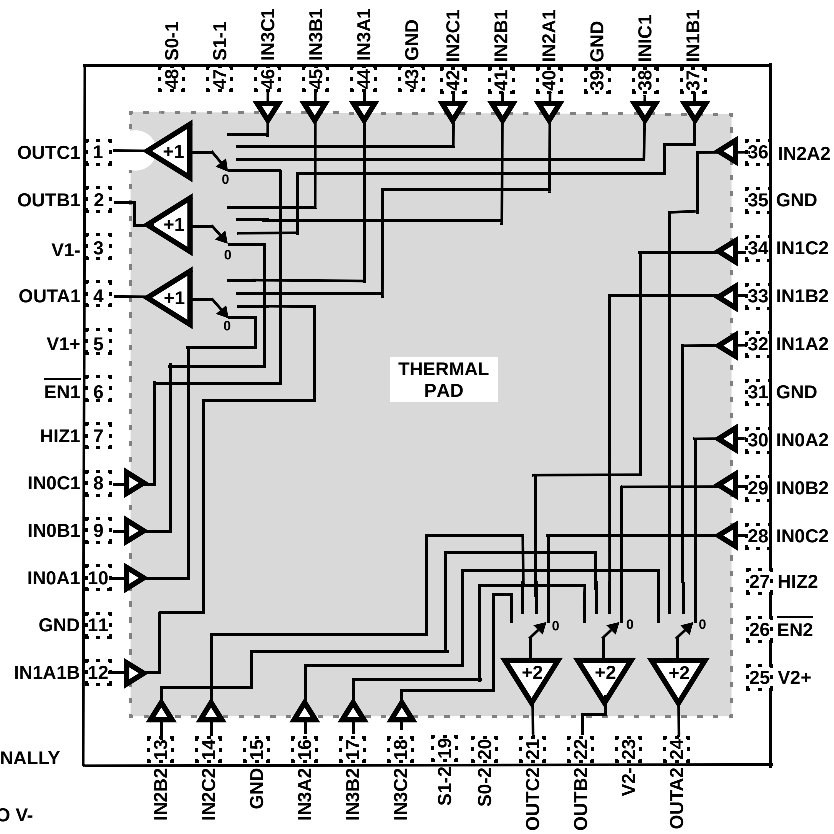
- Separate gain of 1 and gain of 2, triple 4:1 multiplexers for RGB
- Externally configurable for various video MUX circuits including
  - 8:1 RGB MUX with selectable gains of 1 or 2
  - Two separate 4:1 RGB MUX with gains of 1 and 2
- High impedance outputs (HIZ)
- Power-down mode ($\overline{EN}$)
- ±5V operation
- ±870V/µs slew rate (G = 1), ±1600V/µs slew rate (G = 2)
- 500MHz bandwidth
- Supply current 16mA/CH
- Pb-free plus anneal (RoHS compliant)

Applications

- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set-top boxes
- Security video
- Broadcast video equipment

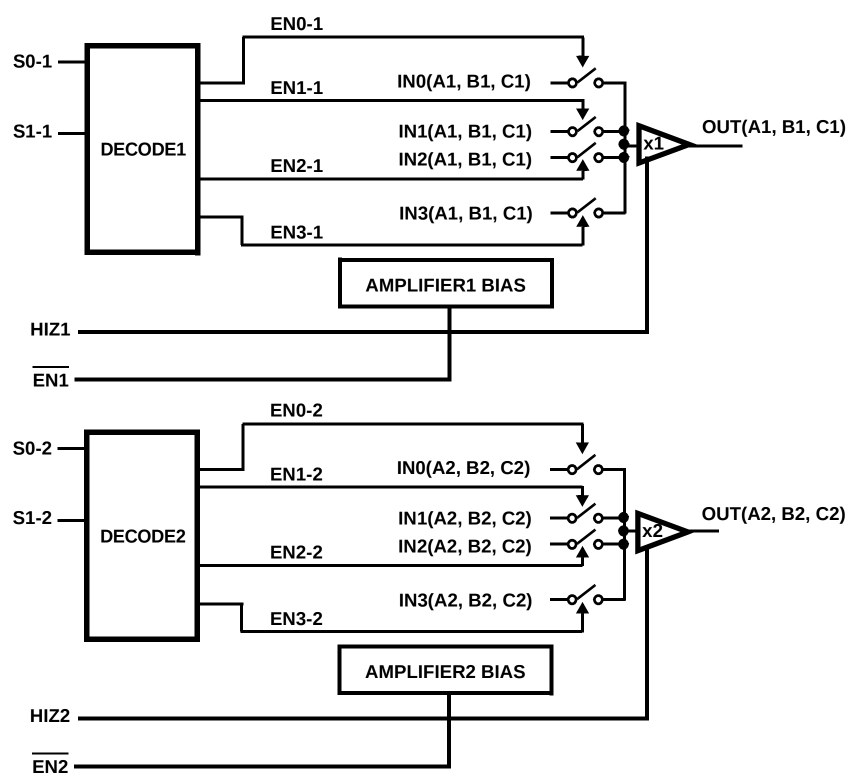
Pinout

ISL59483
(48 LD QFN)
TOP VIEW



THERMAL PAD INTERNALLY
CONNECTED TO V-
PAD MUST BE TIED TO V-

Functional Diagram ISL59483



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to V-) 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
  Human Body Model (Per MIL-STD-883 Method 3015.7) 2500V
  Machine Model 300V

Thermal Information

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V1+ = V2+ = +5V, V1- = V2- = -5V, GND = 0V, T_A = +25° C, Input Video = $1V_{P-P}$ and R_L = 500Ω to GND, C_L = 5pF unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
$+I_S$ Enabled	Enabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ Low	75	92	100	mA
$-I_S$ Enabled	Enabled Supply Curren	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ Low	-96	-87	-68	mA
$+I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ High	4	6.5	8	µA
$-I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{EN1}$, $\overline{EN2}$ High	-200	-10		µA
V_{OUT}	MUX1: Positive and Negative Output Swing	V_{IN} = ±3.5V, R_L = 500Ω	3.1	3.4		|V|
	MUX2: Positive and Negative Output Swing	V_{IN} = ±2.5V; R_L = 500Ω	3.8	4.0	4.2	|V|
I_{OUT}	Output Current	R_L = 10Ω to GND	80	125		|mA|
V_{OS}	MUX1: Output Offset Voltage	V_{IN} = 0V	-10	2	14	mV
	MUX2: Output Offset Voltage	V_{IN} = 0V	-60	-25	20	mV
Ib	Input Bias Current	V_{IN} = 0V	-10	-2	+10	µA
R_{OUT}	MUX1: HIZ Output Resistance	HIZ = Logic High		1.2		MΩ
	MUX2: HIZ Output Resistance	HIZ = Logic High	700	1000	1300	Ω
R_{OUT}	Enabled Output Resistance	HIZ = Logic Low		0.1		Ω
R_{IN}	Input Resistance	V_{IN} = ±3.5V		10		MΩ
A_{CL} or A_V	MUX1: Voltage Gain	V_{IN} = ±1.5V, R_L= 500Ω	0.98	0.99	1.02	V/V
	MUX2: Voltage Gain	V_{IN} = ±1.5V, R_L= 500Ω	1.94	1.99	2.04	V/V
I_{HIZ}	MUX1: Output Current in High Impedance State	V_{OUT} = 0V		-9		µA
LOGIC						
V_{IH}	Input High Voltage (Logic Inputs)		2			V
V_{IL}	Input Low Voltage (Logic Inputs)				0.8	V
I_{IH}	Input High Current (Logic Inputs)	V_H = 5V	200	270	320	µA
I_{IL}	Input Low Current (Logic Inputs)	V_L = 0V	-10	-1	+10	µA

Electrical Specifications V1+ = V2+ = +5V, V1- = V2- = -5V, GND = 0V, T_A = +25° C, Input Video = $1V_{P-P}$ and R_L = 500Ω to GND, C_L = 5pF unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC GENERAL						
PSRR	MUX1: Power Supply Rejection Ratio	DC, PSRR V+ and V- combined	52	56		dB
	MUX2: Power Supply Rejection Ratio	DC, PSRR V+ and V- combined	45	53		dB
ISO	Channel Isolation	f = 10MHz, Ch-Ch X-Talk and Off Isolation, C_L = 1.5pF		75		dB
dG	MUX1: Differential Gain Error	NTC-7, RL = 150, C_L = 1.5pF		0.02		%
	MUX2: Differential Gain Error	NTC-7, R_L = 150, C_L = 1.2pF		0.008		%
dP	MUX1: Differential Phase Error	NTC-7, RL = 150, C_L = 1.5pF		0.02		°
	MUX2: Differential Phase Error	NTC-7, R_L = 150, C_L = 1.2pF		0.01		°
BW	Small Signal -3dB Bandwidth	V_{OUT} = $0.2V_{P-P}$; C_L = 1.5pF R_L =500Ω		500		MHz
FBW	MUX1: 0.1dB Bandwidth	C_L = 1.5pF R_L = 500Ω		60		MHz
		C_L = 4.7pF R_L = 500Ω		120		MHz
FBW	MUX2: 0.1dB Bandwidth	C_L = 1.1pF R_L = 500Ω		160		MHz
		C_L = 1.1pF R_L = 150Ω		50		MHz
SR	MUX1: Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L = 1.5pF		±870		V/µs
	MUX2: Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L = 1.5pF		±1600		V/µs
SWITCHING CHARACTERISTICS						
V_{GLITCH} MUX1:	Channel-to-Channel Switching Glitch	V_{IN} = 0V C_L = 1.2pF		40		mV_{P-P}
	$\overline{EN}$ Switching Glitch	V_{IN} = 0V C_L = 1.2pF		300		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V C_L = 1.2pF		200		mV_{P-P}
V_{GLITCH} MUX2:	Channel-to-Channel Switching Glitch	V_{IN} = 0V, R_L = 150Ω; C_L = 2.1pF		15		mV_{P-P}
	$\overline{EN}$ Switching Glitch	V_{IN} = 0V, R_L = 150Ω; C_L = 2.1pF		1800		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V, R_L = 150Ω; C_L = 2.1pF		340		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		22		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		25		ns
tr, tf	Rise and Fall Time	10% to 90%; V_{IN} = 1V R_L =500Ω C_L = 1.2pF		1.2		ns
		10% to 90%; V_{IN} = 0.1V R_L=500Ω C_L=1.2pF		0.7		ns
ts	0.1% Settling Time	V_{IN} = 1V R_L = 500Ω C_L = 1.2pF		22		ns
tpd	Propagation Delay	10% to 10%		0.73		ns

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, un less otherwise specified.

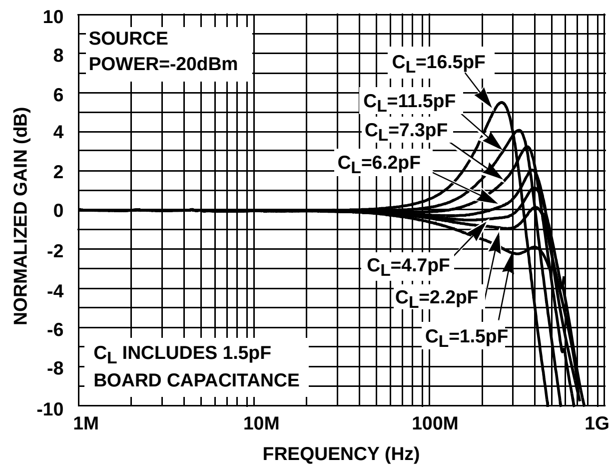


FIGURE 1. MUX1: GAIN vs FREQUENCY vs C_L

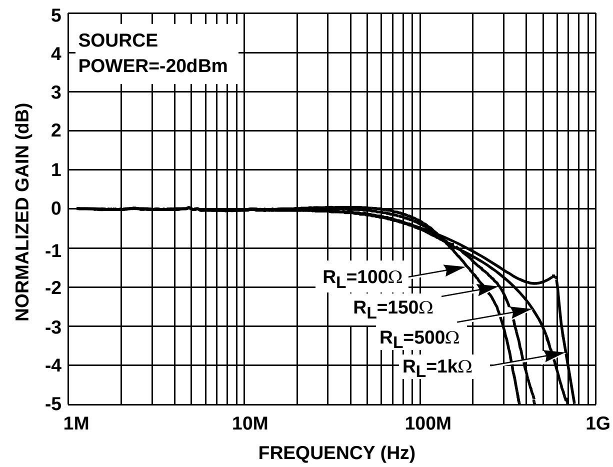


FIGURE 2. MUX1: GAIN vs FREQUENCY vs R_L

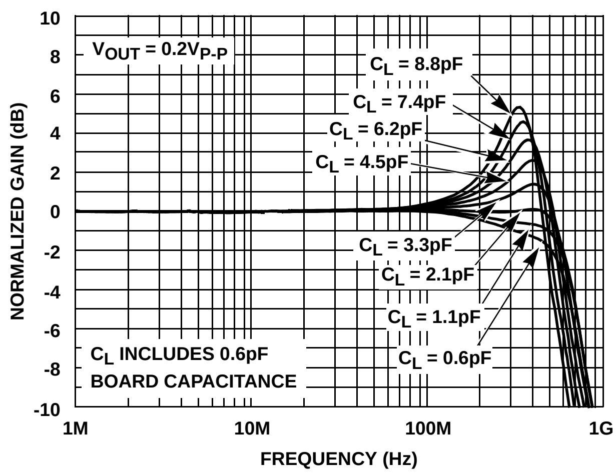


FIGURE 3. MUX2: SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 500Ω LOAD

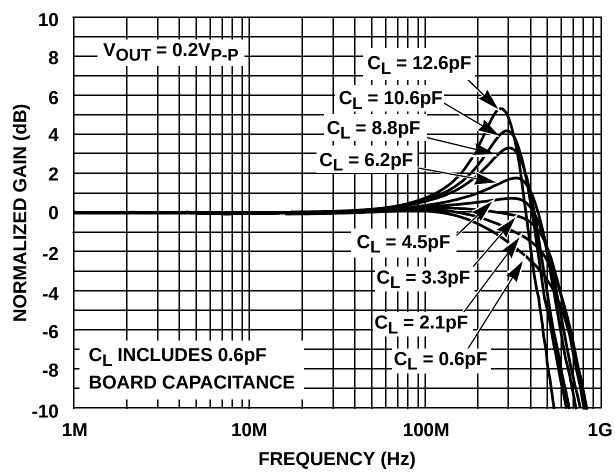


FIGURE 4. MUX2: SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD

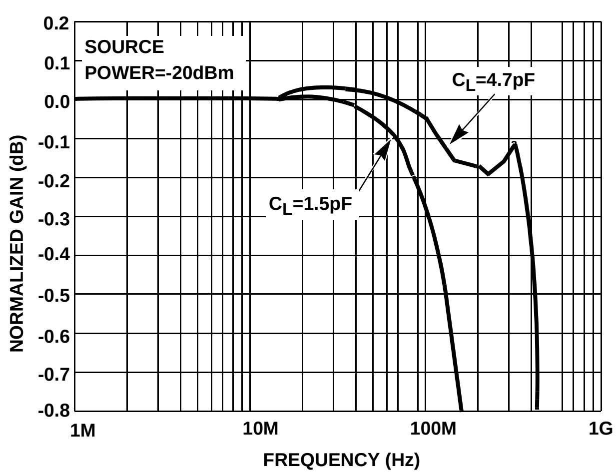


FIGURE 5. MUX1: 0.1dB GAIN vs FREQUENCY

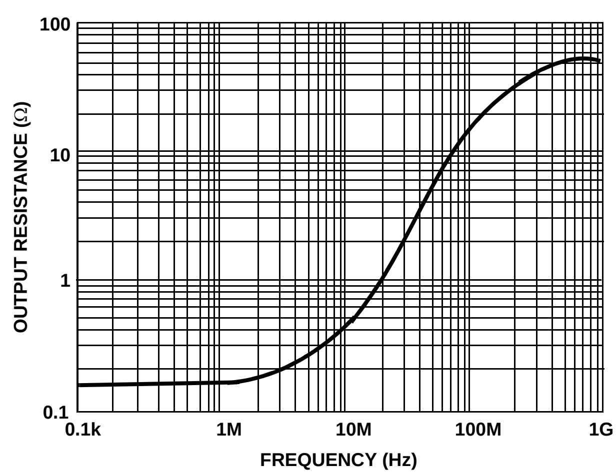


FIGURE 6. MUX1: R_{OUT} vs FREQUENCY

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, un less otherwise specified. **(Continued)**

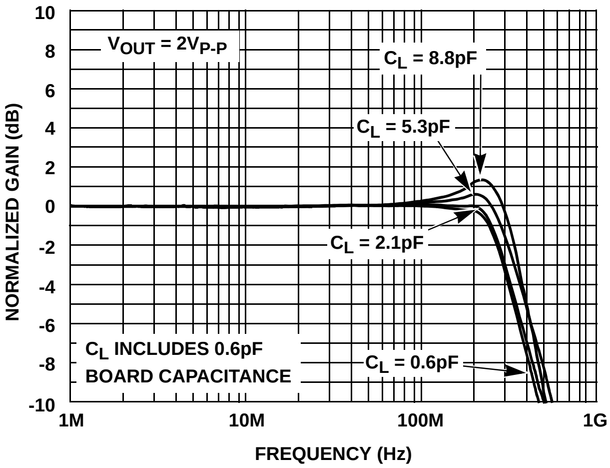


FIGURE 7. MUX2: LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 500Ω LOAD

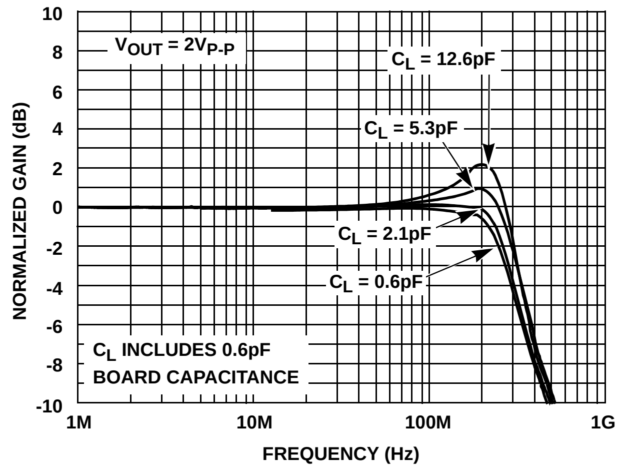


FIGURE 8. MUX2: LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD

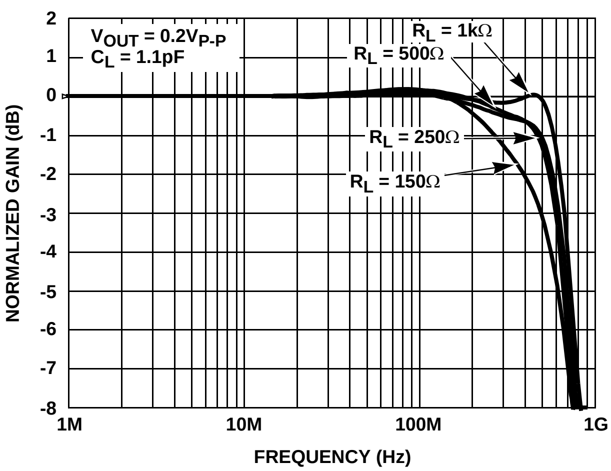


FIGURE 9. MUX2: GAIN vs FREQUENCY vs R_L

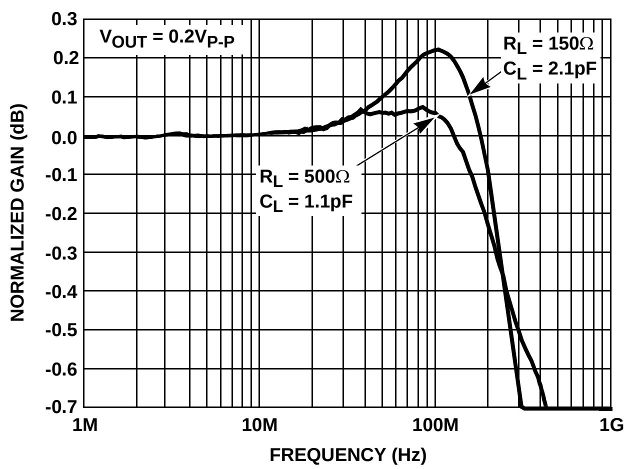


FIGURE 10. MUX2: 0.1dB GAIN FLATNESS

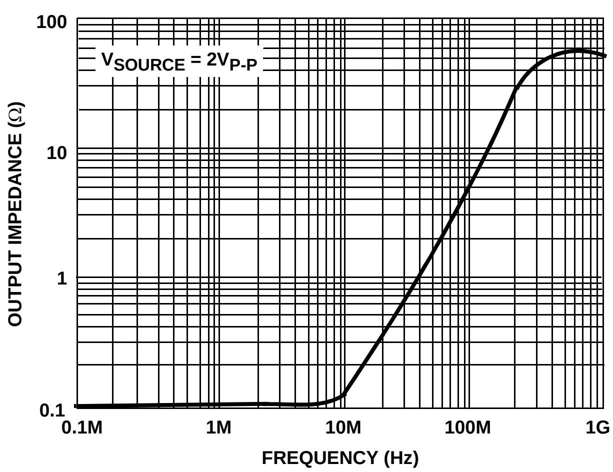


FIGURE 11. MUX2: Z_{OUT} vs FREQUENCY - ENABLED

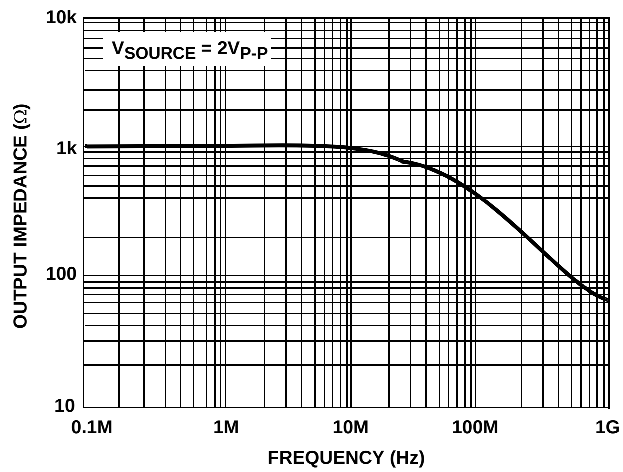


FIGURE 12. MUX2: Z_{OUT} vs FREQUENCY - HIZ

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, un less otherwise specified. **(Continued)**

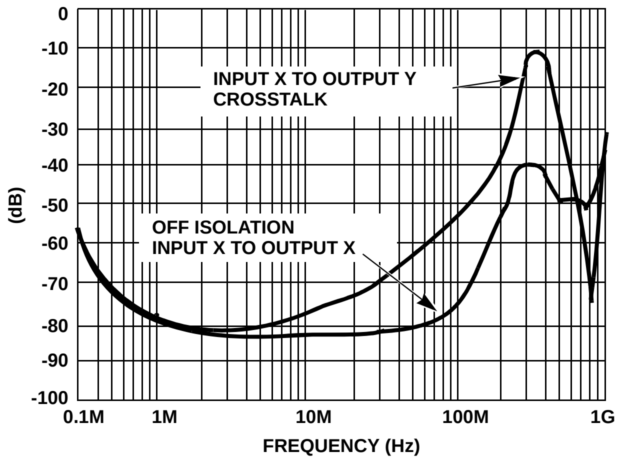


FIGURE 13. MUX1: CROSSTALK AND OFF ISOLATION

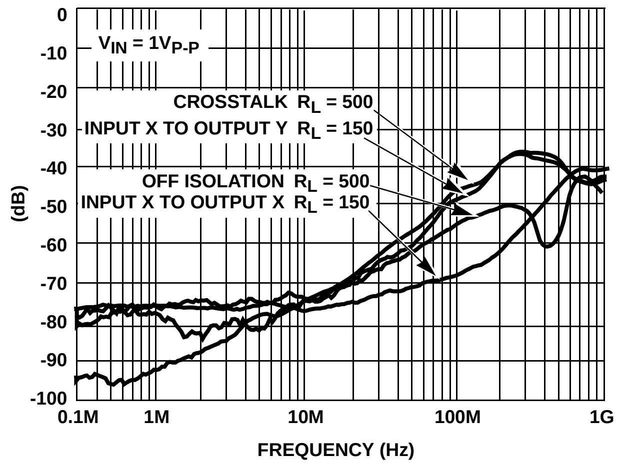


FIGURE 14. MUX 2: CROSSTALK AND OFF ISOLATION

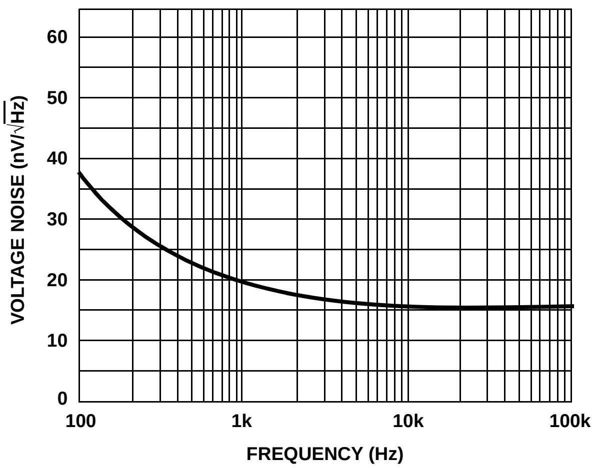


FIGURE 15. MUX1: INPUT NOISE vs FREQUENCY

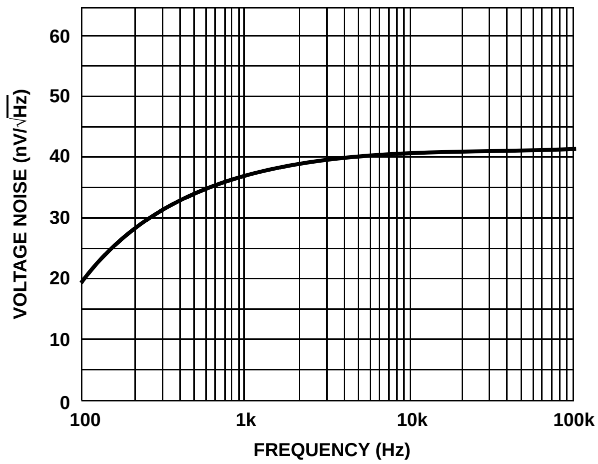


FIGURE 16. MUX2: INPUT NOISE vs FREQUENCY

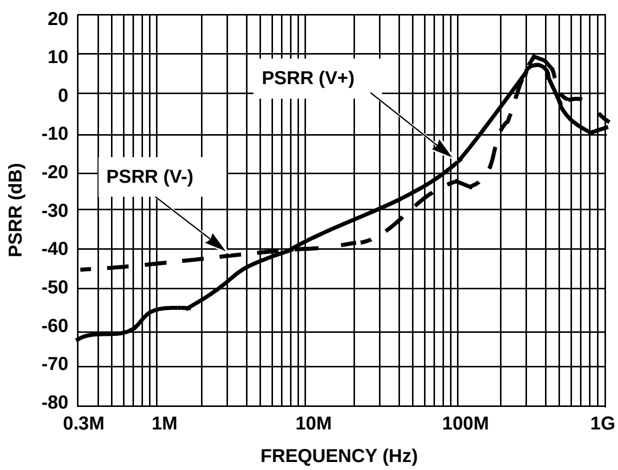


FIGURE 17. MUX 1: PSRR vs FREQUENCY

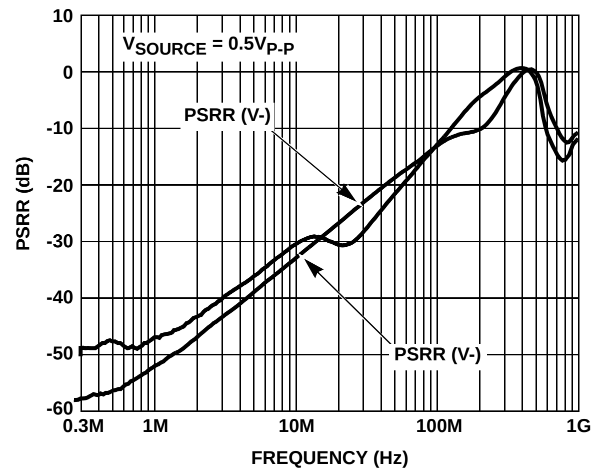


FIGURE 18. MUX 2: PSRR vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, un less otherwise specified. **(Continued)**

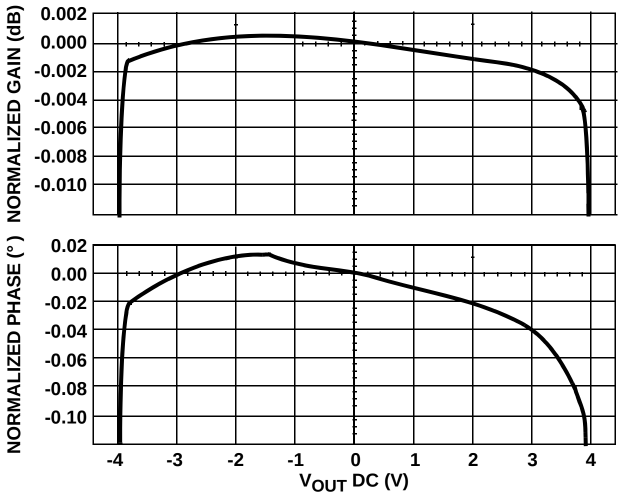


FIGURE 19. MUX 2: DIFFERENTIAL GAIN AND PHASE; $V_{OUT} = 0.2V_{P-P}$, $F_O = 3.58MHz$, $R_L = 500\Omega$

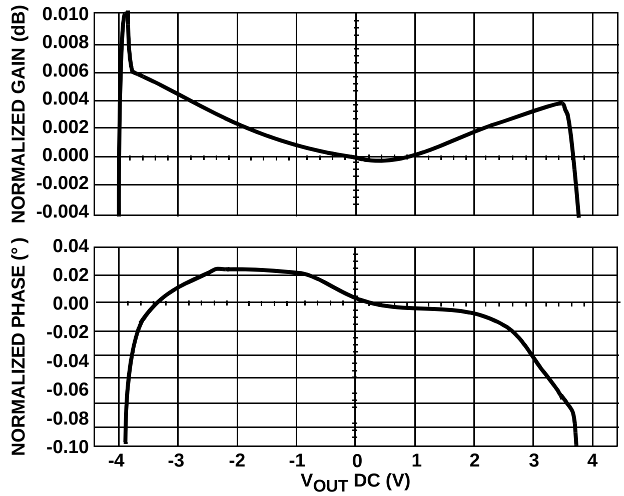


FIGURE 20. MUX 2: DIFFERENTIAL GAIN AND PHASE; $V_{OUT} = 0.2V_{P-P}$, $F_O = 3.58MHz$, $R_L = 150\Omega$

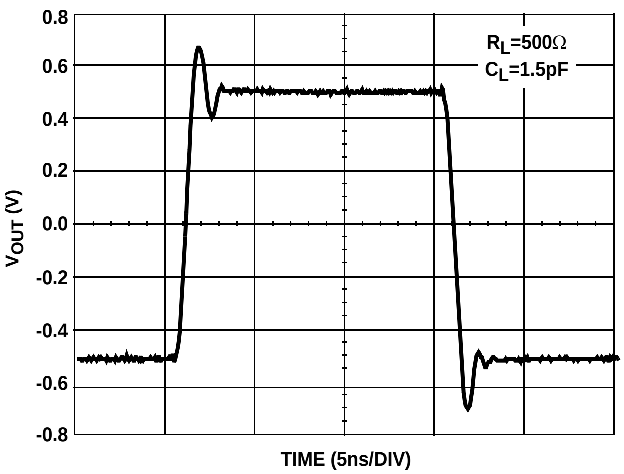


FIGURE 21. MUX 1: SMALL SIGNAL TRANSIENT RESPONSE

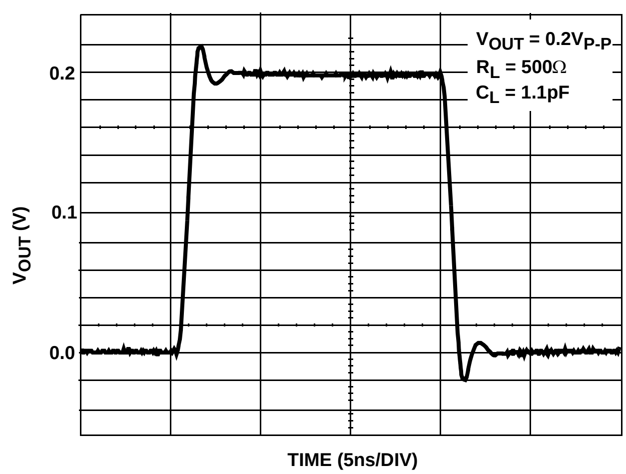


FIGURE 22. MUX 2: SMALL SIGNAL TRANSIENT RESPONSE; $R_L = 500\Omega$

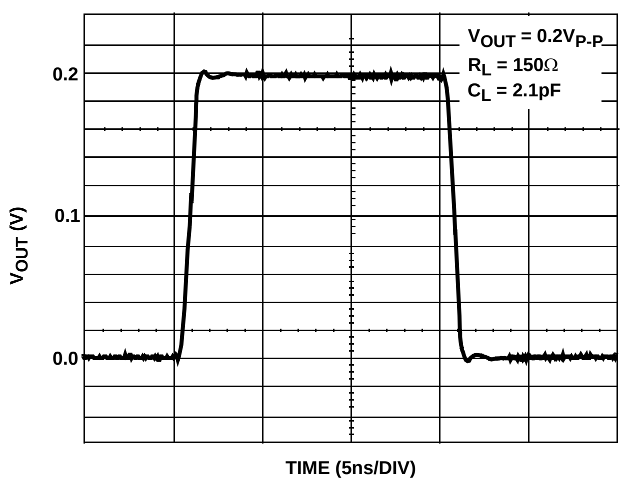


FIGURE 23. MUX 2: SMALL SIGNAL TRANSIENT RESPONSE; $R_L = 150\Omega$

Typical Performance Curves $V_S = \pm 5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, un less otherwise specified. **(Continued)**

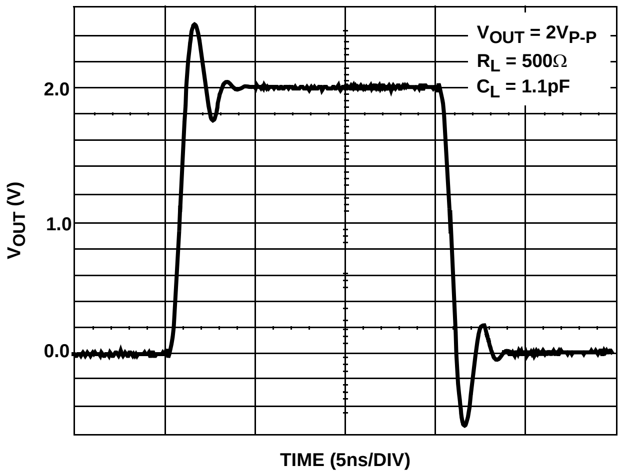


FIGURE 24. MUX2 : LARGE SIGNAL TRANSIENT RESPONSE; $R_L = 500\Omega$

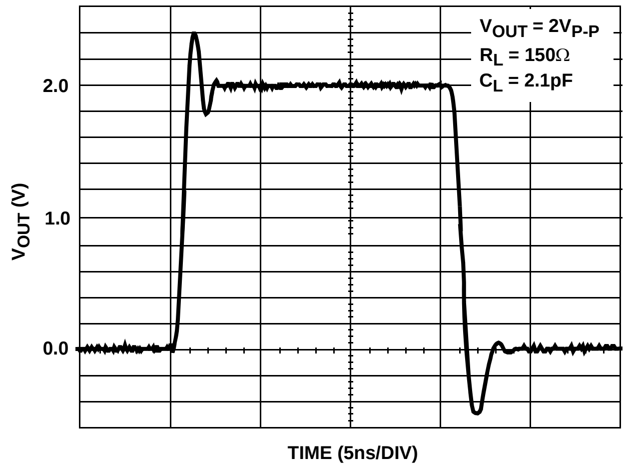


FIGURE 25. MUX 2: LARGE SIGNAL TRANSIENT RESPONSE; $R_L = 150\Omega$

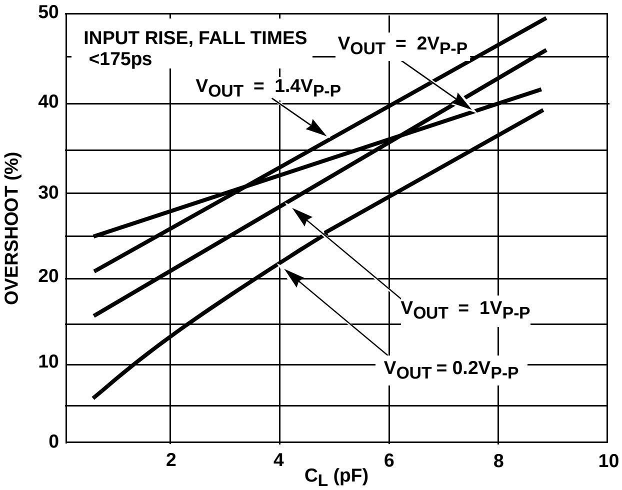


FIGURE 26. MUX 2: PULSE OVERSHOOT vs V_{OUT}, C_L; R_L=500Ω

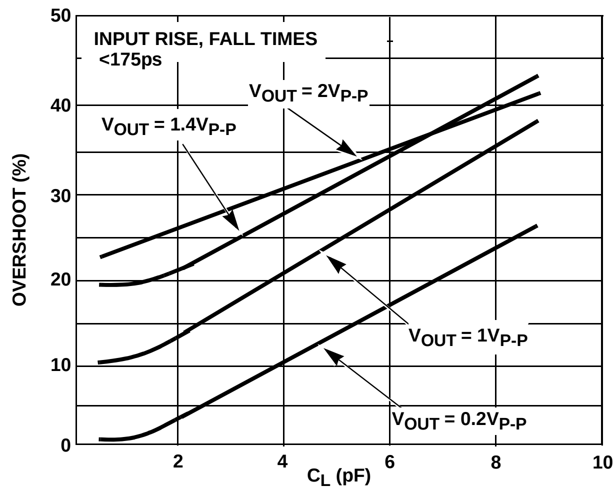


FIGURE 27. MUX 2: PULSE OVERSHOOT vs V_{OUT}, C_L; R_L=150Ω

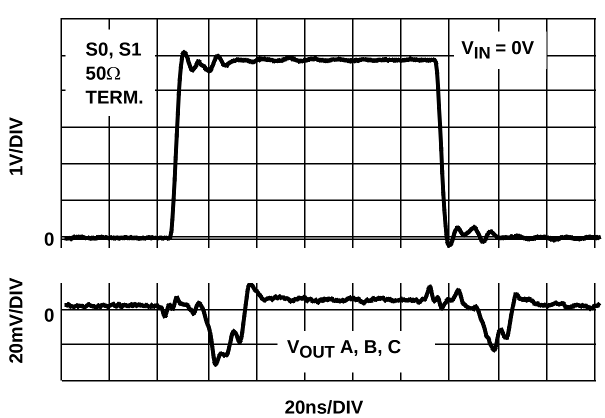


FIGURE 28. MUX 1: CHANNEL TO CHANNEL SWITCHING GLITCH V_{IN} = 0V

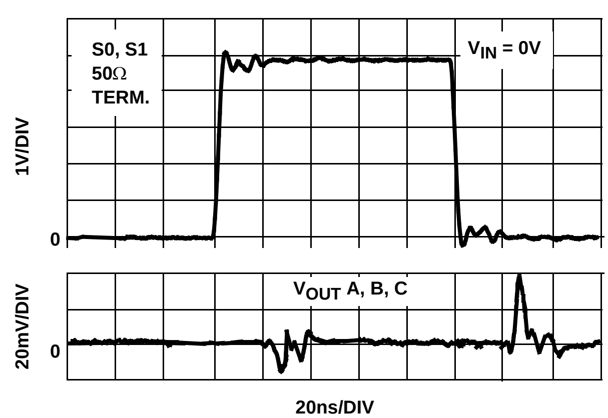


FIGURE 29. MUX 2: CHANNEL TO CHANNEL SWITCHING GLITCH V_{IN} = 0V

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, un less otherwise specified. **(Continued)**

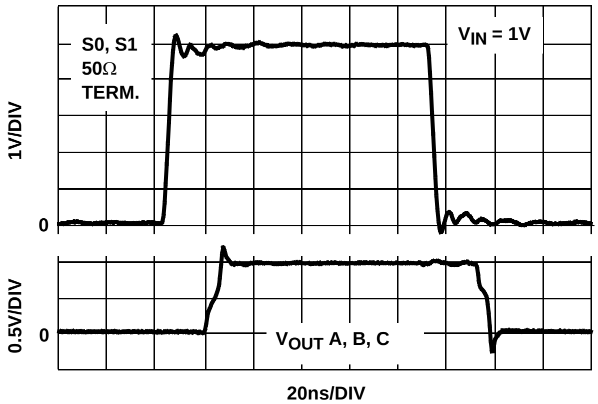


FIGURE 30. MUX 1: CHANNEL TO CHANNEL TRANSIENT RESPONSE V_{IN} = 1V

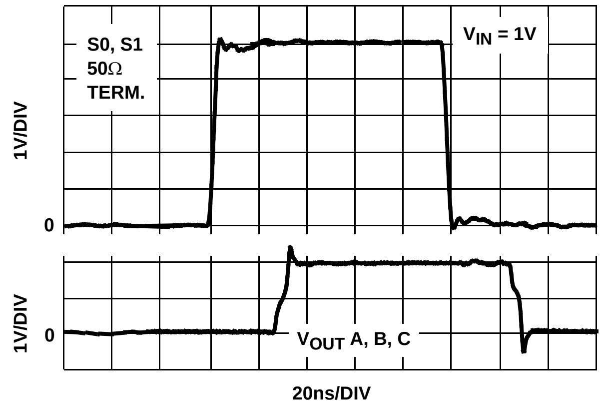


FIGURE 31. MUX 2: CHANNEL TO CHANNEL TRANSIENT RESPONSE V_{IN} = 1V

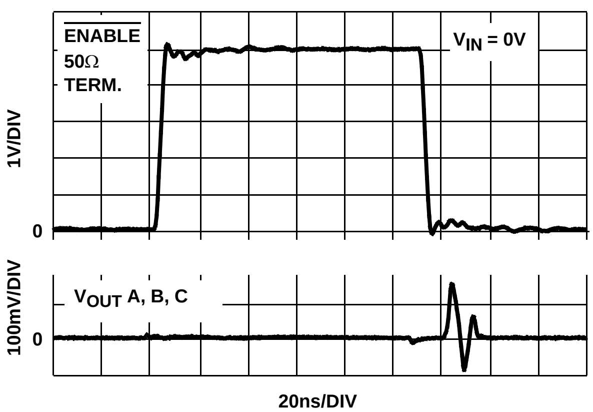


FIGURE 32. $\overline{\text{MUX 1}}$: $\overline{\text{ENABLE}}$ SWITCHING GLITCH V_{IN} = 0V

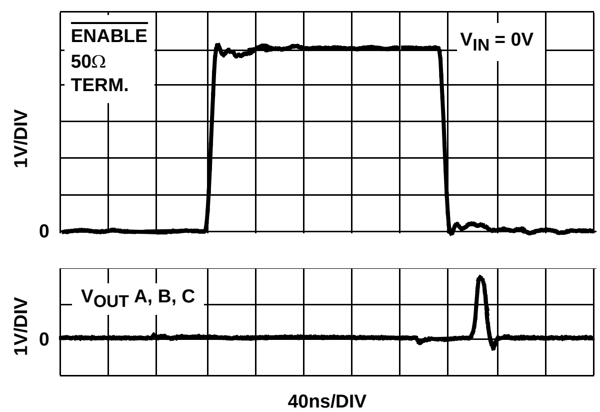


FIGURE 33. $\overline{\text{MUX 2}}$: $\overline{\text{ENABLE}}$ SWITCHING GLITCH V_{IN} = 0V

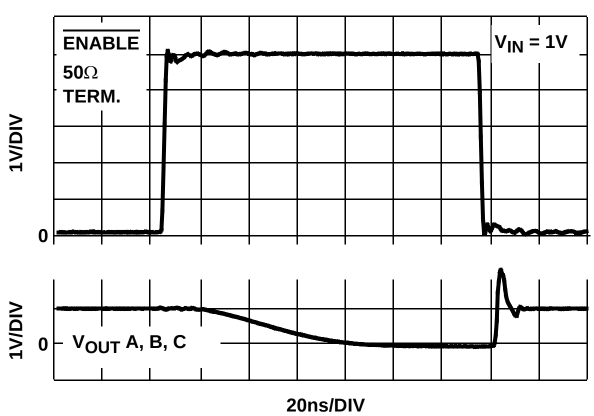


FIGURE 34. $\overline{\text{MUX 1}}$: $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE V_{IN} = 1V

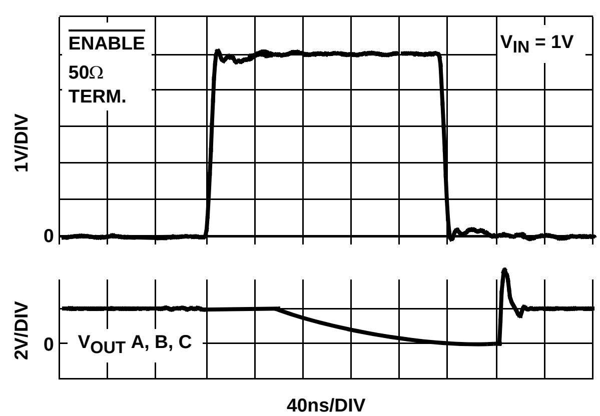


FIGURE 35. $\overline{\text{MUX 2}}$: $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE V_{IN} = 1V

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

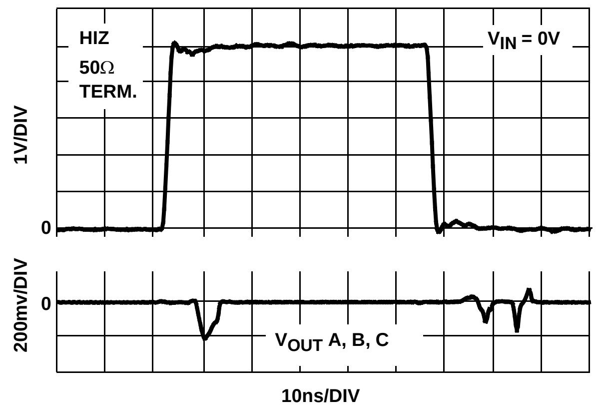


FIGURE 36. MUX 1: HIZ SWITCHING GLITCH V_{IN} = 0V

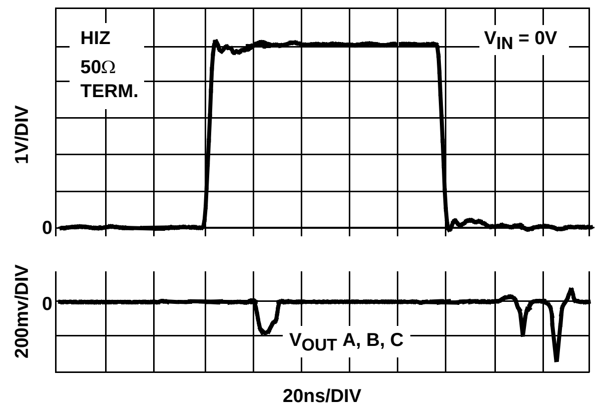


FIGURE 37. MUX 2: HIZ SWITCHING GLITCH V_{IN} = 0V

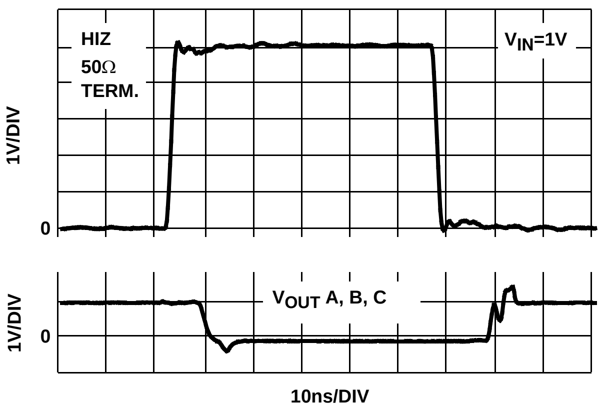


FIGURE 38. MUX 1: HIZ TRANSIENT RESPONSE V_{IN} = 1V

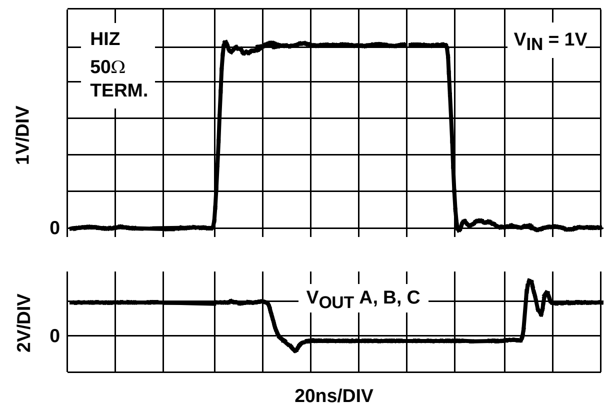


FIGURE 39. MUX 2: HIZ TRANSIENT RESPONSE V_{IN} = 1V

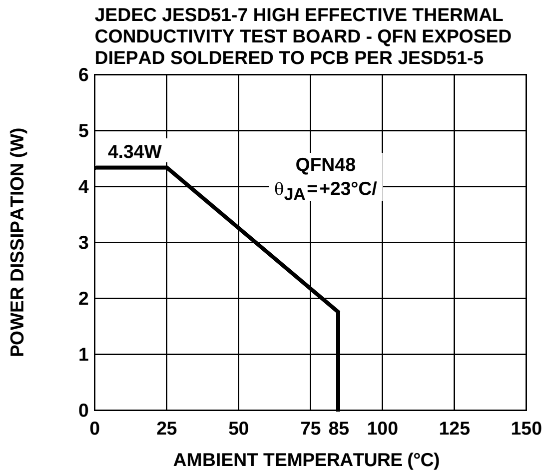


FIGURE 40. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

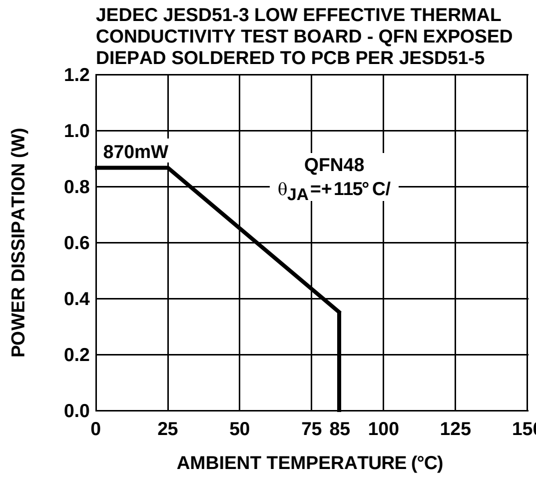
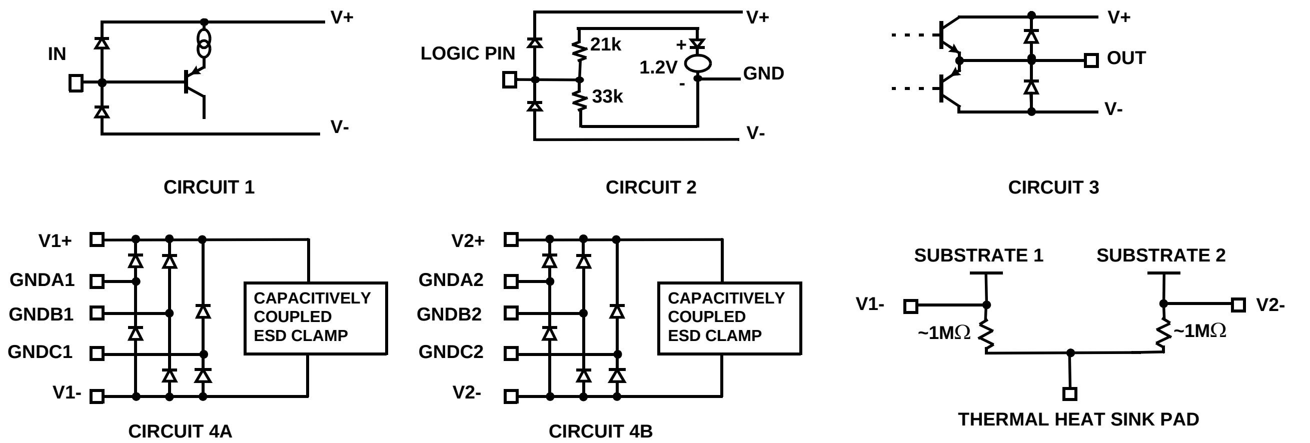


FIGURE 41. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Description

ISL59483 (48 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUTC1	Circuit 3	Output of amplifier C1
2	OUTB1	Circuit 3	Output of amplifier B1
3, 23	V1-, V2-	Circuit 4A	Negative power supply #1 and #2
4	OUTA1	Circuit 3	Output of amplifier A1
5, 25	V1+, V2+	Circuit 4A	Positive Power Supply #1 and #2
6	$\overline{\text{EN1}}$	Circuit 2	Device enable (active low) with internal pull-down resistor. A logic High puts device into power-down mode leaving the logic circuitry active. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
26	$\overline{\text{EN2}}$		
7	HIZ1	Circuit 2	Output disable (active high) with internal pull-down resistor. A logic high puts the output in a high impedance state. Use this state when more than one MUX-amp share the same video output line.
27	HIZ2		
8	IN0C1	Circuit 1	Channel 0 input for amplifier C1
9	IN0B1	Circuit 1	Channel 0 input for amplifier B1
10	IN0A1	Circuit 1	Channel 0 input for amplifier A1
11	GND	Circuit 4A	Ground pin for amplifier A1
12	IN1A1	Circuit 1	Channel 1 input for amplifier A1
13	IN2B2	Circuit 1	Channel 2 input for amplifier B2
14	IN2C2	Circuit 1	Channel 2 input for amplifier C2
15	GND	Circuit 4B	Ground pin for amplifier C2
16	IN3A2	Circuit 1	Channel 3 input for amplifier A2
17	IN3B2	Circuit 1	Channel 3 input for amplifier B2
18	IN3C2	Circuit 1	Channel 3 input for amplifier C2
19, 47	S1-2, S1-1	Circuit 2	Channel select pin MSB (binary logic code) for amplifiers A2, B2, C2 (S1-2) and A1, B1, C1 (S1-1)
20, 48	S0-2, S0-1	Circuit 2	Channel select pin LSB (binary logic code) for amplifiers A2, B2, C2 (S0-2) and A1, B1, C1 (S0-1)
21	OUTC2	Circuit 2	Output of amplifier C2
22	OUTB2	Circuit 1	Output of amplifier B2
24	OUTA2	Circuit 1	Output of amplifier A2
28	IN0C2	Circuit 1	Channel 0 input for amplifier A2
29	IN0B2	Circuit 1	Channel 0 input for amplifier B2
30	IN0A2	Circuit 1	Channel 0 input for amplifier C2
31	GND	Circuit 4B	Ground pin for amplifier A2
32	IN1A2	Circuit 1	Channel 1 input for amplifier A2
33	IN1B2	Circuit 1	Channel 1 input for amplifier B2
34	IN1C2	Circuit 1	Channel 1 input for amplifier C2
35	GND	Circuit 4B	Ground pin for amplifier B2
36	IN2A2	Circuit 1	Channel 2 input for amplifier A2
37	IN1B1	Circuit 1	Channel 1 input for amplifier B1
38	IN1C1	Circuit 1	Channel 1 input for amplifier C1
39	GND	Circuit 4A	Ground pin for amplifier B1
40	IN2A1	Circuit 1	Channel 2 input for amplifier A1
41	IN2B1	Circuit 1	Channel 2 input for amplifier B1
42	IN2C1	Circuit 1	Channel 2 input for amplifier C1
43	GND	Circuit 4A	Ground pin for amplifier C1
44	IN3A1	Circuit 1	Channel 3 input for amplifier A1
45	IN3B1	Circuit 1	Channel 3 input for amplifier B1
46	IN3C1	Circuit 1	Channel 3 input for amplifier C1

Pin Equivalent Circuits



AC Test Circuits

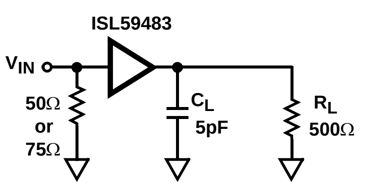


FIGURE 42A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

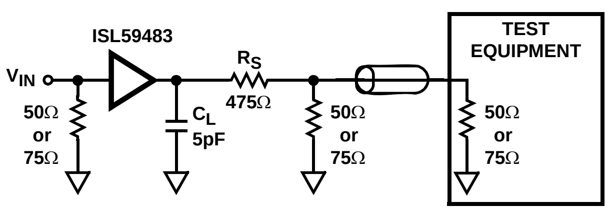


FIGURE 42B. TEST CIRCUIT FOR MEASURING WITH 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

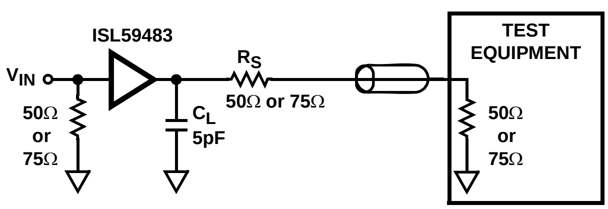


FIGURE 42C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

FIGURE 42. TEST CIRCUITS

Figure 42A illustrates the optimum output load for testing AC performance. Figure 42B illustrates the optimum output load when connecting to 50Ω input terminated equipment.

Application Information

General

The ISL59483 is ideal as the matrix element of high performance switchers and routers. Key features include high impedance buffered analog inputs and excellent AC performance at output loads down to 150Ω for video cable-driving. The current feedback output amplifiers are stable operating into capacitive loads and bandwidth is optimized with a load of 5pF in parallel with a 500Ω. Total output capacitance can be split between the PCB capacitance and an external load capacitor.

Ground Connections

For the best isolation and crosstalk rejection, all GND pins must connect to the GND plane.

Power-up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT-triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 43) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply. One Schottky can be used to protect both V+ power supply pins, and a second for the protection of both V- pins.

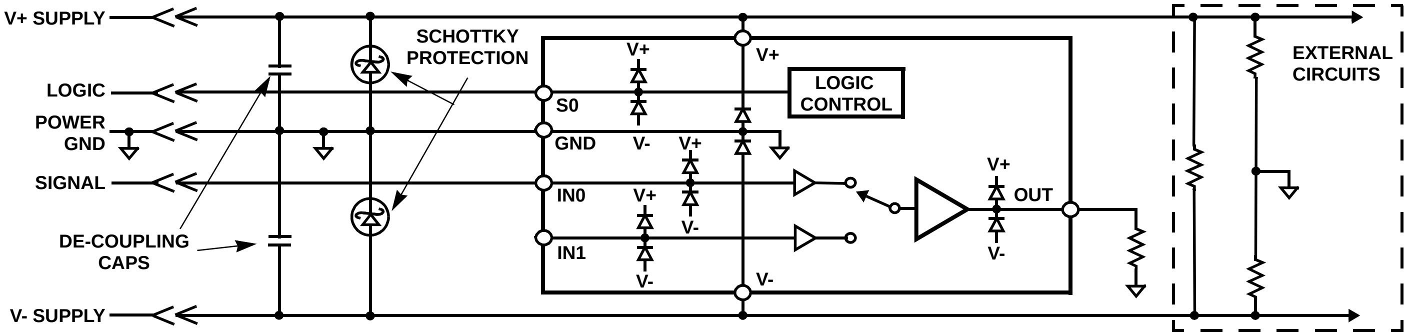


FIGURE 43. SCHOTTKY PROTECTION CIRCUIT

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+ can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

HIZ State

Each internal 4:1 triple MUX-amp has a high impedance output control pin (HIZ1 and HIZ2). Each has an internal pull-down resistor to set the output to the enabled state with no connection to the HIZ pin. The HIZ state is established within approximately 15ns by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the MUX 1 output is a high impedance 1.4MΩ with approximately 1.5pF in parallel with a 10µA bias current from the output. In the HIZ state the MUX 2 output impedance is ~900Ω. The supply current during this state is the same as the active state.

$\overline{\text{EN}}$ and Power-down States

The $\overline{\text{EN}}$ pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{EN}}$ pin. The power-down state is established within approximately 80ns if a logic high (>2V) is placed on the $\overline{\text{EN}}$ pin. In the power-down state, supply current is reduced significantly by shutting the three amplifiers off. The output presents a high impedance to the output pin, however, there is a risk that the disabled amplifier output can be back-driven at signal voltage levels exceeding ~$2V_{P-P}$. Under this condition, large incoming slew rates can cause fault currents of tens of mA**.** Therefore, the parallel connection of multiple outputs is not recommended unless the application can tolerate the limited power-down output impedance.

Output Capacitive Loading Considerations

High speed amplifiers may be sensitive to capacitance at the output. Excessive pulse overshoot may result from the combination of output slew rates approaching the amplifier maximum and the presence of parasitic capacitance. In applications where high slew rates are expected and PC board output pin capacitance exceeds ~5pF, series connected resistors (ranging from 10Ω to 75Ω) may be needed close to the output pin in order to buffer the amplifer output stage from the effects of capacitive loading. When paralleling the amplifier outputs, resistance in series with MUX 1 output will form a resistor divider with the 900Ω HIZ impedance of MUX 2 when MUX 1 is enabled and MUX 2 is in the HIZ state. However, resistance in series with MUX 2 does not result in a resistor divider with MUX 1 due to the 1.4MΩ HIZ impedance. In all cases, series resistance will form a voltage divider with any downstream load resistance, therefore the effects of series resistance on throughput gain must be considered.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners. Use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless controlled impedance (50Ω or 75Ω) strip lines or microstrips are used.
- Match channel to channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.

- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of 2 power supply decoupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible. Avoid vias between the cap and the device because vias adds unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the V1- and V2- supply pins through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Do **not** tie this pin to GND as this could result in large back biased currents flowing between GND and the V- pins. Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible, an isolated thermal pad on another layer should be used. Pad area requirements should be evaluated on a case by case basis.

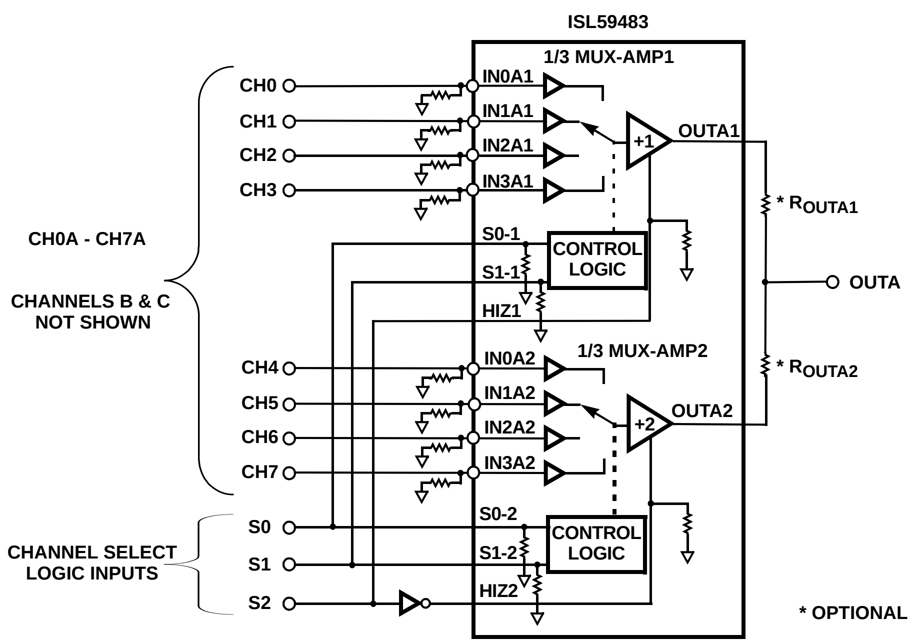
MUX Application Circuits

Each of the two 4:1 triple MUX amplifiers have their own binary-coded, TTL compatible channel select logic inputs (S0-1, 2, and S1-1, 2). All three amplifiers are switched simultaneously from their respective inputs with S0-1 S1-1 controlling MUX 1, and S0-2, S1-2 controlling MUX 2.

The HIZ control inputs (HIZ1, HIZ2) and device enable control inputs ($\overline{EN1}$ and $\overline{EN2}$) control MUX 1 and MUX 2 in a similar fashion. The individual control for each 4:1 triple MUX enables external connections to configure the device for different MUX applications.

8:1 RGB Dual Gain Video MUX

The triple input RGB 8:1 MUX (Figure 44) connects the RGB amplifier output of MUX 1 to the parallel-connected RGB amplifier output of MUX 2 to produce a single RGB video output. Input channels CH0 to CH3 are assigned to MUX 1 and have a throughput gain of 1. Channels CH4 through CH7 are assigned to MUX 2 and have a throughput gain of 2. Channels CH0 through CH3 are selected by setting S2 low, which forces HIZ1 low and HIZ2 high (enables MUX 1 and three-states MUX 2). Setting S2 high reverses the logic inputs of HIZ1, HIZ2 and switches from MUX 1 to MUX 2, enabling the selection of channels CH4 through CH7. The channel select inputs are parallel connected (S0-1 to S0-2) and S1-1 to S1-2) to form two logic controls, S0 and S1. The logic control truth table is shown in Figure 44.



CHANNEL SELECT TRUTH TABLE

8:1 VIDEO MUX

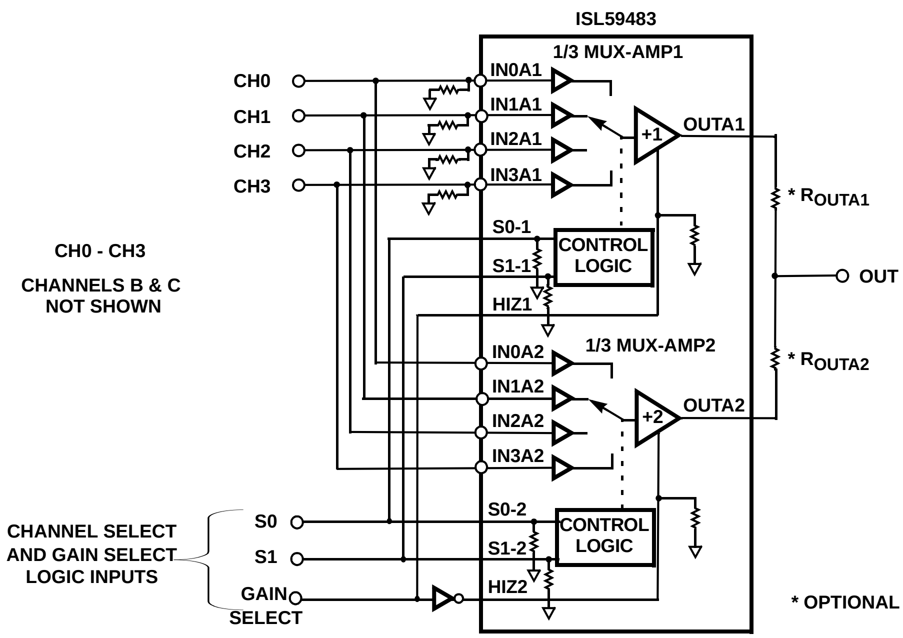
S2	S1	S0	GAIN	OUTA, B, C
0	0	0	1	CH0A, B, C
0	0	1	1	CH1A, B, C
0	1	0	1	CH2A, B, C
0	1	1	1	CH3A, B, C
1	0	0	2	CH4A, B, C
1	0	1	2	CH5A, B ,C
1	1	0	2	CH6A, B, C
1	1	1	2	CH7A, B, C

* OPTIONAL - DEPENDING ON PARASITIC CAPACITANCE

FIGURE 44. APPLICATION CIRCUIT FOR A DUAL GAIN 8:1 RGB VIDEO MUX

4:1 RGB Dual Gain Video MUX

Connecting the MUX inputs and outputs in parallel allows the 8 channel ISL59483 to be used as a 4:1 RGB MUX with selectable gains of 1 or 2 (Figure 10). In this example, the high input impedance of the MUX enables each input video line to be shared by any number of MUX input pins. The gain select logic function is created by providing complememtary logic to the HIZ1 and HIZ2 pins. Channels CH0 through CH3 are selected by connecting the MUX 1 and MUX 2 S0-1, 2 and S1-1, 2 channel select inputs together to form channel select (S0 and S1), as shown in the truth table in Figure 10.



CHANNEL SELECT TRUTH TABLE
DUAL GAIN 4:1 VIDEO MUX

S1	S1	GAIN SELECT	GAIN	OUTA, B, C
0	0	0	1	CH0A, B, C
0	0	0	1	CH1A, B, C
1	1	0	1	CH2A, B, C
1	1	0	1	CH3A, B, C
0	0	1	2	CH0A, B, C
0	0	1	2	CH1A, B, C
1	1	1	2	CH2A, B, C
1	1	1	2	CH3A, B, C

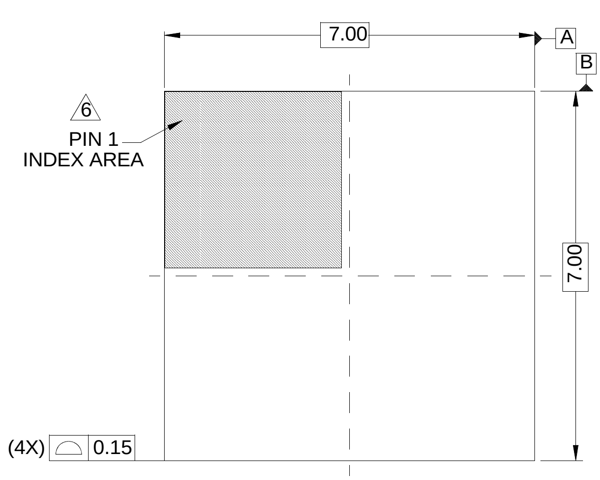
* OPTIONAL - DEPENDING ON PARASITIC CAPACITANCE

FIGURE 45. APPLICATION CIRCUIT FOR DUAL GAIN 4:1 VIDEO MUX

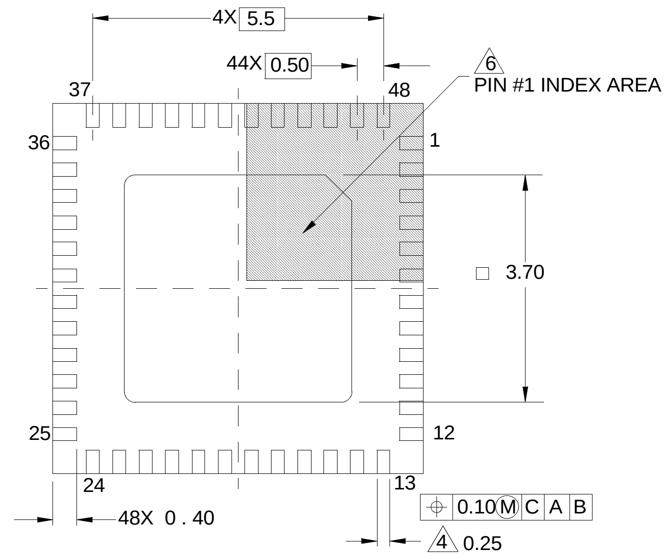
Package Outline Drawing

L48.7x7B

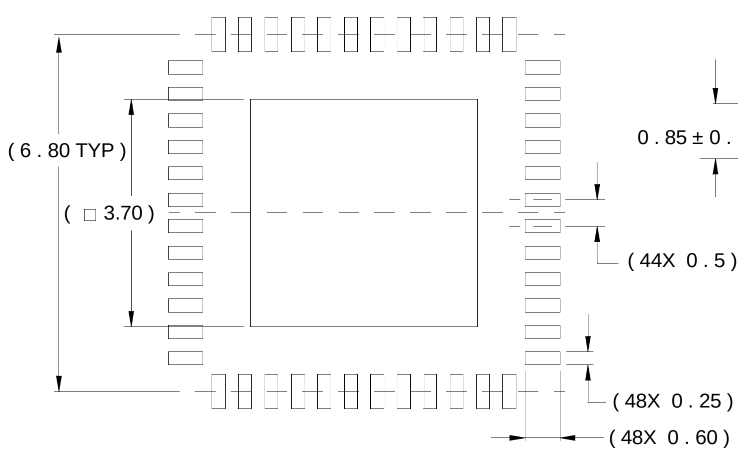
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 12/06



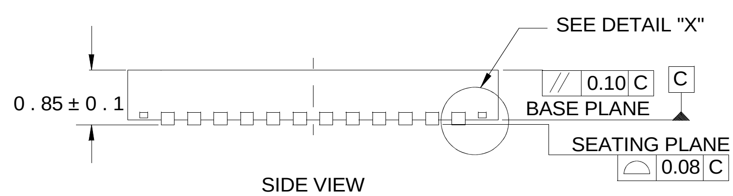
TOP VIEW



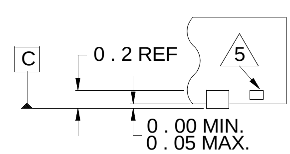
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.