TD40MCA Datasheet

CENTELLAX

DC-40 GHz
Divide-by-2/4/8 Test Accessory

Features

- Wide Frequency Range: 0.2 - 40 GHz
- High Input Sensitivity
- Very Low Jitter
- Fast Rise/Fall Times
- Divide-by-2/4/8 Outputs
- AC Power Supply Included
- Size: 3.5” x 4.0” x 1”

Description

The TD40MCA divider is a general purpose test accessory designed for microwave, communications and test applications. The accessory simultaneously provides divide-by-2, divide-by-4, and divide-by-8 outputs. The single-ended input is accessed from the rear via a 2.9mm connector while the outputs are provided at the front panel via SMA connectors. All inputs and outputs are AC coupled. The divider is self contained and plugs into standard AC power sources.

Application

The TD40MCA divider can be used to extend the trigger range of high speed sampling oscilloscopes. Precision timebase measurements will benefit from the very low added jitter and fast waveform edges. The TD40MCA can be used to generate sychronized, high frequency clocks from existing sinusoidal, synthesized sources. The low 1/f phase noise characteristics of the divider will benefit high frequency phase lock loop designs.

Key Specifications (Specifications pertain to measurements @ 25°C)

Parameter	Description	Minimum	Typical	Maximum
S11 (dB)	Input Return Loss	-	-10	-
S22 (dB)	Div-by-2 Output Return Loss	-	-12	-
S33 (dB)	Div-by-4 Output Return Loss	-	-10	-
S44 (dB)	Div-by-8 Output Return Loss	-	-10	-
Jrms (fs)	Output RMS Jitter	-	<400	500
Trf (ps)	Output Rise/Fall Times	-	30	35
F_{max} (GHZ)	Maximum Division Frequency	38	40	-
P_{in} (dBm)	Nominal Input Power	-	0	+10
P_{out} (dBm)	Nominal Output Power	-6	-3	-
$\mathcal{L}$(dBc/Hz)	SSB Phase Noise @ 100kHz offset	-	-153	-

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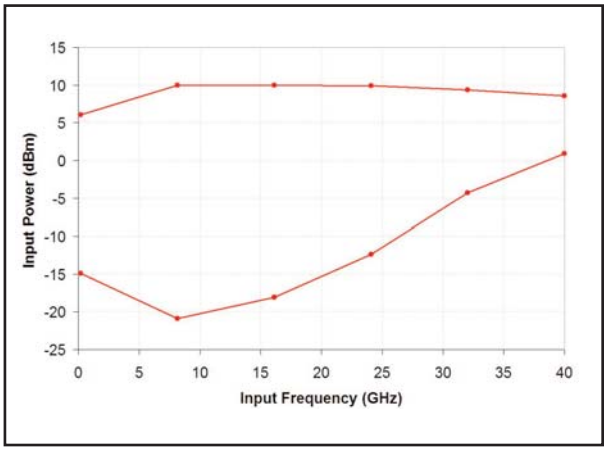
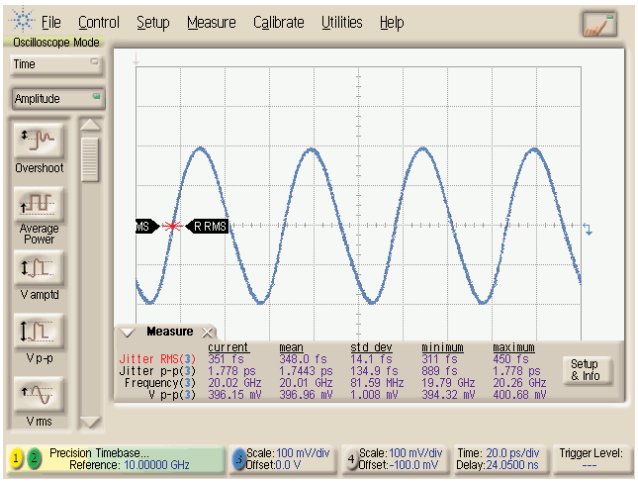
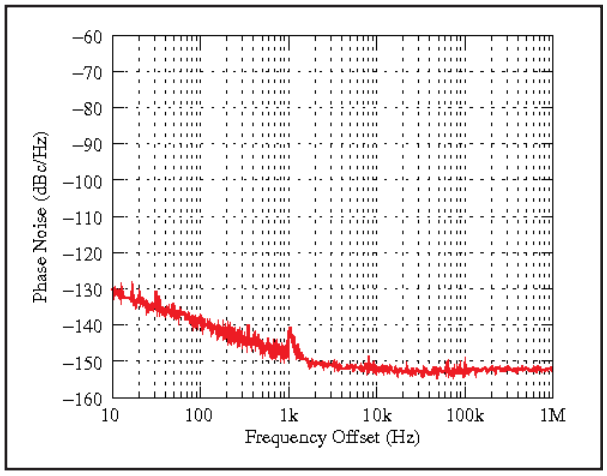


input Sensitivity Window
Min/Max Single-Ended Input Power



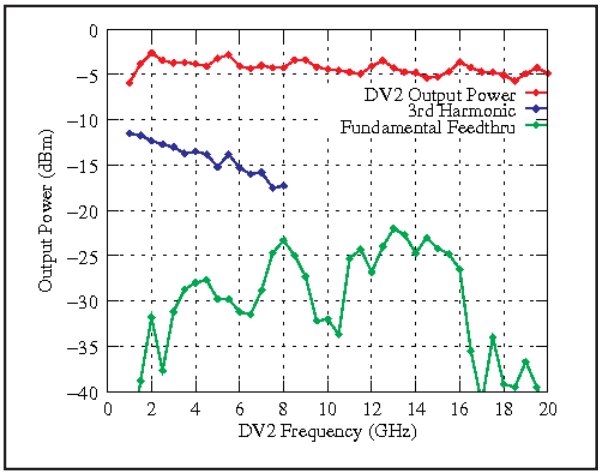
Divide-by-2 Output Waveform
Input Signal: 40 GHz @0dBm



SSB Phase Noise of Div-by-8 port
Input Freq = 7.8 GHz

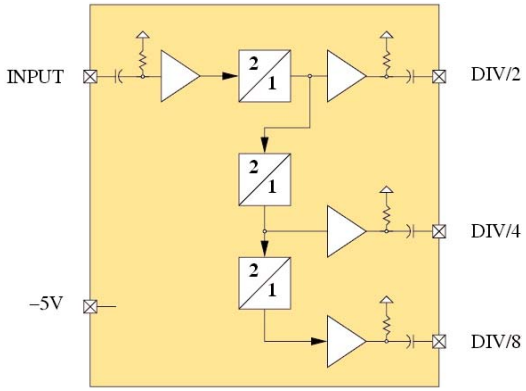
TD40MCA Front Panel

TD40MCA Rear Panel



Divide-by-2 Output Power,
3rd Harmonic & Input Feedthru

Functional Block Diagram



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