

FEATURES

Low Offset Voltage Drift
Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Currents
Crosstalk: -124 dB at 1 kHz
Low Bias Current: 35 pA max Warmed Up
Low Offset Voltage: 250 μ V max
Low Input Voltage Noise: 2 μ V p-p
High Open Loop Gain: 108 dB
Low Quiescent Current: 2.8 mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pinout
Available in Hermetic Metal Can Package, Hermetic Surface Mount (20-Pin LCC) and Chip Form
MIL-STD-883B Processing Also Available
Single Version Available: AD547

PRODUCT DESCRIPTION

The AD647 is an ultralow drift, dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100 μ V (250 μ V max) and drifts of 2.5 μ V/ $^{\circ}$ C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

The high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

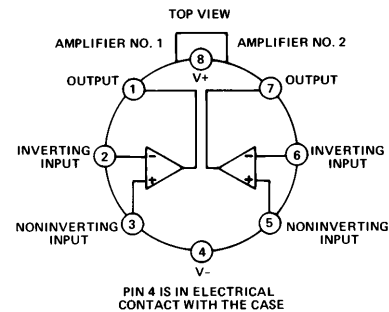
The AD647 is offered in four performance grades, three commercial (the J, K and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages and are available processed to MIL-STD-883B. The LCC version is also available processed to MIL-STD-883B.

REV. A

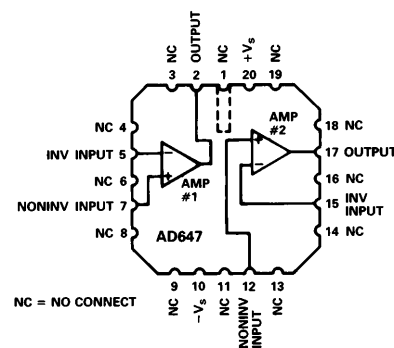
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PIN CONFIGURATION

TO-99 (H) Package



LCC (E) Package



PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250 μ V and 2.5 μ V/ $^{\circ}$ C max.
3. Voltage noise is guaranteed at 4 μ V p-p max (0.1 Hz to 10 Hz) on K, L and S grades.
4. Bias current (35 pA K, L, S; 75 pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8 mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pinout permits the direct substitution of the AD647 for lower performance devices.
8. The AD647 is available in chip form.

AD647—SPECIFICATIONS (@ +25°C and $V_S = \pm 15$ V dc)

Model	AD647J			AD647K			AD647L			AD647S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN $V_O = \pm 10$ V, $R_L \geq 2$ k Ω T_{MIN} to T_{MAX} , $R_L = 2$ k Ω	100,000			250,000			250,000			250,000			V/V V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2$ k Ω , T_{MIN} to T_{MAX}	± 10	± 12		± 10	± 12		± 10	± 12		± 10	± 12		V
Voltage @ $R_L = 10$ k Ω , T_{MIN} to T_{MAX}	± 12	± 13		± 12	± 13		± 12	± 13		± 12	± 13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0		V/ μ s
INPUT OFFSET VOLTAGE ¹													
Initial Offset			1.0			0.5			0.25			0.5	mV
Input Offset Voltage vs. Temperature			10			5			2.5			5.0	μ V/ $^{\circ}$ C
Input Offset Voltage vs. Supply, T_{MIN} to T_{MAX}			200			100			100			100	μ V/V
INPUT BIAS CURRENT ²													
Either Input		10	75		10	35		10	35		10	35	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS ³													
Input Offset Voltage			1.0			0.5			0.25			0.5	mV
Input Offset Voltage T_{MIN} to T_{MAX}			10			5			2.5			10.0	μ V/ $^{\circ}$ C
Input Bias Current			35			25			25			25	pA
Crosstalk		-124			-124			-124			-124		dB
INPUT IMPEDANCE													
Differential		10 ¹² 6			10 ¹² 6			10 ¹² 6			10 ¹² 6		M Ω pF
Common Mode		10 ¹² 6			10 ¹² 6			10 ¹² 6			10 ¹² 6		M Ω pF
INPUT VOLTAGE RANGE													
Differential ⁴		± 20			± 20			± 20			± 20		V
Common Mode	± 10	± 12		± 10	± 12		± 10	± 12		± 10	± 12		V
Common-Mode Rejection		76			80			80			80		dB
INPUT NOISE													
Voltage 0.1 Hz to 10 Hz		2			4			4			4		μ V p-p nV/ $\sqrt{\text{Hz}}$
f = 10 Hz		70			70			70			70		nV/ $\sqrt{\text{Hz}}$
f = 100 Hz		45			45			45			45		nV/ $\sqrt{\text{Hz}}$
f = 1 kHz		30			30			30			30		nV/ $\sqrt{\text{Hz}}$
f = 10 kHz		25			25			25			25		nV/ $\sqrt{\text{Hz}}$
POWER SUPPLY													
Rated Performance		± 15			± 15			± 15			± 15		V
Operating	± 5		± 18	± 5		± 18	± 5		± 18	± 5		± 18	V
Quiescent Current		2.8			2.8			2.8			2.8		mA
TEMPERATURE RANGE													
Operating, Rated Performance		0	+70		0	+70		0	+70		-55	+125	$^{\circ}$ C
Storage		-65	+150		-65	+150		-65	+150		-65	+150	$^{\circ}$ C
PACKAGE OPTION													
TO-99 Style (H-08B)		AD647JH			AD647KH			AD647LH			AD647SH		
LCC (E-20A)											AD647SE		
											AD647SE/883BH		

NOTES

¹Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}\text{C}$.

²Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at $T_A = +25^{\circ}\text{C}$. For higher temperatures, the current doubles every 10°C .

³Matching is defined as the difference between parameters of the two amplifiers.

⁴Defined as the maximum safe voltage between inputs, such that neither exceeds ± 10 V from ground.

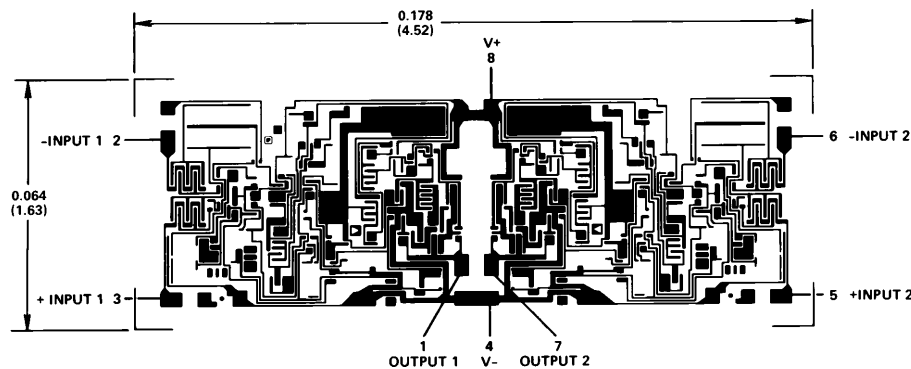
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).

Contact factory for latest dimensions.



Typical Characteristics—AD647

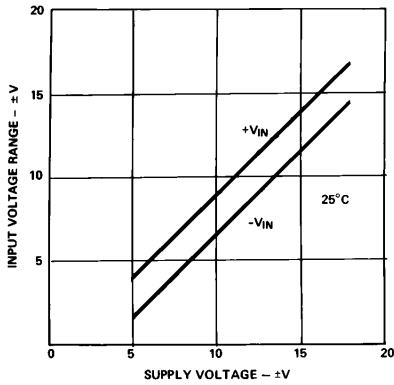


Figure 1. Input Voltage Range vs. Supply Voltage

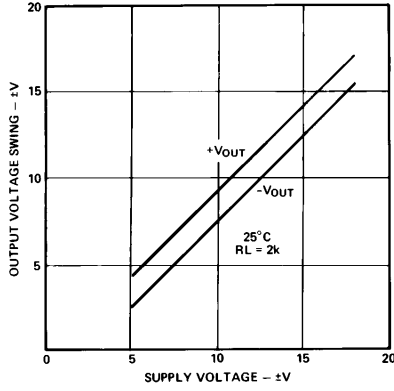


Figure 2. Output Voltage Swing vs. Supply Voltage

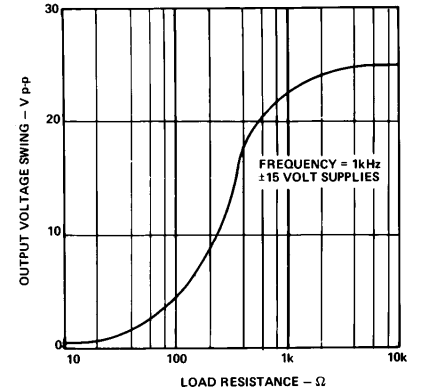


Figure 3. Output Voltage Swing vs. Load Resistance

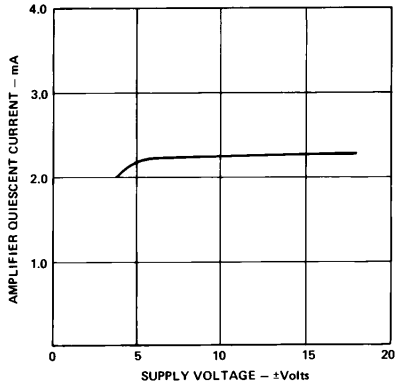


Figure 4. Quiescent Current vs. Supply Voltage

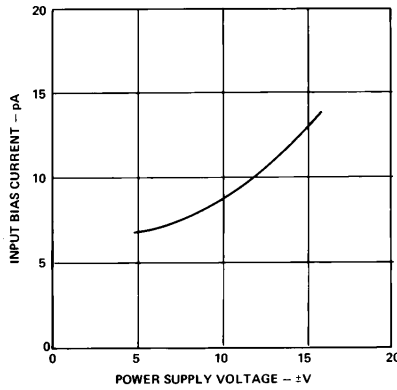


Figure 5. Input Bias Current vs. Power Supply Voltage

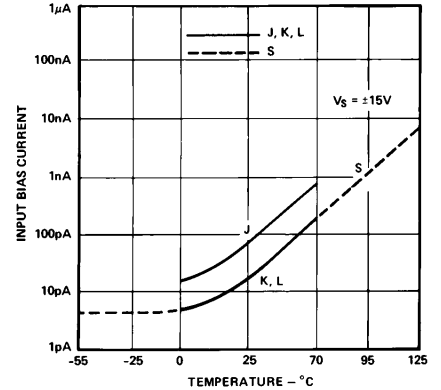


Figure 6. Input Bias Current vs. Temperature

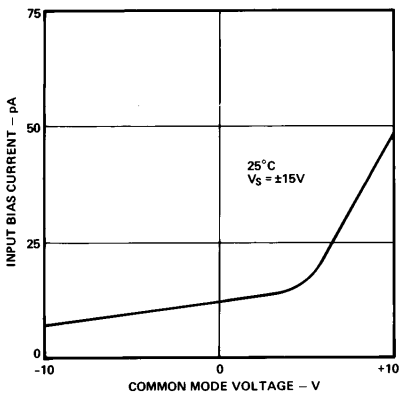


Figure 7. Input Bias Current vs. CMV

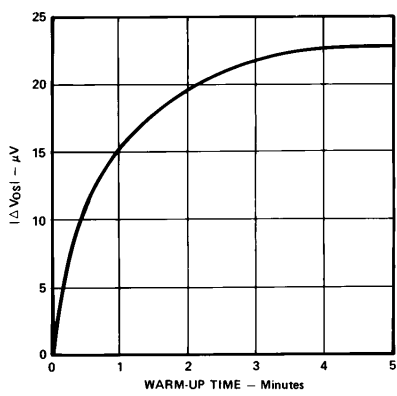


Figure 8. Change in Offset Voltage vs. Warm-Up Time

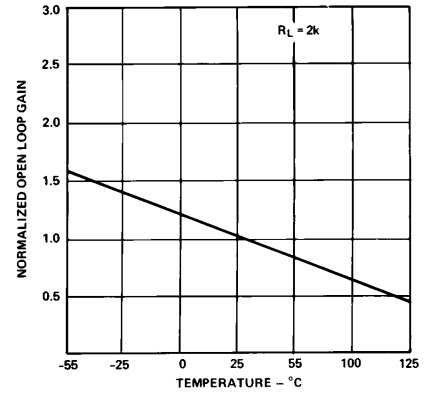


Figure 9. Open Loop Gain vs. Temperature

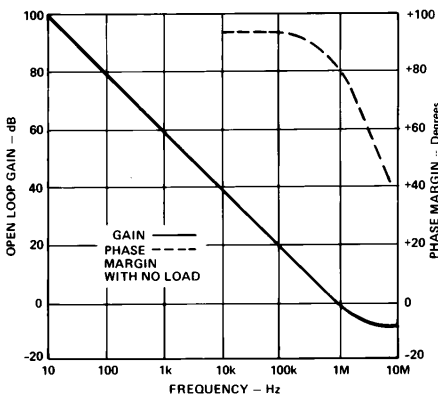


Figure 10. Open Loop Frequency Response

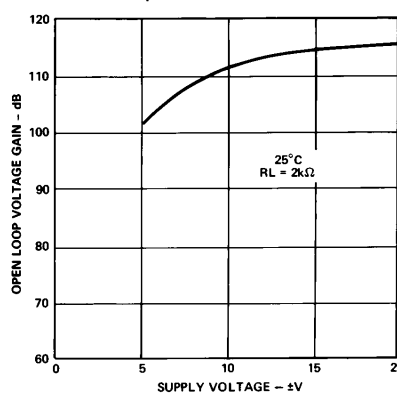


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

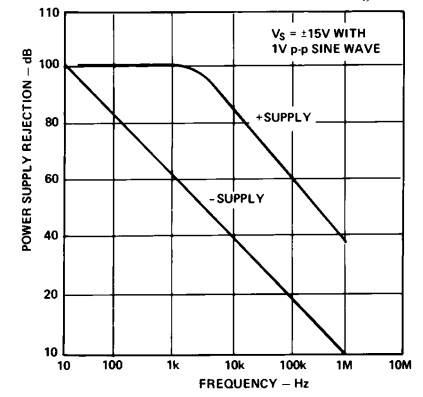


Figure 12. Power Supply Rejection vs. Frequency

AD647

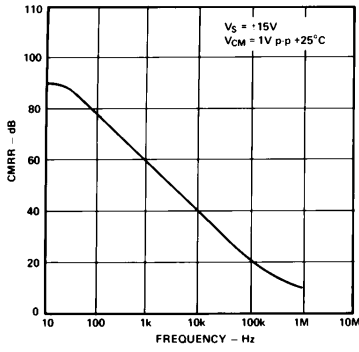


Figure 13. Common-Mode Rejection Ratio vs. Frequency

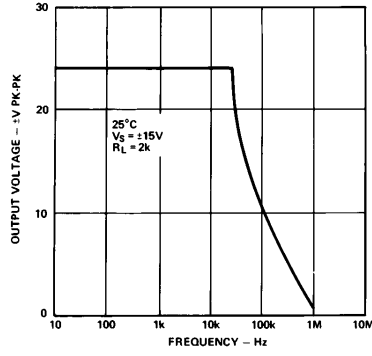


Figure 14. Large Signal Frequency Response

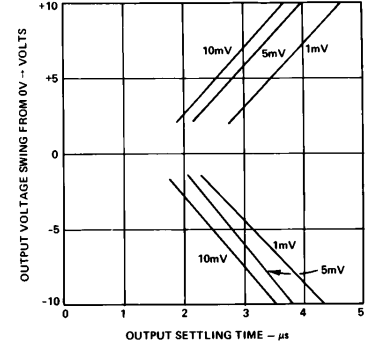


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

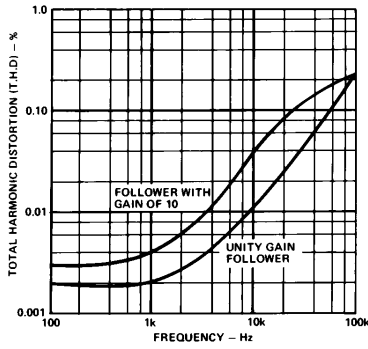


Figure 16. Total Harmonic Distortion vs. Frequency

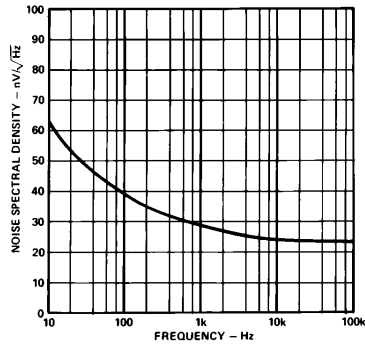


Figure 17. Input Noise Voltage Spectral Density

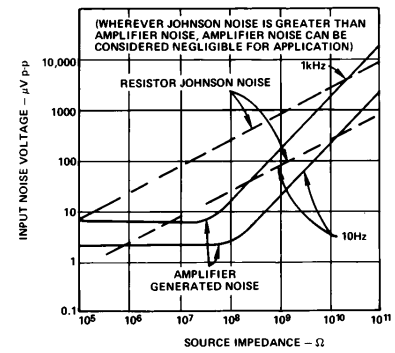
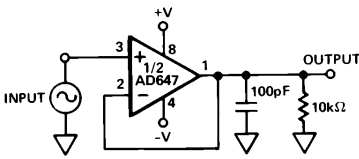
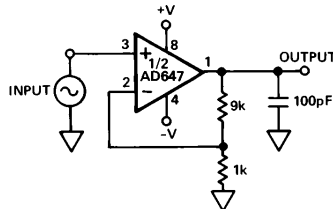


Figure 18. Total RMS Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

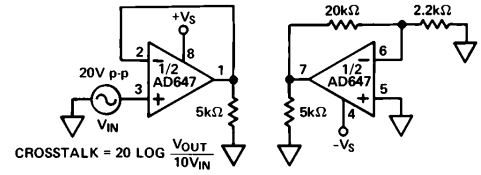


Figure 20. Crosstalk Test Circuit

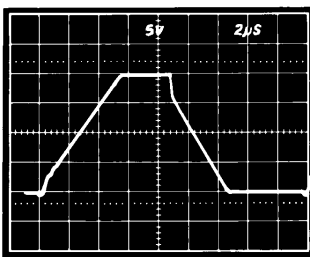


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

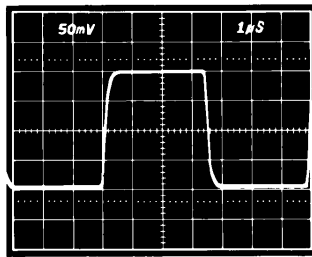


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

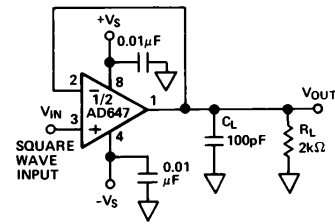


Figure 21c. Unity Gain Follower

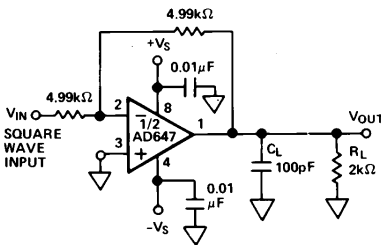


Figure 22a. Unity Gain Inverter

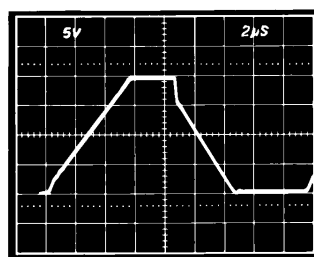


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

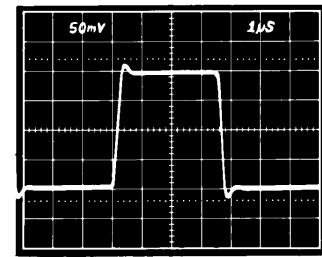


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD647 is fully specified under actual operating conditions to insure high performance in any application, but there are some steps that will improve on even this high level of performance.

The bias current of a JFET amplifier doubles with every 10°C increase in junction temperature. Any heat source that can be eliminated or minimized will significantly improve bias current performance. To account for normal power dissipation, the largest contributor to chip self-heating, the bias currents of the AD647 are guaranteed fully warmed up with ±15 V supplies. A decrease in supply voltage will decrease power consumption, resulting in a corresponding drop in bias currents.

Open loop gain and bias currents, to some extent, are affected by output loading. In applications where high linearity is essential, load impedance should be kept as high as possible to minimize degradation of open loop gain.

The outstanding ac and dc performance of the AD647 make it an ideal choice for critical instrumentation applications. In such applications, leakage paths, line losses and external noise sources should be considered in the layout of printed circuit boards. A guard ring surrounding the inputs and connected to a low impedance potential (at the same level as the inputs) should be placed on both sides of the circuit board. This will eliminate leakage paths that could degrade bias current performance. All signal paths should be shielded to minimize noise pickup.

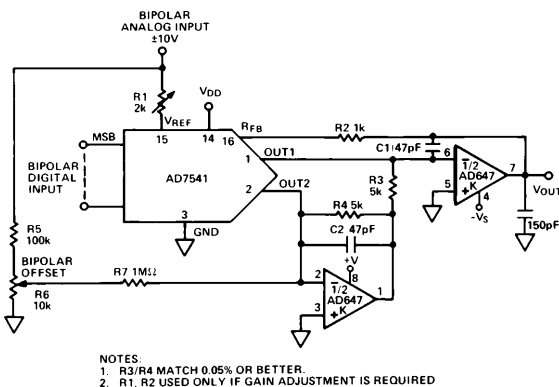


Figure 23. AD647 Used as DAC Output Amplifier

A CMOS DAC AMPLIFIER

The output impedance of a CMOS DAC, such as the AD7541, varies with digital input code. This causes a corresponding variation in the noise gain of the DAC-amplifier combination. This noise gain modulation introduces a nonlinearity whose magnitude is dependent on the amount of offset voltage present.

Laser wafer drift trimming lowers the initial offset voltage and the offset voltage drift of the AD647, therefore minimizing the effect of this nonlinearity and its drift with temperature. This, in conjunction with the low bias current and high open loop gain, makes the AD647 ideal for DAC output amplifier applications.

THE AD647 USED WITH THE AD7546

Figure 24 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

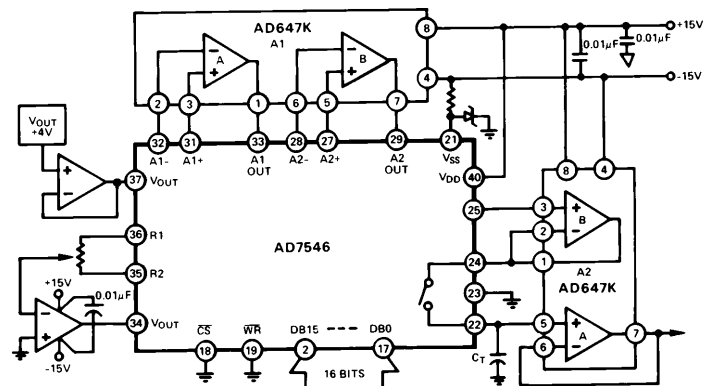


Figure 24. AD647 Used with AD7546 16-Bit DAC

USING THE AD647 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

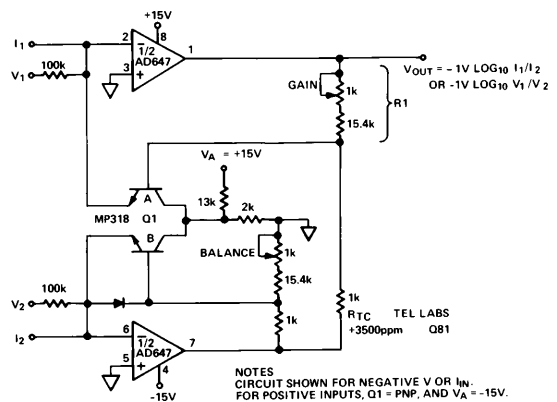


Figure 25. Log-Ratio Amplifier

