ANALOG DEVICES

ADSL Chipset

AD6435

FEATURES

Component in Analog Devices DMT ADSL Chipset—AD20msp910
Designed to ANSI/ETSI T1.413
Suitable for CO or Residence (ATU-R and ATU-C)
Performs All Digital Interface Tasks:
- **Elastic Store; Byte-Stuffing/Robbing**
- **Synchronization and EOC and AOC Insertion/Removal**
- **CRC Generation/Detection**
- **Scrambler and Descrambler**
- **Forward Error Correction/Detection**
- **Interleave/Deinterleave**

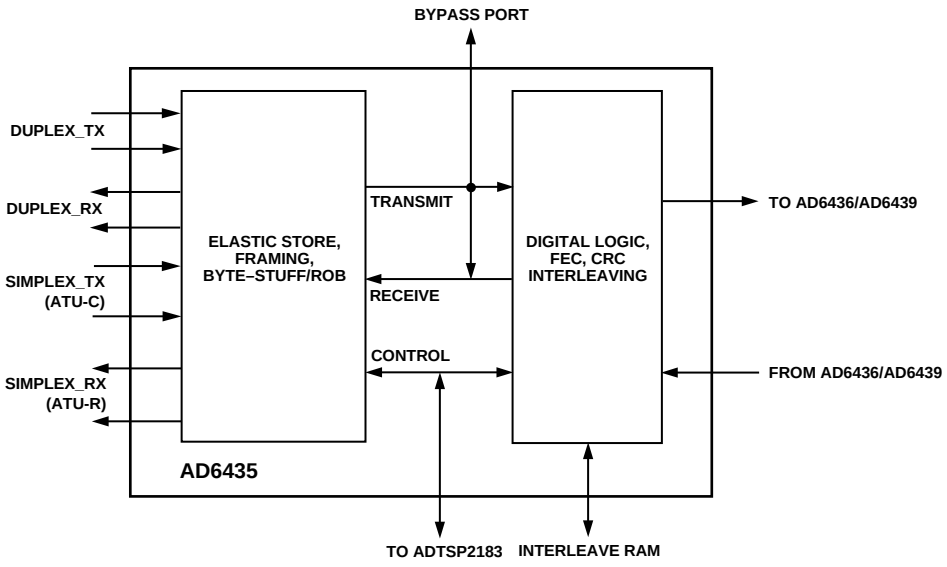
Absolute Maximum Data Rate: 12 Mbps Simplex/4 Mbps Duplex
Simple Interface: Synchronous Simplex and Duplex Streams
128-Lead TQFP
Operating Temperature Range: –40°C to +85°C
3.3 V Operation, 400 mW

GENERAL DESCRIPTION

The AD6435 is part of the Analog Devices ADSL chipset, the AD20msp910. It accompanies the AD6436 (DMT accelerator), AD6437 (single-chip analog front end) and ADTSP-2183 (control and DSP). Object code is also supplied. Offering a flexible, standard-based approach (designed to ANSI T1.413, Category 1) with low total bill of materials and high performance, the chipset offers a straightforward approach to realizing an ADSL modem.

The AD6435 interfaces the ADSL modem to the external system, at either CO or RT modem. It implements all the bit-stuffing/robbing and elastic store operations, and all digital processing (block and forward error correction, scrambling, interleaving, etc.). The AD6435 has four simple synchronous connections, duplex in and out, simplex in (only used at ATU-C) and simplex out (used at ATU-R), which may be treated as the AS0 Simplex and LS0 duplex stream of the standard. These have "clean" clock and data, and may operate asynchronously of one another, or of the modem itself.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD6435–SPECIFICATIONS

Parameter	Units	Comments
ABSOLUTE MAXIMUM SIMPLEX DATA RATE	12.288 Mbps	Absolute Maximum. May not be achieved under realistic conditions. Actual performance will depend on copper loop.
ABSOLUTE MAXIMUM DUPLEX DATA RATE	4.096 Mbps	Absolute Maximum. May not be achieved under realistic conditions. Actual performance will depend on copper loop.
INTERNAL PLL FOR CLOCK REGENERATION	176.64 MHz	Resolution is 172.5 Hz/Bit 0.076 Unit Intervals.
V_{DD} SUPPLY VOLTAGE	3.3 V ± 10%	
POWER DISSIPATION	400 mW	Typical
T_A OPERATING TEMPERATURE	–40°C to +85°C	

Specifications are subject to change without notice.

ELECTRICAL SPECIFICATIONS

Parameter	Typ Value	Comments*
V_{OH}	V_{DD}–0.4 V dc	At I_{OH} = –0.5 mA
V_{OL}	0.4 V dc	At I_{OL} = +1.0 mA
V_{IH}	2.0 V dc	
V_{IL}	1.0 V dc	
I_{IH}	±500 nA	V_{IN} = V_{DD} = 3.6 V
I_{IL}	±500 nA	V_{IN} = 0 V, V_{DD} = 3.6 V

*V_{DD} = 3.3 V dc ± 10%.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

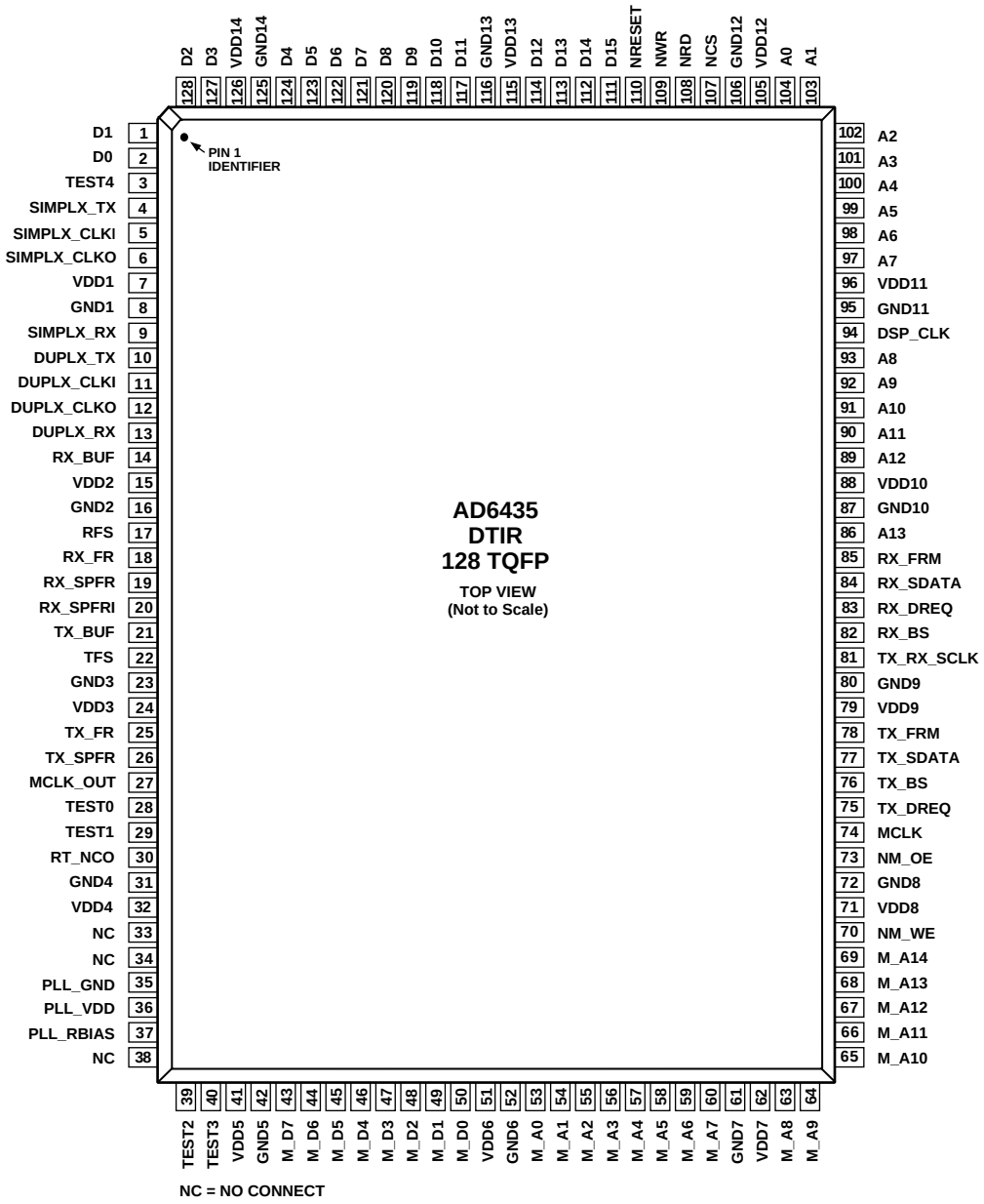
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6435	–40°C to +85°C	128-Lead Plastic Thin Quad Flatpack	ST-128

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6435 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NC = NO CONNECT

PIN DESCRIPTION

The AD6435 contains 91 signal pins, 33 output pins, 35 input pins, and 24 bidirectional pins. There are also 5 test pins and 28 digital supply pins, 2 analog supply pins, and 1 PLL bias pin for the PLL.

PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Name	Type	Description
1–2	D1, D0	I/O	16-Bit Data Bus for DSP Port. See also 111:114, 117:124, 127:128.
3	TEST4	Input	Tie to Ground Through a 10 kΩ Resistor.
4	SIMPLX_TX	Input	Input Downstream Data at CO. Pin not used at RT.
5	SIMPLX_CLKI	Input	Input Clock at CO for Downstream Data. Pin is not used at RT.
6	SIMPLX_CLKO	Output	Recovered Downstream Clock at RT. Pin not used at CO.
7	VDD1	Supply	3.3 V.
8	GND1	Supply	Ground.
9	SIMPLX_RX	Output	Received Downstream Data at RT. Pin not used at CO.
10	DUPLX_TX	Input	Input Duplex Data.
11	DUPLX_CLKI	Input	Input Duplex Clock.
12	DUPLX_CLKO	Output	Recovered Duplex Clock.
13	DUPLX_RX	Output	Received Duplex Data Stream.
14	RX_BUF	Output	TICL Bypass—RX Data Buffer. If TCIL is not used, this pin must have a pull-up resistor.
15	VDD2	Supply	3.3 V.
16	GND2	Supply	Ground.
17	RFS	Output	TICL Bypass—RX Byte Sync.
18	RX_FR	Output	TICL Bypass—RX Frame Sync. 10 kΩ to Ground.
19	RX_SPFR	Output	TICL Bypass—TICL Superframe Sync.
20	RX_SPFRI	Output	TICL Bypass—RX Interleaved Superframe Sync.
21	TX_BUF	Input	TICL Bypass—TX Data Buffer.
22	TFS	Output	TICL Bypass—TX Byte Sync.
23	GND3	Supply	Ground.
24	VDD3	Supply	3.3 V.
25	TX_FR	Output	TICL Bypass—TX Frame Sync.
26	TX_SPFR	Output	TICL Bypass—TX Superframe Sync.
27	MCLK_OUT	Output	TICL Bypass—Output MCLK.
28	TEST0		No Connection.
29	TEST1		No Connection.
30	RT_NCO		Mode Pin, 1 = RT Mode, 0 = CO Mode.
31	GND4	Supply	Ground.
32	VDD4	Supply	3.3 V.
33, 34	NC		No Connect.
35	PLL_GND		PLL Analog Ground.
36	PLL_VDD		PLL Analog Power.
37	PLL_RBIAS		Tie to Ground Through a 30 kΩ Resistor.
38	NC		No Connect.
39	TEST2	Input	Tie to Ground Through a 10 kΩ Resistor.
40	TEST3	Three-State	No Connection.
41	VDD5	Supply	3.3 V.
42	GND5	Supply	Ground.
43–50	M_D7–0	I/O	Data for Interleave Ram.
51	VDD6	Supply	3.3 V.
52	GND6	Supply	Ground.
53–60	M_A0–7	Output	Address Bus for Interleave Ram. See also Pins 60–66.

PIN FUNCTION DESCRIPTIONS (Continued)

Pin No.	Pin Name	Type	Description
61	GND7	Supply	Ground.
62	VDD6	Supply	3.3 V.
63–69	M_A8–14	Output	Address Bus for Interleave Ram. See also Pins 50–57.
70	NM_WE	Output	Write Enable for Interleave Ram.
71	VDD8	Supply	3.3 V.
72	GND8	Supply	Ground.
73	NM_OE	Output	Output Enable for Interleave Ram.
74	MCLK	Input	The AD6435 Master Clk (35.328 MHz).
75	TX _DREQ	Input	Data Request Provided by the AD6436.
76	TX _BS	Output	Transmit Byte Strobe Provided by the AD6435.
77	TX _SDATA	Output	Transmit Serial Data Provided by the AD6435.
78	TX _FRM	Input	Transmit Frame Strobe Provided by the AD6436.
79	VDD9	Supply	3.3 V.
80	GND9	Supply	Ground.
81	TX _RX_SCLK	Input	Transmit and Receive Serial Clock.
82	RX_BS	Input	Receive Byte Strobe Provided by the AD6436.
83	RX_DREQ	Output	Receive Data Request Provided by the AD6435.
84	RX_SDATA	Input	Receive Serial Data Provided by the AD6436.
85	RX_FRM	Input	Receive Frame Strobe Provided by the AD6436.
86	A13	Input	14-Bit Address Bus for DSP Port. See also 86–90 and 94–101.
87	GND10	Supply	Ground.
88	VDD10	Supply	3.3 V.
89–93	A12–A8	Input	14-Bit Address Bus for DSP Port. See also 83 and 94–101.
94	DSP_CLK	Input	DSP Output Clock.
95	GND11	Supply	Ground.
96	VDD11	Supply	3.3 V.
97–104	A7–0	Supply	14-Bit Address Bus for DSP Port. See also 83 and 86–90.
105	VDD12	Supply	3.3 V.
106	GND12	Supply	Ground.
107	NCS	Input	DSP Memory Select. Active Low.
108	NRD	Input	DSP Memory Read Enable, Active Low.
109	NWR	Input	DSP Write Enable, Active Low.
110	NRESET	Input	Reset Pin, Active Low.
111–114	D15–D12	I/O	16-Bit Data Bus for DSP Port. See also 1–2, 117–124, 127–128.
115	VDD13	Supply	3.3 V.
116	GND13	Supply	Ground.
117–124	D11–D4	I/O	16-Bit Data Bus for DSP Port. See also 1–2, 111–114, 127–128.
125	GND14	Supply	Ground.
126	VDD14	Supply	3.3 V.
127, 128	D3–D2	I/O	16-Bit Data Bus for DSP Port. See also 1–2, 111–114, 117–124.

INTRODUCTION

The AD6435 is the interface chip in the AD20msp910 ADSL chipset, connecting the core transceiver functions to the external system. The other portions within the AD20msp910 chipset are the AD6436 (which connects to the AD6435 and is responsible for the core DMT signal processing), the AD6437 analog front-end IC, the AD816 driver/receiver and ADTSP2183, which is used as the system control processor. An object code licence for all modem software is supplied with the AD20msp910 chipset.

The AD6435 implements a generic interface, with straightforward synchronous clock and data streams corresponding to simplex and duplex bearer channels. These can be considered as the AS0 (simplex) and LS0 (duplex) streams as per the standard, but can run at any rate; the "duplex" channel can be treated as two independent streams, one up and one down. This implementation is a simplified variant of that described in ANSI T1.413. It is easy to use this structure to connect to the rest of the system, or to external devices, such as framers or dedicated ICs for particular protocols. Variants of the AD6435 with support for specific functions or interfaces (e.g., ATM, Ethernet) are under development.

There are two main blocks within the AD6435:

- The digital processing section (Digital Interface Area or "DIA"), which is responsible for error correction, scrambling, interleaving, AOC and control operations. This is based on the earlier AD6442 device. This is a highly programmable system, whose operation is not restricted to the operating modes as defined in ANSI T1.413, but which could be used in variety of systems. The DIA supports the following codeword cases:
  a. One codeword per frame in the fact and/or interleaved data portion of a frame.
  b. Multiple codewords per frame in the fast and/or interleaved data portion, providing the codeword length evenly divides into the output (DME) frame length.
  c. Multiple frames per codeword on the interleaved portion of the frame only, up to 20 frames per codeword. The number of checkbytes must be an integer multiple of the number of frames in the codeword.
  d. Codewords may span superframes.
- The interface block (Transceiver Interface and Control Logic or "TICL"), which handles the framing, signal buffering and data retiming functions required to support clean synchronous data streams. (This essentially corresponds to the transmission convergence layer of a stack.) As some designs may not require the TICL block, there is a bypass mode, in which this block is powered down and there is access to the unformatted/unframed data stream from the DIA.

This data sheet gives a user's description of the AD6435. It describes functionality and interfacing, but does not give any details of the internal structure. For details of the internal structure, see the AD6435 User's Manual, available on request.

When used as part of the AD20msp910 ADSL chipset, the internal functionality is under the control of the firmware supplied with the ADTSP2183, and the Messaging Protocol (MP) implemented there. This protocol supplies a hardware-neutral method of controlling the operation of the ADSL chipset, which will be compatible between different hardware implementations.

The AD6435 can implement rate adaptive ADSL (RADSL). This is under the control of the MP, and several different modes are supported.

The absolute maximum data rate of the AD6435 is 12 Mbps downstream, and 4 Mbps upstream. However, the rate depends primarily on the channel conditions, and these rates will not be achieved on real loops, with attenuation and crosstalk.

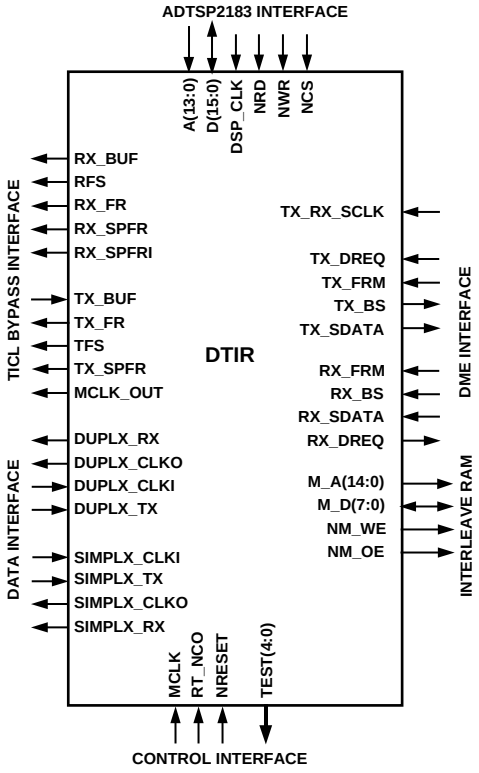


Figure 1. Functional Diagram

INTERFACES

The standard interface is a very straightforward buffered and demultiplexed synchronous connection. It is physically the same at both ATU-R and ATU-C, and presents four channels—simplex in and out, duplex in and out—with just two signals per connection, clock and data (obviously, only three of these channels can be used at an end; with the ATU-C using simplex_in and the ATU-R simplex_out). These streams are independent and can be used asynchronously of one another. No framing signals are provided.

The "duplex" stream can be used as a true duplex carrier (same rates upstream and downstream) or the two may be independent (i.e., the chipset has two simplex downstream paths, one fast and one slower, and one simplex upstream).

Table I. Interface Descriptions

Name	Description
duplex_rx	Duplex data output from the AD6435 (i.e., data received).
duplex_clko	Clock associated with duplex_rx (output).
duplex_tx	Duplex data input to the AD6435 (i.e., data to be transmitted).
duplex_clki	Clock associated with duplex_tx input.
simplex_rx	Simplex data output from the AD6435. ATU-R: downstream data received. ATU-C: not used.
simplex_clko	Clock associated with simplex_rx (output).
simplex_tx	Simplex data input to the AD6435. ATU-R: not used. ATU-C: downstream data to be sent.
simplex_clki	Clock associated with simplex_tx (input).

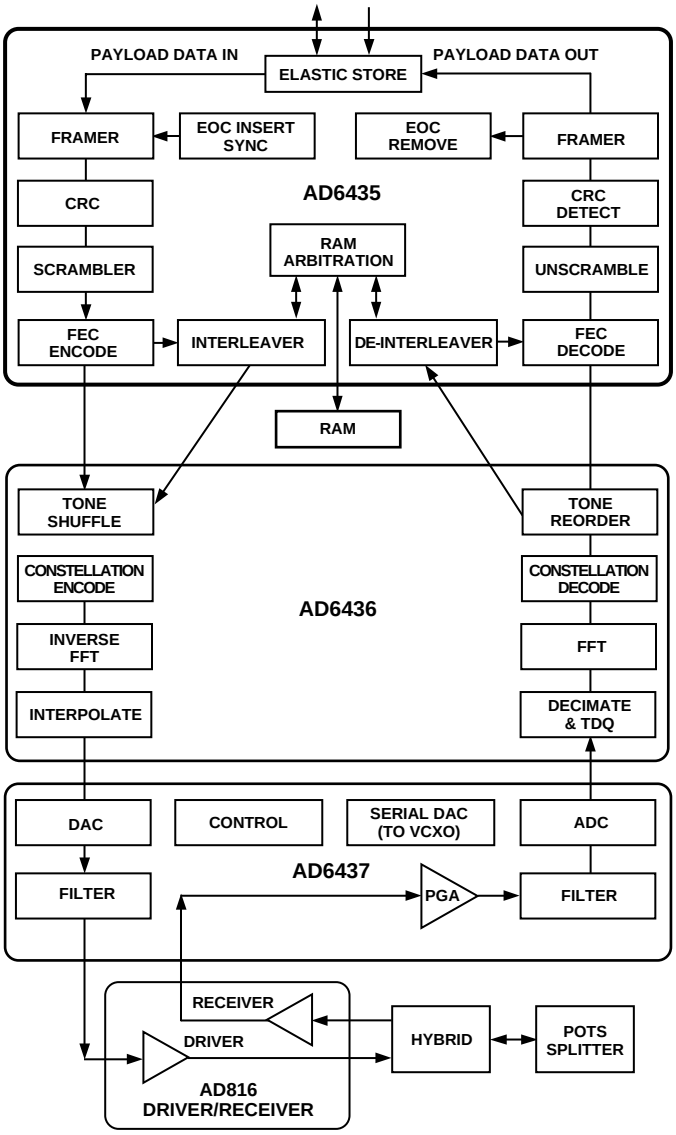


Figure 2. AD20msp910 System Block Diagram

In general tx clock signals (i.e., duplex_clcki, simplex_clki) are input to the AD6435, while the received data clock signals (duplex_clko, simplex_clko) are outputs. In other words, the sending modem (at ATU-C or ATU-R) supplies the clock to the AD6435, and the receiving modem's AD6435 recovers it (using a digital phase locked loop) and supplies it to the external system. The channels all have separate—independent—clocks.

There are two exceptions; the duplex streams can be "locked" with a single clock or, in a "one down/one up" system typical for data applications, the unused DPLL can be programmed to be a clock source at the desired data rate for the tx channel.

To avoid overflow/underflow of internal buffers, the clock rate of the streams should be held roughly constant. As such, although a degree of jitter or rate variation is supported, pure burst-mode is not, and idle cell insertion (deletion) is necessary and must be implemented by an external device.

Alternatively, the buffering multiplex/demultiplex and bit-stuff/rob operations may be bypassed (TICL bypass operation). These blocks are then powered down, reducing the AD6435's power consumption. The interface presented is then a "raw" stream of upstream and downstream data. As the elastic store has been disabled, these have the relic of the ADSL line superframe structure, and will show an irregular clock (with a pause for every 69th frame). This mode is compatible with the AD6442 DIA interface and is suited to packet (e.g., ATM) operation. It results in a slight power saving.

NB: Although the AD6435 can implement the T1.413 standard, and includes the required framing/interfacing (e.g., elastic store, bit-stuffing/robbing), it does not support the full optional suite of seven bearer streams (ASx and LSx) and associated multiplexing/demultiplexing as defined in T1.413. Instead, simple synchronous data streams are provided. These are essentially AS0 (simplex) and LS0 (duplex) but with variable rate or rate adaptive (not merely fixed multiples of standard PDH rates, as per Chapter 5 of T1.413). Additionally, the "duplex" stream can be treated as two independent streams, one up and one down. Indeed, in many applications, only one stream in each direction is required; in this case, the downstream duplex path is not used.

Further TC-layer operations can be defined by the system for their requirements (e.g., for V.35, ATM or 10BaseT), and simply interfaced to the AD6435 serial ports.

INTERFACE TIMING

The DTIR contains simplex (AS) and duplex (LS) channels that interface with the Central Office (CO) and Remote Terminal (RT). The DTIR contains a transmit serial port in which the DTIR transmits a bit stream to the DME and a receive serial port in which DTIR receives a serial bit stream from the DME. Since the DIA is being treated as a black box, the TICL-DIA interface will be defined here. This interface is similar to the DIA-DME transmit and receive interfaces. The DTIR also interfaces with a 32k × 8 Interleave RAM. The DTIR also has a DSP host port that allows a DSP to monitor the DTIR and control the data through the device.

CO/RT INTERFACE TIMING

Simplex Serial Port

The simplex serial port consists of four pins, two outputs, SIMPLX_RX and SIMPLX_CLKO, and two inputs, SIMPLX_TX and SIMPLX_CLKI. The serial clock rate is completely variable between 8 kbps and 12.288 Mbps. The interface operates differently at the CO and RT locations.

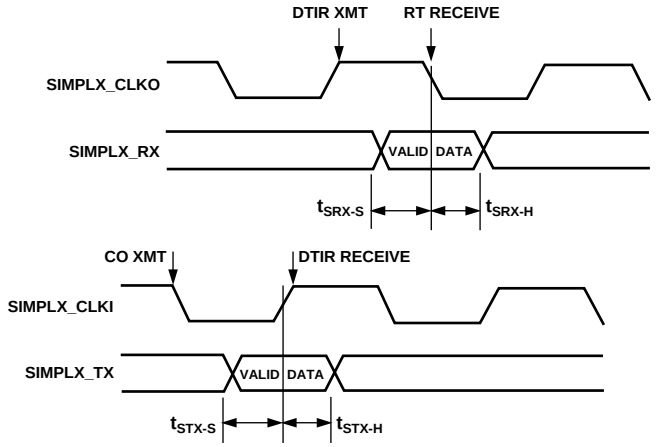


Figure 3. Simplex Serial Port

Table II. TX Serial I/F Timing

Parameter	Description	Typ
t_{SRX-S}	Setup Time of SIMPLX_RX from Falling Edge of SIMPLX_CLKO	5 ns
t_{SRX-H}	Hold Time of SIMPLX_RX from Falling Edge of SIMPLX_CLKO	5 ns
t_{STX-S}	Setup Time of SIMPLX_TX from Rising Edge of SIMPLX_CLKI	5 ns
t_{STX-H}	Hold Time of SIMPLX_TX from Rising Edge of SIMPLX_CLKI	5 ns

At the CO, the two input pins SIMPLX_TX and SIMPLX_CLKI are used while the two output pins SIMPLX_RX and SIMPLX_CLKO are not functionally connected. The interface can operate at a continuous data stream into SIMPLX_RX at a fixed frequency between 8 kbps and 12.288 Mbps. The data rate is set while the DTIR is in reset and does not change without going into the reset state again.

At the RT, the two output pins SIMPLX_RX and SIMPLX_CLKO are used while the two input pins SIMPLX_TX and SIMPLX_CLKI are not functionally connected. The interface can operate at a continuous data stream out of SIMPLX_RX at a fixed frequency between 8 kbps and 12.288 Mbps. The data rate is set while the DTIR is in reset and does not change without going into the reset state again.

For the Simplex Rx channel, data is driven out of the AD6435 on the positive edge of the respective CLKO signal and should be sampled by the external circuit on the negative edge.

For the Simplex Tx channel, the data is sampled by the AD6435 on the positive edge of the respective CLKO signal and should be driven by the external circuit on the negative edge.

Duplex Serial Port

The duplex serial port consists of four pins, two outputs, DUPLX_RX and DUPLX_CLKO, and two inputs, DUPLX_TX and DUPLX_CLKI. The serial clock rate is completely variable between 8 kbps and 4.096 Mbps. The interface operates identically at the CO and RT locations. The input interface can accept a continuous stream of data at a fixed frequency within the duplex rate. The output interface on the other end transmits the same continuous stream of data at the same fixed frequency. This frequency is established and programmed into the registers by the DSP during reset.

For the Duplex Rx channel, data is driven out of the AD6435 on the positive edge of the respective CLKO signal and should be sampled by the external circuit on the negative edge.

For the Duplex Tx channel, the data is sampled by the AD6435 on the positive edge of the respective CLKO signal and should be driven by the external circuit on the negative edge.

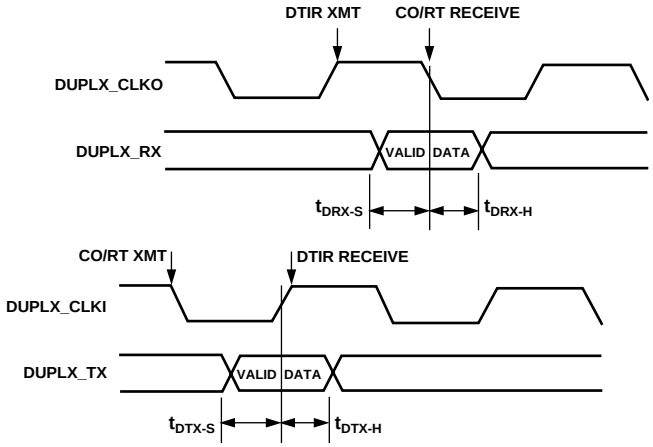


Figure 4. Duplex Serial Port

Table III. TX Serial I/F Timing

Parameter	Description	Typ
t_{DRX-S}	Setup Time of DUPLX_RX from Falling Edge of DUPLX_CLKO	5 ns
t_{DRX-H}	Hold Time of DUPLX_RX from Falling Edge of DUPLX_CLKO	5 ns
t_{DTX-S}	Setup Time of DUPLX_TX from Rising Edge of DUPLX_CLKI	5 ns
t_{DTX-H}	Hold Time of DUPLX_TX from Rising Edge of DUPLX_CLKI	5 ns

INTERLEAVE RAM INTERFACE

The DTIR (DIA) Interfaces an external 32k × 8 Interleave RAM. The interleave RAM interface consists of M_A(14:0), M_D(7:0), NM_WE, and NM_OE. When operating at 3.3 V RAM must have access time less than 50 ns. For further information concerning the operation of the RAM access, consult the DIA specification.

DME INTERFACE TIMING

All signals transmitted by the DME to the DTIR are transmitted on the rising edge and sampled on the falling edge except for the TX_DREQ signal that is transmitted by the DME on the falling edge and sampled by the DTIR on the rising edge. All output signals from the DTIR to the DME are transmitted by the DTIR on the rising edge and received by the DME on the rising edge.

Parameter	Description	Typ	Units
TX Serial I/F Timing			
t_{TFRM-S}	Setup Time of TX_FRM from Falling Edge of TX_RX_SCLK	5	ns
t_{TFRM-H}	Hold Time of TX_FRM from Falling Edge of TX_RX_SCLK	15	ns
$t_{TDREQ-S}$	Setup Time of TX_DREQ from Rising Edge of TX_RX_SCLK	5	ns
$t_{TDREQ-H}$	Hold Time of TX_DREQ from Rising Edge of TX_RX_SCLK	15	ns
t_{TBS-S}	Setup Time of TX_BS from Rising Edge of TX_RX_SCLK	10	ns
t_{TBS-H}	Hold Time of TX_BS from Rising Edge of TX_RX_SCLK	0	ns
t_{TD_S}	Setup Time of TX_SDATA from Rising Edge of TX_RX_SCLK	5	ns
t_{TD_H}	Hold Time of TX_SDATA from Rising Edge of TX_RX_SCLK	0	ns

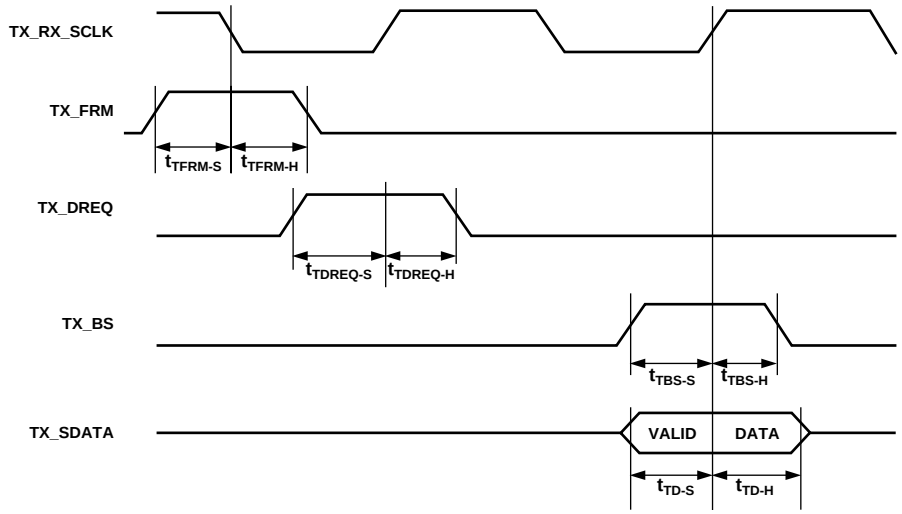


Figure 5. TX Serial I/F Timing

Parameter	Description	Typ	Units
RX Serial I/F Timing			
t_{RFRM-S}	Setup Time of RX_FRM from Falling Edge of TX_RX_SCLK	5	ns
t_{RFRM-H}	Hold Time of RX_FRM from Falling Edge of TX_RX_SCLK	15	ns
$t_{RDREQ-S}$	Setup Time of RX_DREQ from Rising Edge of TX_RX_SCLK	5	ns
$t_{RDREQ-H}$	Hold Time of RX_DREQ from Rising Edge of TX_RX_SCLK	0	ns
t_{RBS-S}	Setup Time of RX_BS from Falling Edge of TX_RX_SCLK	5	ns
t_{RBS-H}	Hold Time of RX_BS from Falling Edge of TX_RX_SCLK	15	ns
t_{RD-S}	Setup Time of RX_SDATA from Falling Edge of TX_RX_SCLK	5	ns
t_{RD-H}	Hold Time of RX_SDATA from Falling Edge of TX_RX_SCLK	15	ns

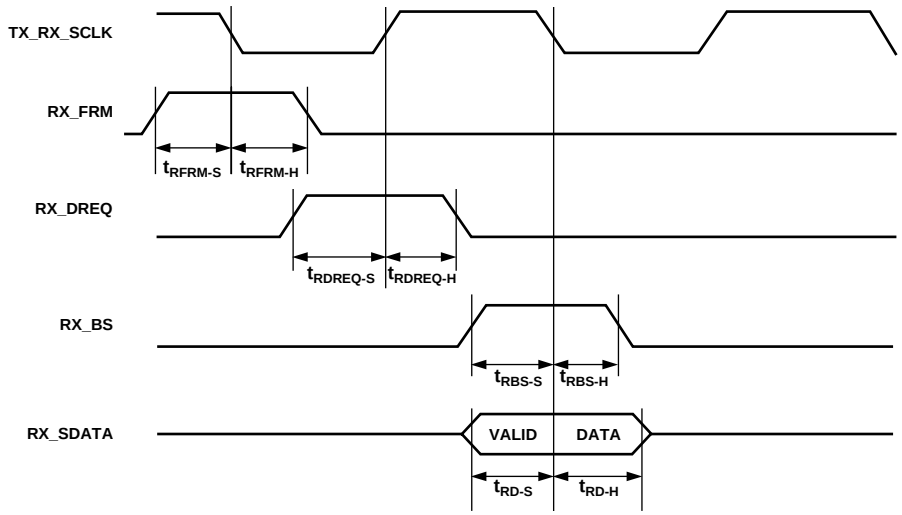


Figure 6. RX Serial I/F Timing

TX Serial Port
The TX serial interface between the DME and DTIR uses five (5) signals:

TX_RX_SCLK:	Serial clock provided by DME.
TX_DREQ:	Data request provided by DME.
TX_FRM:	Frame strobe provided by DME.
TX_BS:	Byte strobe provided by DTIR.
TX_SDATA:	Serial data provided by DTIR.

RX Serial Interface
The RX serial interface between the DME and DTIR uses five (5) signals:

TX_RX_SCLK:	Serial clock provided by DME.
RX_FRMRX_FRM:	Frame strobe provided by DME.
RX_BS:	Byte strobe provided by DME.
RX_SDATA:	Serial data provided by DME.
RX_DREQ:	Data request provided by DTIR.

DSP PORT
The DSP port consists of a 14-bit address bus, A[13:0], a 16-bit data bus, D[15:0], DSP_CLK and three bus control pins, NRD, NWR, NCS.

Parameter		Min	Max	Unit
Read Operation				
Timing Requirements:				
t_{RDD}	NRD Low to Data Valid		8	ns
t_{AA}	A0–A13, NCS to Data Valid		14	ns
t_{RDH}	Data Hold from NRD High	0		ns
Switching Characteristics:				
t_{RP}	NRD Pulsewidth	12		ns
t_{CRD}	DSP_CLK High to NRD Low	3	16	ns
t_{ASR}	A0–A13, NCS Setup before NRD Low	2		ns
t_{RDA}	A0–A13, NCS Hold after NRD Deasserted	5		ns
t_{RWR}	NRD High to NRD or NWR Low	12		ns

NOTE:
DSP clock 28 MHz (35.7 ns)

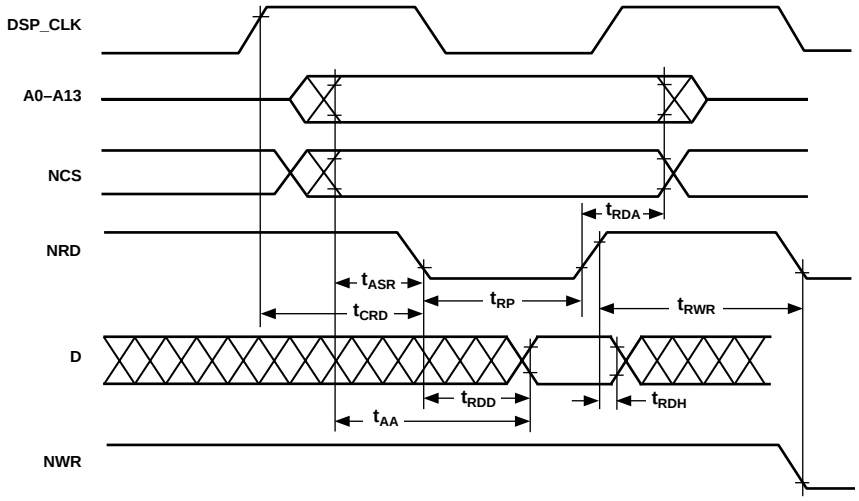


Figure 7. Read Operation

Parameter		Min	Max	Unit
Write Operation				
Switching Characteristics:				
t_{DW}	Data Setup before NWR High	10		ns
t_{DH}	Data Hold after NWR High	6		ns
t_{WP}	NWR Pulsewidth	12		ns
t_{WDE}	NWR Low to Data Enabled	0		ns
t_{ASW}	A0–A13, NCS Setup before NWR Low	2		ns
t_{DDR}	Data Disable before NWR or NRD Low	1		ns
t_{CWR}	DSP_CLK High to NWR Low	3	16	ns
t_{AW}	A0–A13, NCS, Setup before NWR Deasserted	17		ns
t_{WRA}	A0–A13, NCS Hold after NWR Deasserted	5		ns
t_{WWR}	NWR High to NRD or NWR Low	12		ns

NOTE:
DSP clock 28 MHz (35.7 ns)

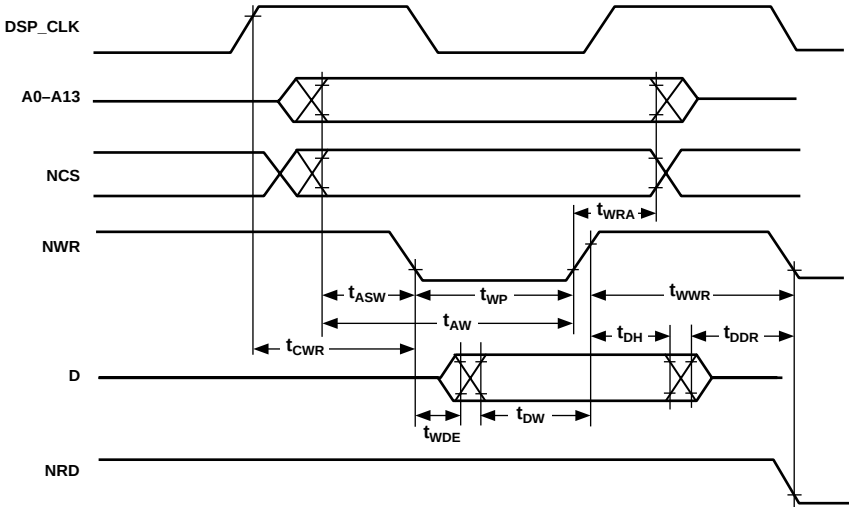
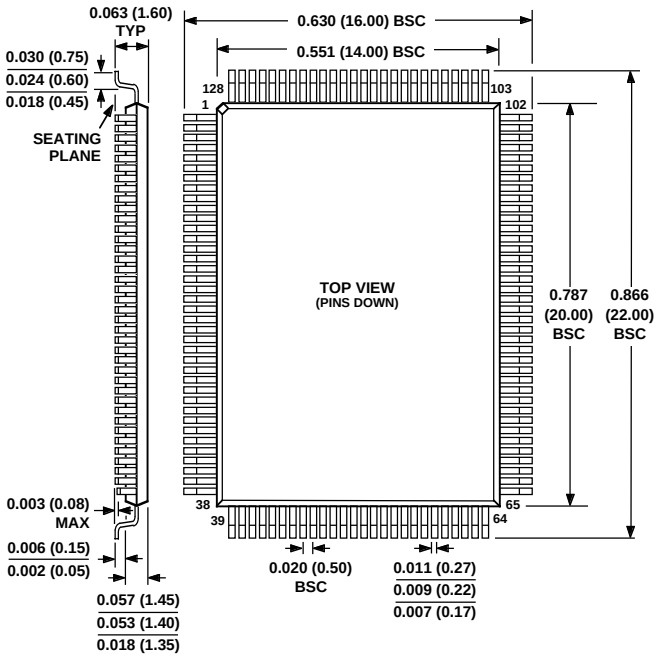


Figure 8. Write Operation

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead Plastic Thin Quad Flatpack
(ST-128)



C3227–3–10/97

PRINTED IN U.S.A.