

FEATURES

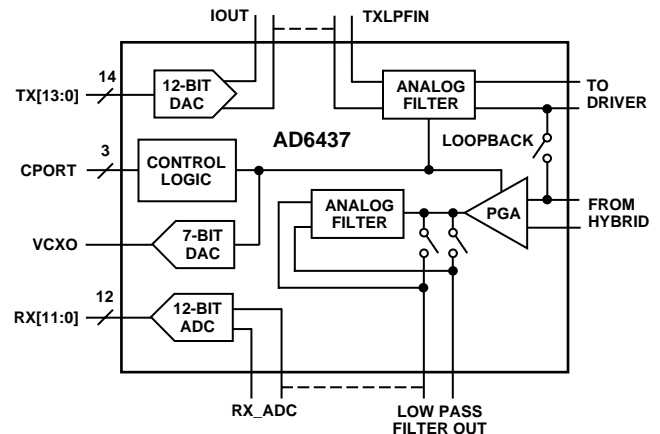
Complete Analog Front End for ADSL Modems
 Part of ADI ADSL Chipset (AD20msp910)
 Designed to ANSI T1.413/ETSI TR238/ITU G.adsl
 Performance
 e.g., 6.1 Mbps Downstream Over 12K Ft.
 Suitable for CO or Residence (ATU-C and ATU-R)
 Includes Transmit and Receive Signal Paths:
 DAC: 20 MSPS 12-Bit Current Output
 ADC: 10 MSPS 12-Bit
 PGA: 0 dB–25 dB of Gain with 1 dB Steps
 Programmable Filters
 Auxiliary DAC for Timing Recovery
 Interface to 3.3 V or 5 V Digital Logic
 Low Power Consumption (485 mW)
 80-Lead PQFP
 –40°C to +85°C Operation

GENERAL DESCRIPTION

The AD6437 is a complete analog front-end IC (AD6437) for ADSL systems. Although part of the Analog Devices DMT chipset, it is suitable for use with digital implementations from other suppliers.

As part of the AD20msp910 chipset, it complements the AD6435, the AD6436 and ADSP-2183; together with the AD816 driver and an external filter, they make a complete ADSL datapump, designed to comply with ANSI and ETSI standards for DMT-based ADSL.

FUNCTIONAL BLOCK DIAGRAM



The AD6437 includes both transmit and receive paths. These include the DAC (up to 20 MSPS, allowing for oversampling of the downstream transmit signal), ADC (up to 10 MSPS), low noise PGA and filters. The filters are software configurable for both the CO and RT modes. There is an auxiliary 7-bit auxiliary DAC (e.g., for timing recovery).

The AD6437 has been designed to be versatile, and most blocks can be used or externally bypassed.

REV. 0

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AD6437–SPECIFICATIONS

| Parameter | Min | Typ | Max | Units | Notes |
|-------------------------------|-----|------------|-----|------------------------|--|
| TRANSMIT CHANNEL | | | | | |
| SNR | | 70 | | dB | 400 kHz Test Tone, First Five Harmonics |
| THD | | 72 | | dB | |
| DAC | | | | | |
| Resolution | | 12 | | Bits | Guaranteed by Design Straight Binary |
| Sample Rate | | | 20 | MSPS | |
| Data Format | | | | | |
| Output Compliance Range | | 2.0 | | V ppd | |
| TRANSMIT FILTER | | | | | 4th Order Butterworth |
| Input Voltage Range | | 2.0 | | V ppd | Ohms Differential Load Impedance 30 k 30 pF |
| Input Impedance | | 10 | | k Ω | |
| Output Voltage Range | | 2.0 | | V ppd | |
| CO Mode | | | | | |
| 3 dB Frequency | | 4 | | MHz | |
| Stopband Rejection @ 16 MHz | | 26 | | dB | |
| Passband | | 1.1 | | MHz | |
| Passband Gain | | ± 0.5 | | dB | |
| RT Mode | | | | | |
| 3 dB Frequency | | 600 | | kHz | |
| Stopband Rejection @ 2.07 MHz | | 25 | | dB | |
| Passband | | 138 | | kHz | |
| Passband Gain | | ± 0.5 | | dB | |
| RECEIVE CHANNEL | | | | | |
| SNR | | 70 | | dB | 400 kHz Test Tone, First Five Harmonics |
| THD | | 72 | | dB | |
| PGA | | | | | 0.5 dB Below f_s Out $\pm 30\%$ Differential 25 dB Gain, 1.2 MHz |
| Gain Range | | 0–30 | | dB | |
| Gain Error | | ± 1 | | dB | |
| Gain Step Error | | ± 0.25 | | dB | |
| Input Resistance | | 500 | | Ω | |
| Input Voltage Range | | 5 | | V ppd | |
| Input Referred Noise | | 12 | | nV/ $\sqrt{\text{Hz}}$ | |
| Output Voltage Range | | 5 | | V ppd | |
| ADC | | | | | |
| Resolution | | 12 | | Bit | |
| Sample Rate | | | 10 | MSPS | Guaranteed by Design Straight Binary |
| Data Format | | | | | |
| Input Voltage | | | 5 | V ppd | |
| | | | | | |
| RECEIVE FILTER | | | | | 4th Order Butterworth |
| 3 dB Frequency | | 4 | | MHz | Passband 0 MHz–1.1 MHz |
| Stopband Rejection @ 16 MHz | | 53 | | dB | |
| Pass Band Gain | | ± 0.5 | | dB | |
| Input Voltage Range | | | 5 | V ppd | |
| Output Voltage Range | | | 5 | V ppd | |
| | | | | | |
| CONTROL | | | | | |
| Timing Recovery DAC | | | | | Monotonic Guaranteed by Design Sink/Source 50 μA max Sink/Source 50 μA max Straight Binary |
| Resolution | 7 | | | Bit | |
| Sample Rate | | | 770 | kHz | |
| Output: Low | | 0.5 | | V | |
| Output: High | | 4.5 | | V | |
| Data Format | | | | | |

| Parameter | Min | Typ | Max | Units | Notes |
|-----------------------------------|------|-----|------|-------|-------------------------|
| DIGITAL INTERFACE | | | | | |
| Input Levels | | | | | 3.3 V or 5 V Compatible |
| Output Levels | | | | | 3.3 V or 5 V Compatible |
| Serial Interface: Clock Rate | | | 10 | MHz | Guaranteed by Design |
| ELECTRICAL | | | | | |
| Analog Power Supply (AVDD) | 4.75 | 5.0 | 5.25 | V | |
| 3 V Digital Power Supply (DVDD_3) | 3.00 | | 3.3 | V | |
| 5 V Digital Power Supply (DVDD_5) | 4.75 | 5.0 | 5.25 | V | |
| IDVDD 5 V | | 13 | | mA | |
| IDVDD 3 V | | 0.1 | | mA | |
| IAVDD | | 84 | | mA | |
| Power Consumption (Normal) | | 485 | 600 | mW | |
| Power Consumption (Low Power) | | 266 | | mW | Reg B Bit 4 Set |

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|---------------------------------------|----------------------------|
| Supply Voltage | -0.3 V to +6.0 V |
| Input Voltage | -0.5 V to $V_{DD} + 0.5$ V |
| Output Voltage Swing | -0.5 V to $V_{DD} + 0.5$ V |
| Operating Temperature Range (Ambient) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (5 sec) PQFP | +280°C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6437 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

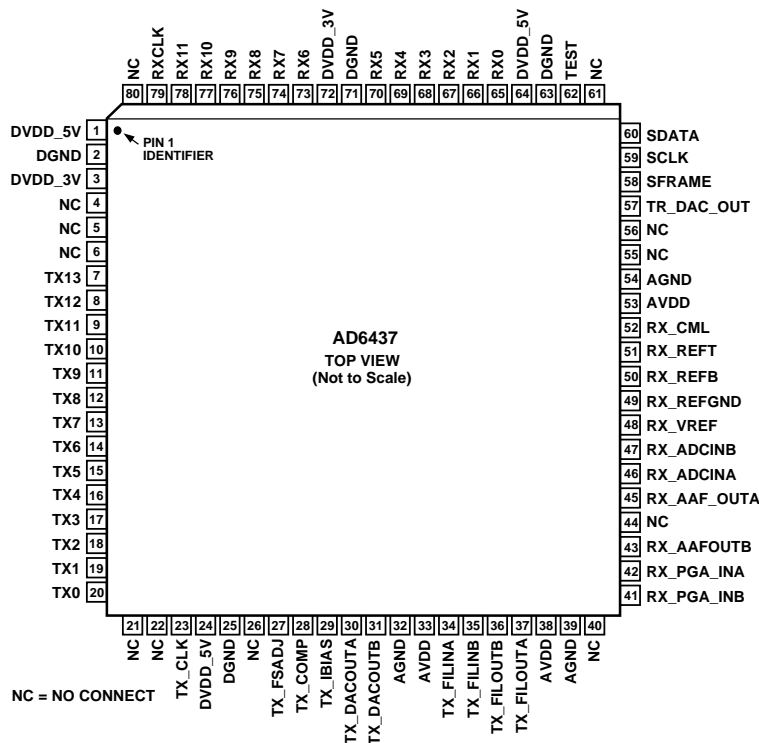
| Model | Temperature Range | Package Description | Package Option |
|--------|-------------------|-----------------------|----------------|
| AD6437 | -40°C to +85°C | Plastic Quad Flatpack | S-80A |



PIN FUNCTION DESCRIPTIONS

| Pin Number | Pin Name | Description |
|---|-------------------|---|
| 1, 24, 64 | DVDD_5 V | +5 V Digital Supply for Converters. Must be connected to 5 V. |
| 2, 25, 63, 71 | DGND | Digital Ground. |
| 3, 72 | DVDD_3 V | Digital Supply for Interface. Can be connected to 3.3 V or 5 V to suit different digital circuitry. |
| 4-6, 21, 22, 26, 40, 44, 55, 56, 61, 80 | NC | No Connect. |
| 7-20 | TX[13:0] | Digital Transmit Data to DAC. |
| 23 | TX_CLK | DAC Clock Input Data Latched on Positive Edge. |
| 27 | TX_FSADJ | Resistor to AGND from this pin sets the full-scale transmit DAC current output. |
| 28, 29 | TX_COMP, TX_IBIAS | Decoupling Pins for Internal Nodes. |
| 30, 31 | TX_DACOUT[A, B] | Complementary Current Outputs. |
| 32, 39, 54 | AGND | Analog Ground. |
| 33, 38, 53 | AVDD | +5 V Analog Supply. |
| 34, 35 | TX_FILIN[A, B] | Differential Input to Transmit LPF. |
| 36, 37 | TX_FILOUT[B, A] | Differential Output from Transmit LPF. |
| 41, 42 | RX_PGA_IN[B, A] | Differential Input to PGA. |
| 43, 45 | RX_AAF_OUT[B, A] | Differential Output of Antialias Filter. |
| 46, 47 | RX_ADC_IN[A, B] | Differential Input to ADC. |
| 48 | RX_VREF | External Voltage Reference Output. |
| 49 | RX_REFGND | External Voltage Reference Ground. |
| 50, 51 | RX_REFB, RX_REFT | Decoupling Pins for ADC Reference Voltage. |
| 52 | RX_CML | Common-Mode Level. Nominally half the supply voltage. |
| 57 | TR_DAC_OUT | Voltage Output from Timing Recovery DAC. |
| 58 | SFRAME | Frame Sync for Timing Recovery DAC Data. |
| 59 | SCLK | Clock for Timing Recovery DAC Serial Data. |
| 60 | SDATA | Serial Data Input to Timing Recovery DAC. |
| 62 | TEST | Factory Test |
| 65-70, 73-78 | RX[0:11] | Digital Output (Receive) Data from ADC. |
| 79 | RX_CLK | ADC Clock Input Sampled on Positive Edge. |

PIN CONFIGURATION



CIRCUIT DESCRIPTION

GENERAL

The AD6437 is designed as the analog front end for the AD20msp910 chipset or other ADSL systems. The AD6437 contains programmable filters that make it suitable for both ATU-C and ATU-R modem applications. Many of the internal circuit of the AD6437 can be programmed or bypassed, making it a versatile CODEC that can be used in other ADSL applications or instrumentation and control systems.

There are four major sections to the AD6437: the transmit channel, which contains a 12-bit DAC and a fourth order reconstruction filter; the receive channel, which includes a PGA with 30 dB of dynamic range, a fourth order antialiasing filter and a 12-bit, 10 MSPS ADC; auxiliary and support circuitry, which consists of a 7-bit DAC used for timing recovery and analog switches used for bypassing internal blocks and channel loopback; finally, there is the interface and control logic.

The AD6437 core runs from a single 5 V supply. The digital interface circuitry can run from either a 3.3 V or 5 V supply. All the analog input and output signals are processed in a fully differential mode. This affords greater immunity to externally coupled noise as well greater signal swings throughout the signal path.

TRANSMIT CHANNEL

The data is received from the digital section (e.g., the AD6436 DME) in parallel format, and passed to the DAC. The output from this is available externally in complementary voltage (TX_DACOUTA, B). Typically, it will then be connected to TXLPF for the on-chip reconstruction filter (4th order Butterworth active filter). However, this filter can be bypassed if a different filter is required (e.g., to use the AD6437 in a non-standard application).

The filter can be switched between two corner frequencies, for use in CO mode or RT mode. For downstream operation (CO mode), the band ends at 1.1 MHz and the filter's 3 dB corner is set at 4 MHz. For upstream operation (RT mode), it is set to 600 kHz, with flat response (± 0.5 dB guaranteed) up to 138 kHz. The selection is made by the txfsel bit in Control Register D (Bit 0).

DAC Output

The DAC is a 12-bit differential output current DAC. The digital coding is straight binary. When the digital inputs are all 1s, I_{OUTA} is at full scale. The value of the outputs are complementary (i.e.,—when I_{OUTA} is at full scale, the current from I_{OUTB} is zero). The current outputs are nominally set to 20 mA

full-scale. The full-scale output current of the DAC is set through an external resistor. The relationship is:

$$I_{OUT_full-scale} = 40/R_{SET} \text{ Amps}$$

e.g., R_{SET} is 2 k Ω for a 20 mA full-scale output.

The current can be converted to a voltage by a grounded resistor. Ideally, this would be immediately converted to a large signal to preserve SNR. However, the output compliance of the DAC is 1.0 V. The resistors would be chosen to be <49.9 Ω for a 1.0 V output (2 V ppd) to stay within the compliance range.

The power consumption of the AD6437 can be reduced by lowering $I_{OUT_full-scale}$. Lowering the full-scale current does increase the THD of the DAC outputs. Lowering the output current would require the termination resistors to increase by the same ratio to maintain a 2 V ppd output signal. This, however, will in turn raise the source impedance.

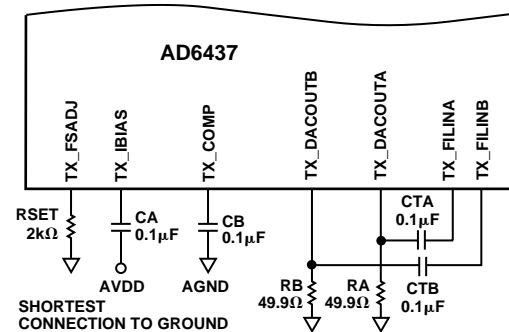


Figure 1. Typical Configuration: Transmit Path

Tx LPF

The AD6437 Tx low-pass filter is designed to attenuate the images created at the DAC output due to the sampling process. The amount of attenuation required is specified in the ANSI T1.413 specification in Sections 6.12 and 7.12 for the ATU-C and ATU-R respectively. The AD6437 filter is designed to meet or exceed these requirements.

The AD6437 Tx LPF is implemented as a fully differential 4th order Butterworth filter. The input voltage range is 2 V ppd, centered about 2.5 volts. The input impedance is approximately 10 k Ω differential. The passband gain of the filter is unity. The THD of the filter is typically less than -75 dB when driving a 30 k|30 pF load. However, the THD rises as the load impedance is decreased. As a result, the load impedance driven by the filter should be kept as high as possible.

AD6437

RECEIVE CHANNEL

The receive channel consists of the programmable gain amplifier, antialias filter and ADC.

Programmable Gain Amplifier

The input from hybrid and filters is required to drive the PGA input. This is centered at 2.5 V and has a maximum input voltage range of 5 V p-p. The input impedance is low, 500 Ω (differential) ± 30%. This means that the amplifier must be able to drive a low impedance with low THD up to 1.1 MHz. Additionally, the multiple feedback topology requires that the amplifier be voltage feedback. Also, the input referred noise should be as low as possible to preserve the SNR of the channel.

Receive Filters

The antialias filter is set to a 3 dB corner at 4 MHz. If desired, the filter can be bypassed and an external one used instead.

Analog-to-Digital Converter

The analog-to-digital converter operates to 12-bit resolution (11-bit linearity), and is clocked at up to 10 MHz.

The filter capacitors shown in Figure 2 are used to decouple the internal reference voltages of the ADC.

A buffer is required after the filters, at the input to the ADC. This must be able to drive the 30 pF input capacitance of the ADC, with the desired bandwidth and distortion properties. A typical part is the AD8042.

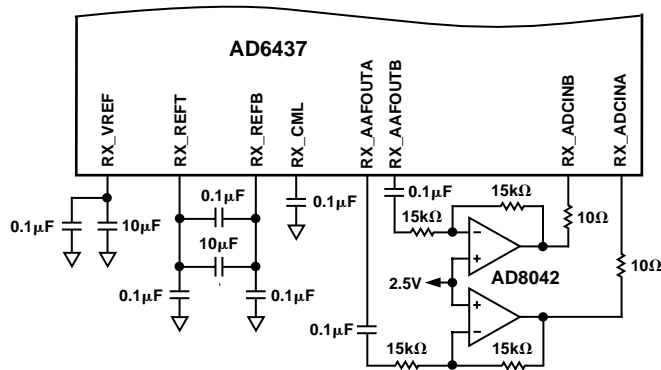


Figure 2. Typical Configuration: Receive Path

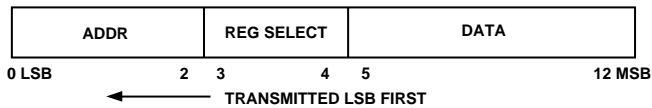


Figure 3. Serial Data Format

Table I. Programmable Gain Amplifier Control

| Pg 5 | Pg 4 | Pg 3 | Pg 2 | Pg 1 | Pg 0 | Relative Gain (dB) |
|------|------|------|------|------|------|--------------------|
| 0 | 0 | x | x | x | x | 0 |
| 0 | 1 | 0 | x | x | x | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 0 | 1 | 1 | 3 |
| 0 | 1 | 1 | 1 | 0 | 0 | 4 |
| 0 | 1 | 1 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 0 | 0 | 0 | 6 |
| 1 | 0 | 0 | 0 | 0 | 1 | 7 |
| 1 | 0 | 0 | 0 | 1 | 0 | 8 |
| 1 | 0 | 0 | 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 1 | 0 | 0 | 10 |
| 1 | 0 | 0 | 1 | 0 | 1 | 11 |
| 1 | 0 | 0 | 1 | 1 | 0 | 12 |
| 1 | 0 | 0 | 1 | 1 | 1 | 12 |
| 1 | 0 | 1 | 0 | 0 | 0 | 12 |
| 1 | 0 | 1 | 0 | 0 | 1 | 13 |
| 1 | 0 | 1 | 0 | 1 | 0 | 14 |
| 1 | 0 | 1 | 0 | 1 | 1 | 15 |
| 1 | 0 | 1 | 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 1 | 0 | 1 | 17 |
| 1 | 0 | 1 | 1 | 1 | 0 | 18 |
| 1 | 0 | 1 | 1 | 1 | 1 | 18 |
| 1 | 1 | 0 | 0 | 0 | 0 | 18 |
| 1 | 1 | 0 | 0 | 0 | 1 | 19 |
| 1 | 1 | 0 | 0 | 1 | 0 | 20 |
| 1 | 1 | 0 | 0 | 1 | 1 | 21 |
| 1 | 1 | 0 | 1 | 0 | 0 | 22 |
| 1 | 1 | 0 | 1 | 0 | 1 | 23 |
| 1 | 1 | 0 | 1 | 1 | 0 | 24 |
| 1 | 1 | 0 | 1 | 1 | 1 | 24 |
| 1 | 1 | 1 | 0 | 0 | 0 | 24 |
| 1 | 1 | 1 | 0 | 0 | 1 | 25 |
| 1 | 1 | 1 | 0 | 1 | 0 | 26 |
| 1 | 1 | 1 | 0 | 1 | 1 | 27 |
| 1 | 1 | 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 1 | 30 |

ANCILLARY AND SUPPORT SECTION**Auxiliary D/A**

There is a 7-bit monotonic DAC, with an output buffer, that can be used for system control. Typically, this will be used for timing recovery, to drive a VCXO.

The output buffer load must be greater than 100 k Ω .

DIGITAL INTERFACE TO AD6437

The digital I/O pins can interface to either 3.3 V or 5 V logic. The voltage connected to the DVDD_3 V power pins (Pins 3 and 72) determines the interface voltage. Although the DVDD_3 V pins can be connected to either 3.3 V or 5 V, they must be connected to the same voltage. When interfacing to the other chips in the ADSL system, the AD6437 DVDD_3 V power pins should ideally be connected to 3.3 V; in addition to lower power consumption, this lowers board noise and digital feedthrough into the AD6437 data converters.

DVDD_5 V must always be connected to 5 V.

See the Digital Interface section of the electrical specifications in the AD6437 data sheet for details on minimum and maximum logic levels.

SERIAL INTERFACE

The serial port interface has the ability to interface with most digital systems (e.g., the ADSP-2183 used in the Analog Devices ADSL chipsets).

The interface consists of three signals: SDATA, SCLK and SFRAME (described in Table II and Figure 6). The SDATA and SFRAME are clocked into the DSP Interface block on a falling edge of SCLK. The DSP interface decodes the first three bits of the incoming data word to determine if the AD6437 is being addressed. If the DSP has selected the AD6437, the next 10 bits are accepted. The first two bits decode one of four internal data registers (Reg A, Reg B, Reg C, and Reg D), and the following eight bits used as data to be loaded into that register.

NOTE: The AD6437 registers may not start up in a defined state on power-up. They should be cleared to explicitly set them to a known state before use.

Table II. AD6437 Serial Port I/O

| Pin Name | Definition | Type | Description |
|----------|---------------------|-------|---|
| SDATA | Data Transmit | Input | Data Output from Host Processor (e.g., ADSP-2183) |
| SFRAME | Transmit Frame Sync | Input | Sync Output from Host Processor |
| SCLK | Serial Clock | Input | Clock Output from Host Processor |

Table III. Register Function

| Register | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|--------------|-------|-------|-------|--------|---------|---------|---------|---------|
| REG A | PGA Control | NA | NA | Pg 5 | Pg 4 | Pg 3 | Pg 2 | Pg 1 | Pg 0 |
| REG B | Power Mode | NA | NA | NA | lpchip | pdpgaaa | pdtxfil | pdtrdac | pd12dac |
| REG C | Aux DAC Data | NA | trd6 | trd5 | trd4 | trd3 | trd2 | trd1 | trd0 |
| REG D | Control | test1 | NA | NA | test | NA | alpbk | aafbp | txfsel |

NA = Not Assigned.

Table IV. Register Bit Field Function

| Name | Field | Description |
|----------|----------|---|
| Pg[5:0] | Reg A | Programmable Gain Amplifier Gain Bits. Pg 0 LSB. See Table I. |
| lpchip | Reg B[4] | Low Power Mode. Powers down all chips except ADC. Active High. |
| pdpgaaa | Reg B[3] | Power-Down Receive PGA and AA Filter. Active High. |
| pdtxfil | Reg B[2] | Power-Down Transmit Filters. Active High. |
| pdtrdac | Reg B[1] | Power-Down Timing Recovery DAC. Active High. |
| pd12dac | Reg B[0] | Power-Down 12-Bit DAC. Active High. |
| trd[6:0] | Reg C | Timing Recovery DAC Data; trd0 LSB, Data Format Binary. |
| alpbk | Reg D[2] | Analog Loop Back. Active High. |
| aafbp | Reg D[1] | AA Filter Bypass. Active High. Powers down the filter. |
| txfsel | Reg D[0] | Transmit Filter Select. txfsel = 0, 138 kHz, txfsel = 1, 1 MHz Filter Select. |

Table V. Serial Interface Data Format

| SDATA [2:0] | SDATA [3:4] | SDATA [5:12] |
|--|---|---|
| Determines if AD6437 is selected, Addr 101 is assigned for AD6437. | Selects AD6437 register. SDATA [4 3] 0 0 Reg A 0 1 Reg B 1 0 Reg C 1 1 Reg D | Data byte written (LSB first). SDATA 12, MSB SDATA 5, LSB |

NOTE

Data is transmitted in 13-bit words: SDATA 0, LSB, transmitted first; SDATA 12, MSB, transmitted last.

TIMING

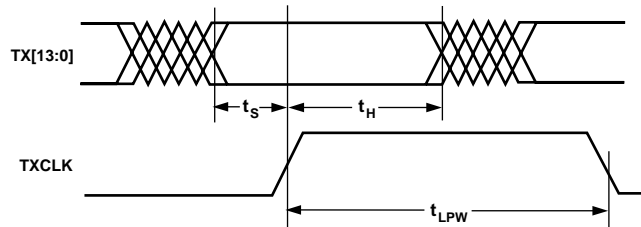


Figure 4. Transmit DAC Data Timing

Table VI. Transmit DAC Timing

| Symbol | Min | Typ | Max | Units |
|-----------|-----|-----|-----|-------|
| t_s | 12 | | | ns |
| t_H | 12 | | | ns |
| t_{LPW} | 16 | | | ns |

RECEIVE INTERFACE

The analog input is sampled every the rising edge of the ADC clock (RX_CLK), with digital data (RX11:RX0) being valid on each falling edge of RX_CLK. Due to the pipeline architecture used in the ADC, there is a three-cycle latency in the receive data as shown in the diagram.

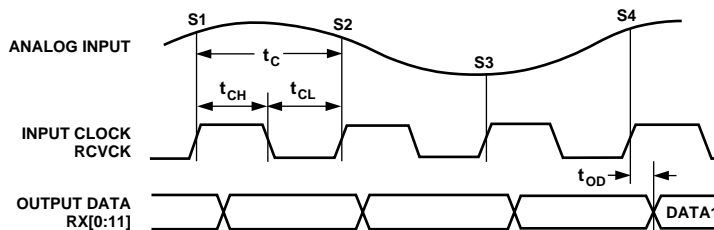


Figure 5. Receive Interface Timing Diagram

Table VII. Receive Switching Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|-----------------------|-----|-----|-----|--------|
| t_c | Clock Period | | 100 | | ns |
| t_{CH} | CLOCK Pulsewidth High | 45 | | | ns |
| t_{CL} | CLOCK Pulsewidth Low | 45 | | | ns |
| t_{OD} | Output Delay | 8 | 13 | 19 | ns |
| Latency | Pipeline Delay | 3 | 3 | 3 | Cycles |

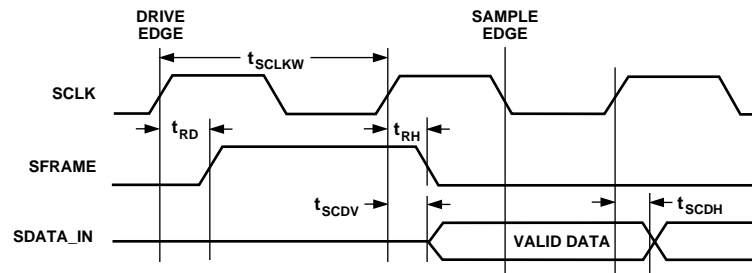


Figure 6. Serial Port Interface Timing

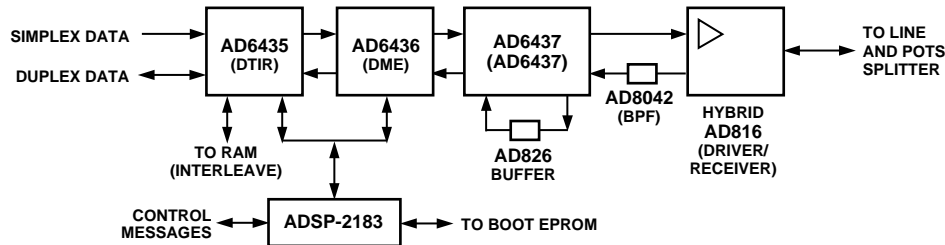


Figure 7. Example System Configuration

Table VIII. Serial Port Interface Timing Parameters

| Symbol | External Clock Switching Characteristics | Typ | Min | Max | Units |
|-------------|--|-----|-----|-----|-------|
| t_{SCLKW} | Clock Period (6.6 MHz) | 151 | | | ns |
| t_{RD} | SFRAME Delay After SCLK | | | 15 | ns |
| t_{RH} | SFRAME Hold After SCLK | | 0 | | ns |
| t_{SCDV} | SCLK High to SDATA Valid (Delayed) | | | 15 | ns |
| t_{SCDH} | Transmit Data Hold After SCLK | | 0 | | ns |

Typical 6.6 MHz synchronous control interface rate.

CONNECTION AND APPLICATION INFORMATION

Decoupling

All the internal bias points of the AD6437 DAC and ADC are decoupled as shown in Figures 2 and 3. All AD6437 power pins should be decoupled with a 10 μ F tantalum capacitor and a parallel 0.1 μ F ceramic chip cap. The 0.1 μ F capacitors should be placed as closely as possible to the device pins. This configuration ensures a low impedance power source over a wide band of frequencies.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**80-Lead Plastic Quad Flatpack (PQFP)
(S-80A)**

