

# Quad SPST CMOS Analog Switch with Latches

## Features

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Built on PLUS-40 Process
- Latches Are Transparent with  $\overline{WR}$  Low
- Low On-Resistance: 60  $\Omega$

## Benefits

- Compatible with Most  $\mu$ P Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

## Applications

- $\mu$ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

## Description

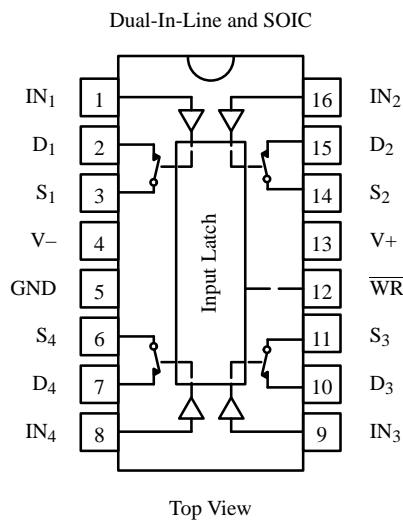
The DG221 is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common  $\overline{WR}$  pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix PLUS-40 CMOS process, the

DG221 combines low power and low on-resistance (60  $\Omega$  typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition. These switches guarantee a rail-to-rail blocking capability (44 V max), in the off condition.

## Functional Block Diagram and Pin Configuration



Four Latchable SPST Switches per Package

**Truth Table**

IN <sub>X</sub>	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X		Control data latched-in, switches on or off as selected by last IN <sub>X</sub>
X	1	Maintains previous state

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V

**Ordering Information**

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG221CJ
-40°C to 85°C	16-Pin Narrow SOIC	DG221DY
-55°C to 125°C	16-Pin CerDIP	DG221AK/883

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70041.

## Absolute Maximum Ratings

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed 1 ms, 10% duty cycle)	70 mA
Storage Temperature:	(AK Suffix) -65 to 150°C
	(CJ and DY Suffix) -65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin CerDIP <sup>c</sup>	900 mW
16-Pin Plastic DIP <sup>d</sup>	470 mW
16-Pin SOIC <sup>e</sup>	600 mW

Notes:

- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 12 mW/°C above 75°C
- d. Derate 6.5 mW/°C above 25°C
- e. Derate 7.7 mW/°C above 75°C

## Schematic Diagram (Typical Channel)

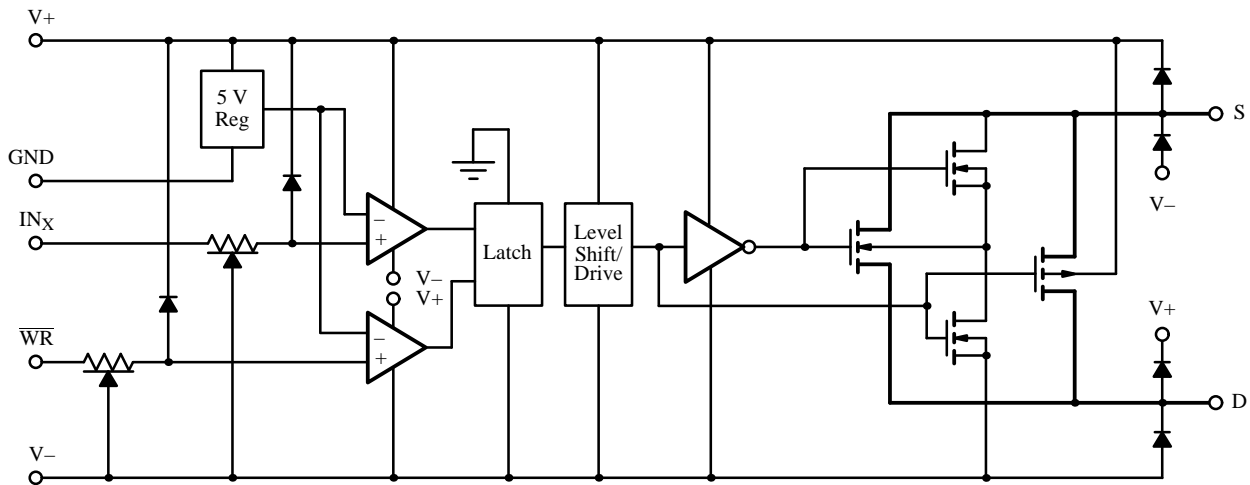


Figure 1.

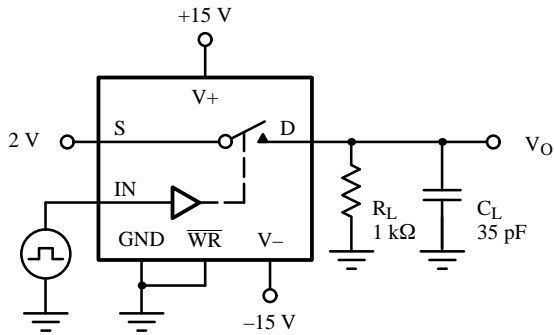
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>IN</sub> = 2.4 V, 0.8 <sup>f</sup> V, $\overline{WR}$ = 0	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ± 10 V	Room Full	60		90 135		90 135	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ± 14 V, V <sub>D</sub> = ∓ 14 V	Room Full	± 0.01	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>		Room Full	± 0.02	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ± 14 V	Room Full	± 0.01	-1 -200	1 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current	I <sub>INL</sub> , I <sub>INH</sub>	V <sub>IN</sub> = 0 V or = 2.4 V	Room Full	-0.0004	-1 -10	1 10	-1 -10	1 10	μA
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	See Figure 2	Room			550		550	ns
Turn-Off Time	t <sub>OFF</sub>		Room			340		340	
Turn-On Time Write	t <sub>ON</sub> , $\overline{WR}$	See Figure 3	Room			550		550	
Turn-Off Time Write	t <sub>OFF</sub> , $\overline{WR}$		Room			340		340	
Write Pulse Width	t <sub>W</sub>	See Figure 4	Room	120	150		150		
Input Setup Time	t <sub>S</sub>		Room	130	180		180		
Input Hold Time	t <sub>H</sub>		Full	0	20		20		
Charge Injection	Q	C <sub>L</sub> = 1000 pF V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room	20					pC
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz, V <sub>S</sub> , V <sub>D</sub> = 0 V	Room	8					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	9					
Channel-On Capacitance	C <sub>D(on)</sub>		Room	29					
Off Isolation	OIRR	V <sub>S</sub> = 1 V <sub>p-p</sub> , f = 100 kHz C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	Room	70					dB
Interchannel Crosstalk	X <sub>TALK</sub>		Room	90					
<b>Power Supplies</b>									
Positive Supply Current	I <sub>+</sub>	All Channels On or Off V <sub>IN</sub> = 0 V or 2.4 V	Full	0.8		1.5		1.5	mA
Negative Supply Current	I <sub>-</sub>		Room	-0.4	-1		-1		

Notes:

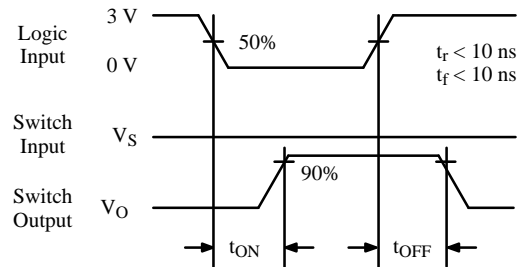
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

## Test Circuits

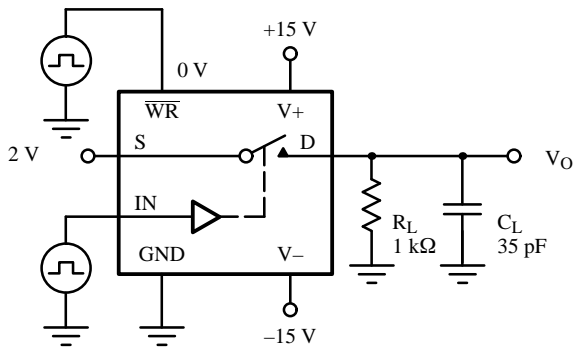


$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

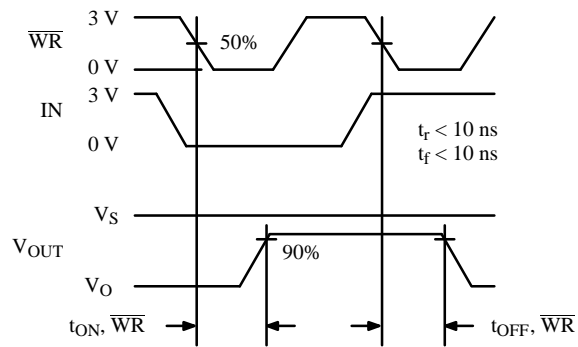


**Figure 2.** Switching Time

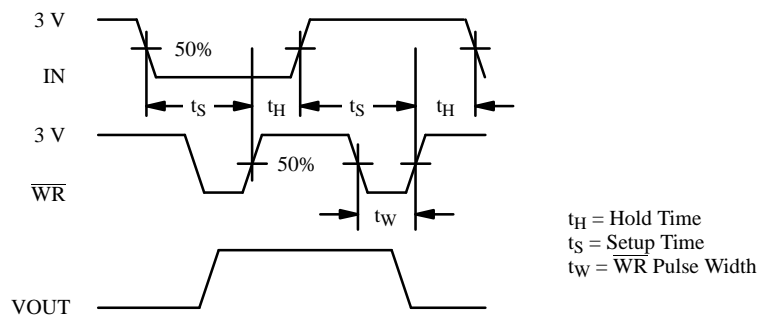


$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



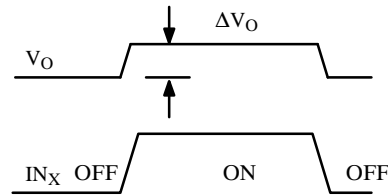
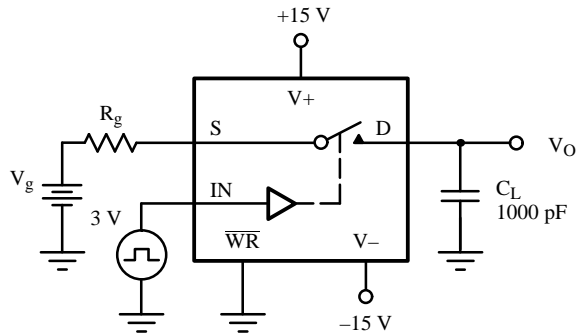
**Figure 3.**  $\overline{WR}$  Switching Time



The latches are level sensitive. When  $\overline{WR}$  is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of  $\overline{WR}$ .

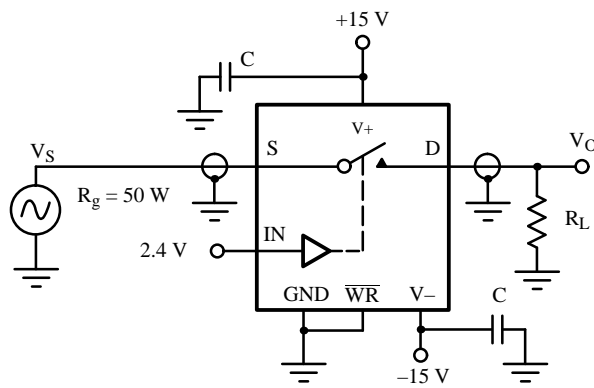
**Figure 4.**  $\overline{WR}$  Setup Conditions

## Test Circuits (Cont'd)



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

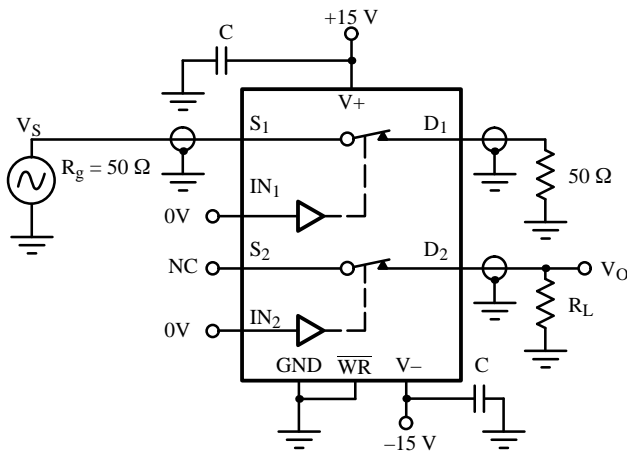
Figure 5. Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 6. Off Isolation



$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 7. Channel-to-Channel Crosstalk

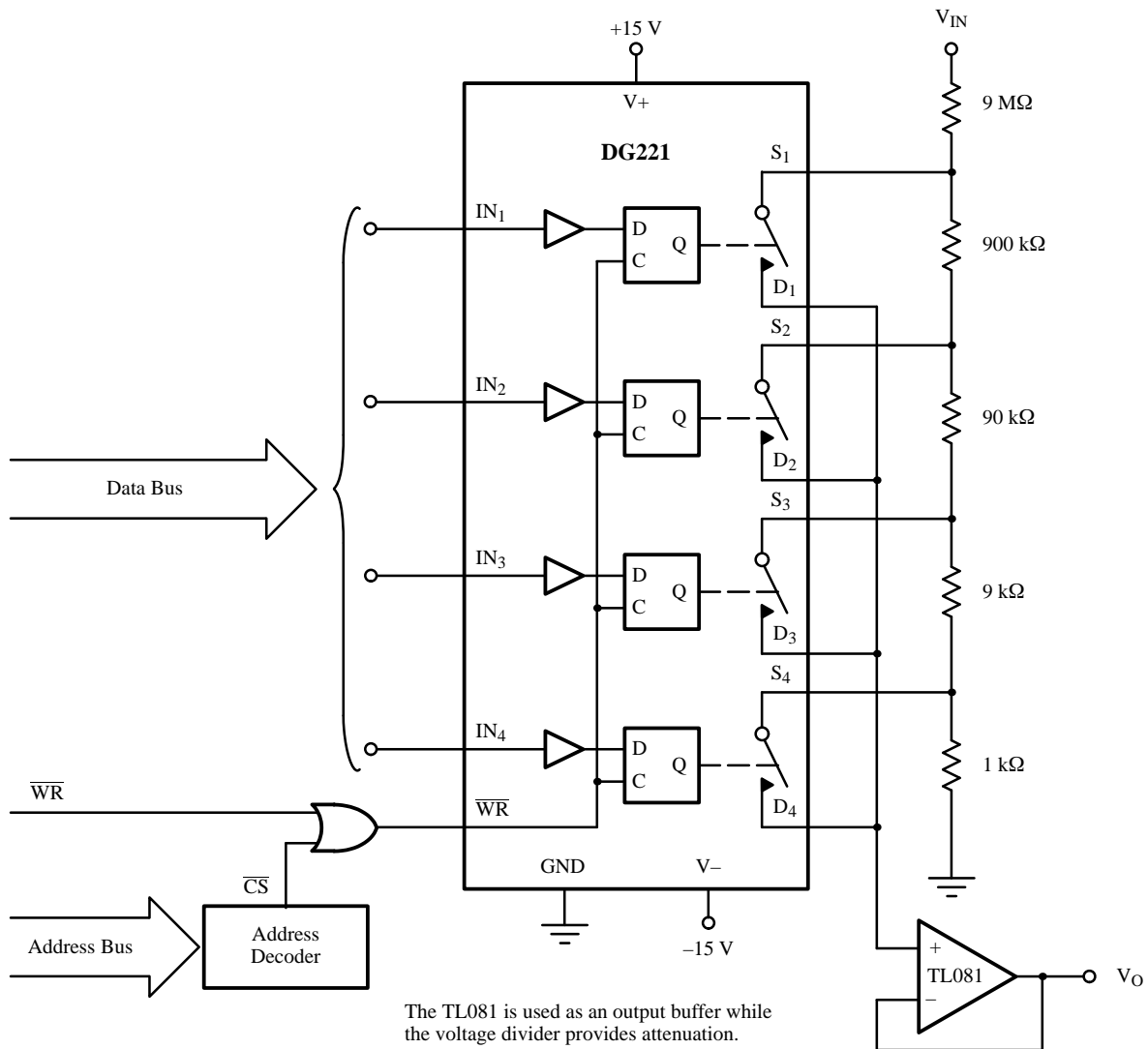
## Application Hints<sup>a</sup>

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND (V)	$\overline{\text{WR}}$ (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	0	2.4/0.8	2.4/0.8	-15 to 15
20	-20	0	2.4/0.8	2.4/0.8	-20 to 20
10	-10	0	2.4/0.8	2.4/0.8	-10 to 10
10	-5	0	2.4/0.8	2.4/0.8	-5 to 10

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

## Applications



**Figure 8.**  $\mu$ P-Controlled Analog Signal Attenuator

**Truth Table**

IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	$\overline{WR}^a$	On Switch
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

**Output Attenuation for Figure 8**

WR	IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

**Notes:**

a.  $\overline{WR}$  may be held at "0" for temporary operation similar to DG201A/DG201B. With  $\overline{WR}$  at "0" SW<sub>1</sub> will remain on as long as IN<sub>1</sub> is held at "0".