µP-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The device provides virtually any frequency translation combination across this operating range. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I^{2}C or SPI interface. The Si5325 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5325 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Optical modules
- Wireless basestations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

Features

- Generates any frequency from 10 to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (30 kHz–1.3 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 2 MHz)
- Dual clock inputs w/manual or automatically controlled switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- LOS, FOS alarm outputs
- Digitally-controlled output phase adjust
- I^{2}C or SPI programmable
- On-chip voltage regulator for 1.8 ±5%, 2.5 or 3.3 V ±10% operation
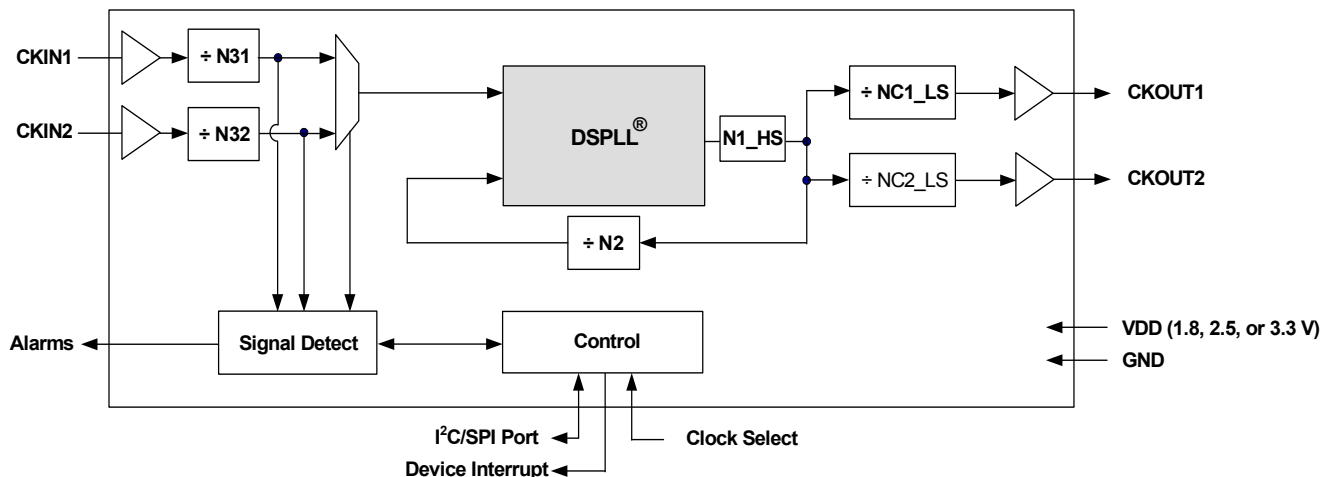- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Table 1. Performance Specifications

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.89	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz Both CKOUTs enabled LVPECL format output	—	251	279	mA
		CKOUT2 disabled	—	217	243	mA
		f_{OUT} = 19.44 MHz Both CKOUTs enabled CMOS format output	—	204	234	mA
		CKOUT2 disabled	—	194	220	mA
		Tristate/Sleep Mode	—	165	TBD	mA
Input Clock Frequency (CKIN1, CKIN2)	CK_F	Input frequency and clock multiplication ratio determined by programming device PLL dividers. Consult Silicon Laboratories configuration software DSPLL-*sim* at www.silabs.com/timing (click on Documentation) to determine PLL divider settings for a given input frequency/clock multiplication ratio combination.	10	—	710	MHz
Output Clock Frequency (CKOUT1, CKOUT2)	CK_{OF}		10 970 1213	— — —	945 1134 1400	MHz
Input Clocks (CKIN1, CKIN2)						
Differential Voltage Swing	CKN_{DPP}		0.25	—	1.9	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Rise/Fall Time	CKN_{TRF}	20–80%		—	11	ns
Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller	40	—	60	%
			2	—	—	ns
Output Clocks (CKOUT1, CKOUT2)						
Common Mode	V_{OCM}	LVPECL	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}	100 Ω load	1.1	—	1.9	V
Single Ended Output Swing	V_{SE}	line-to-line	0.5	—	0.93	V
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps
Duty Cycle Uncertainty	CKO_{DC}	LVPECL Differential 100 Ω Line-to-Line Measured at 50% point	–40	—	40	ps
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation).						

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Table 1. Performance Specifications (Continued)

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance						
Jitter Generation	J_{GEN}	f_{IN} = f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.6	TBD	ps rms
		12 kHz–20 MHz	—	0.6	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
Phase Noise	CKO_{PN}	f_{IN} = f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n $\geq$ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	ºC/W
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation).						

Table 2. Absolute Maximum Ratings

| Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.6	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		200	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		700	V
ESD MM Tolerance; CKIN+/CKIN–		150	V
Latch-Up Tolerance		JESD78 Compliant	
Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.			

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622 MHz In, 622 MHz Out BW=877 kHz
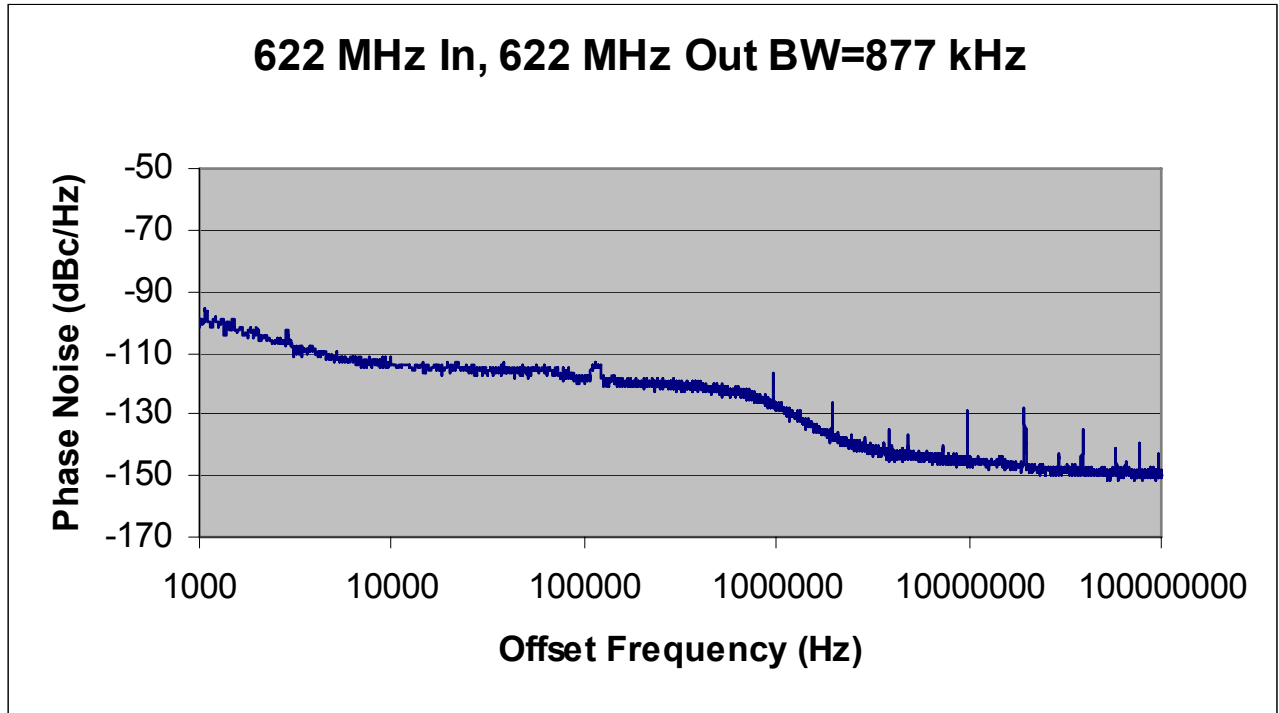
Figure 1. Typical Phase Noise Plot

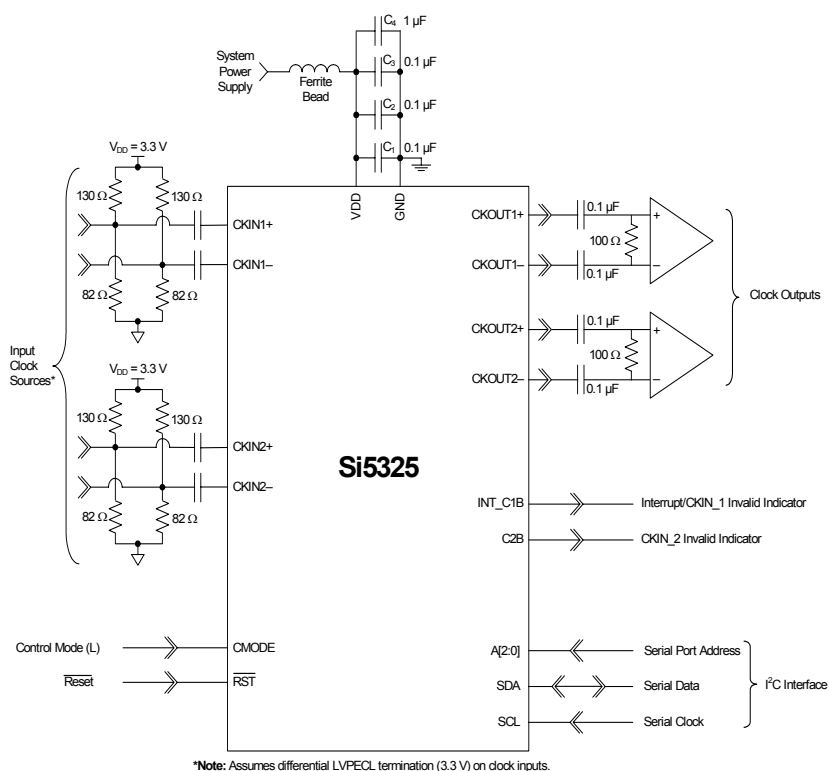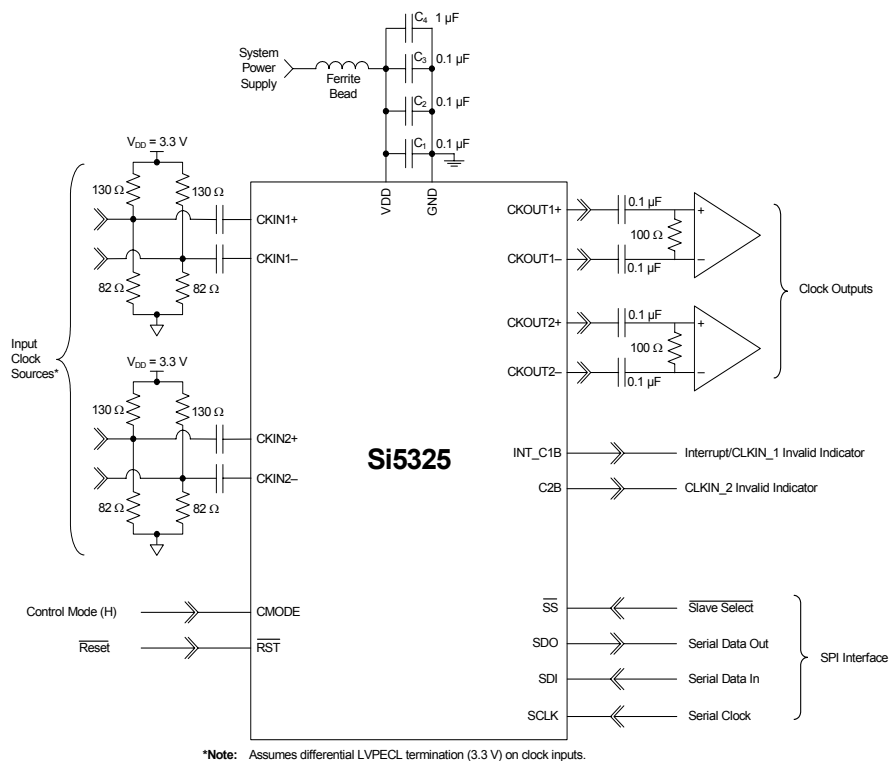| Jitter Bandwidth	RMS Jitter (fs)
OC-48, 12 kHz to 20 MHz	374
OC-192, 20 kHz to 80 MHz	388
OC-192, 4 MHz to 80 MHz	181
OC-192, 50 kHz to 80 MHz	377
Broadband, 800 Hz to 80 MHz	420

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Figure 2. Si5325 Typical Application Circuit (I²C Control Mode)

Figure 3. Si5325 Typical Application Circuit (SPI Control Mode)

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1. Functional Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two synchronous clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for each input clock and output clock, so the Si5325 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5325 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5325 PLL loop bandwidth is digitally programmable and supports a range from 30 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5325 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for detailed information about the Si5325. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

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2. Pin Descriptions: Si5325
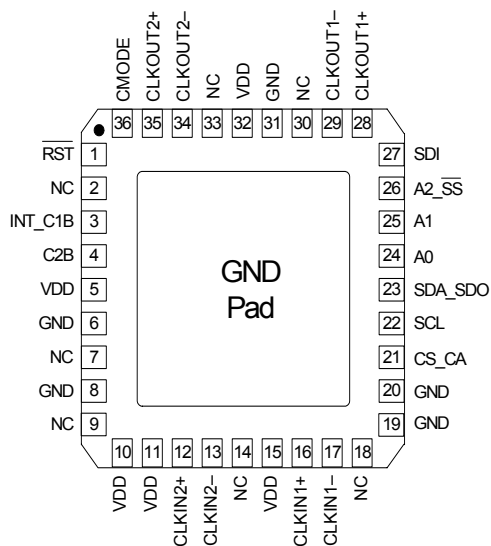
Pin numbers are preliminary and subject to change.

Table 3. Si5325 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	RST	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up.
2, 7, 9, 14, 18, 30, 33	NC	—	—	**No Connect.** This pin must be left unconnected for normal operation.
3	INT_C1B	O	LVCMOS	**Interrupt/CKIN1 Invalid Indicator.** This pin functions as a device interrupt output or an alarm output for CKIN1. If used as an interrupt output, *INT_PIN* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit. If used as an alarm output, the pin functions as a LOS (and optionally FOS) alarm indicator for CKIN1. Set *CK1_BAD_PIN* = 1 and *INT_PIN* = 0. 0 = CKIN1 present. 1 = LOS (FOS) on CKIN1. The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates.
Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5325 Register Map.				

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Table 3. Si5325 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
4	C2B	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin functions as a LOS (and optionally FOS) alarm indicator for CKIN2 if _CK2_BAD_PIN_ = 1. 0 = CKIN2 present. 1 = LOS (FOS) on CKIN2. The active polarity can be changed by _CK_BAD_POL_. If _CK2_BAD_PIN_ = 0, the pin tristates.
5, 10, 11, 15, 32	V$_{DD}$	V$_{DD}$	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following Vdd pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to device as is practical.
6, 8, 19, 20 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.
21	CS_CA	I/O	LVCMOS	**Input Clock Select/Active Clock Indicator.** **Input**: In manual clock selection mode, this pin functions as the manual input clock selector if the _CKSEL_PIN_ is set to 1. 0 = Select CKIN1. 1 = Select CKIN2. If _CKSEL_PIN_ = 0, the _CKSEL_REG_ register bit controls this function. If configured as input, must be set high or low. **Output**: In automatic clock selection mode, this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both clocks, CA will indicate the last active clock that was used before entering the digital hold state. The _CK_ACTV_PIN_ register bit must be set to 1 to reflect the active clock status to the CA output pin. 0 = CKIN1 active input clock. 1 = CKIN2 active input clock. If _CK_ACTV_PIN_ = 0, this pin will tristate. The CA status will always be reflected in the _CK_ACTV_REG_ read only register bit.
Note: Internal register names are indicated by underlined italics, e.g. _INT_PIN_. See Si5325 Register Map.					

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Table 3. Si5325 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
22	SCL	I	LVCMOS	**Serial Clock/Serial Clock.** This pin functions as the serial clock input for both SPI and I^{2}C modes. This pin has a weak pulldown.
23	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^{2}C control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI control mode (CMODE = 1), this pin functions as the serial data output.
25 24	A1 A0	I	LVCMOS	**Serial Port Address.** In I^{2}C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I^{2}C address is 1101 [A2] [A1] [A0]. In SPI control mode (CMODE = 1), these pins are ignored. This pin has a weak pulldown.
26	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/Slave Select.** In I^{2}C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pulldown.
27	SDI	I	LVCMOS	**Serial Data In.** In I^{2}C control mode (CMODE = 0), this pin is ignored. In SPI control mode (CMODE = 1), this pin functions as the serial data input. This pin has a weak pulldown.
29 28	CKOUT1– CKOUT1+	O	Multi	**Output Clock 1.** Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
34 35	CKOUT2– CKOUT2+	O	Multi	**Output Clock 2.** Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT2_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
36	CMODE	I	LVCMOS	**Control Mode.** Selects I^{2}C or SPI control mode for the Si5325. 0 = I^{2}C Control Mode. 1 = SPI Control Mode. Must not float.
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.
Note: Internal register names are indicated by underlined italics, e.g. *INT_PIN*. See Si5325 Register Map.				

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3. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5325A-C-GM	10–945 MHz 970–1134 MHz 1.213–1.417 GHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5325B-C-GM	10–808 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5325C-C-GM	10–346 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C

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4. Package Outline: 36-Pin QFN

Figure 4 illustrates the package details for the Si5325. Table 4 lists the values for the dimensions shown in the illustration.
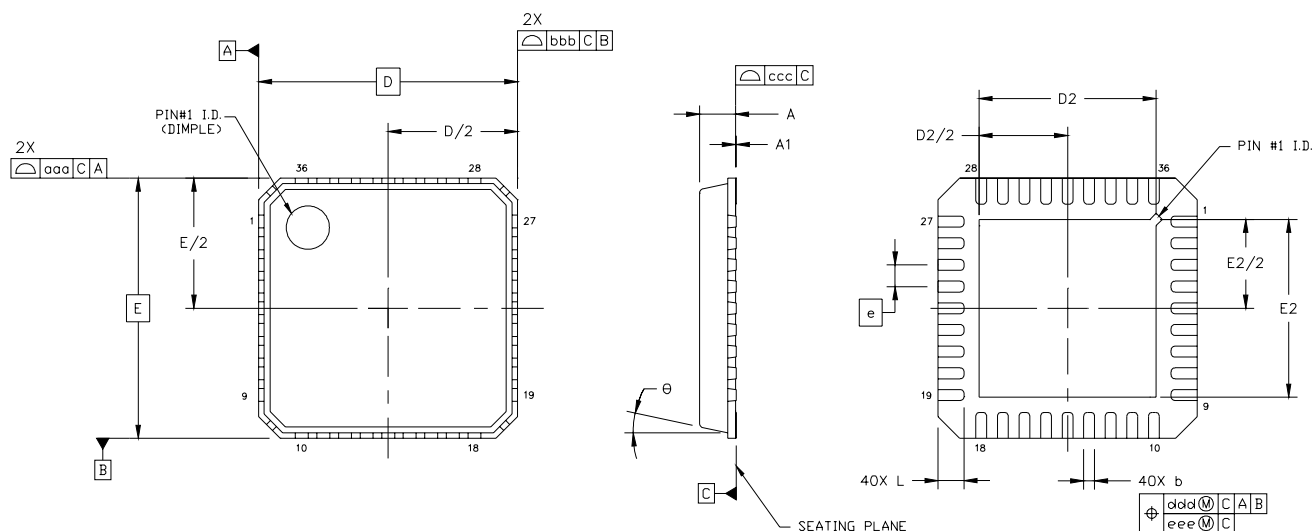
Figure 4. 36-Pin Quad Flat No-lead (QFN)

Table 4. Package Dimensions

Symbol	Millimeters		
	Min	**Nom**	**Max**
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	6.00 BSC		
D2	3.95	4.10	4.25
e	0.50 BSC		
E	6.00 BSC		
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	**Nom**	**Max**
L	0.50	0.60	0.70
θ	—	—	12°
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:
   1. All dimensions shown are in millimeters (mm) unless otherwise noted.
   2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
   3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
   4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Si5325

5. Recommended PCB Layout
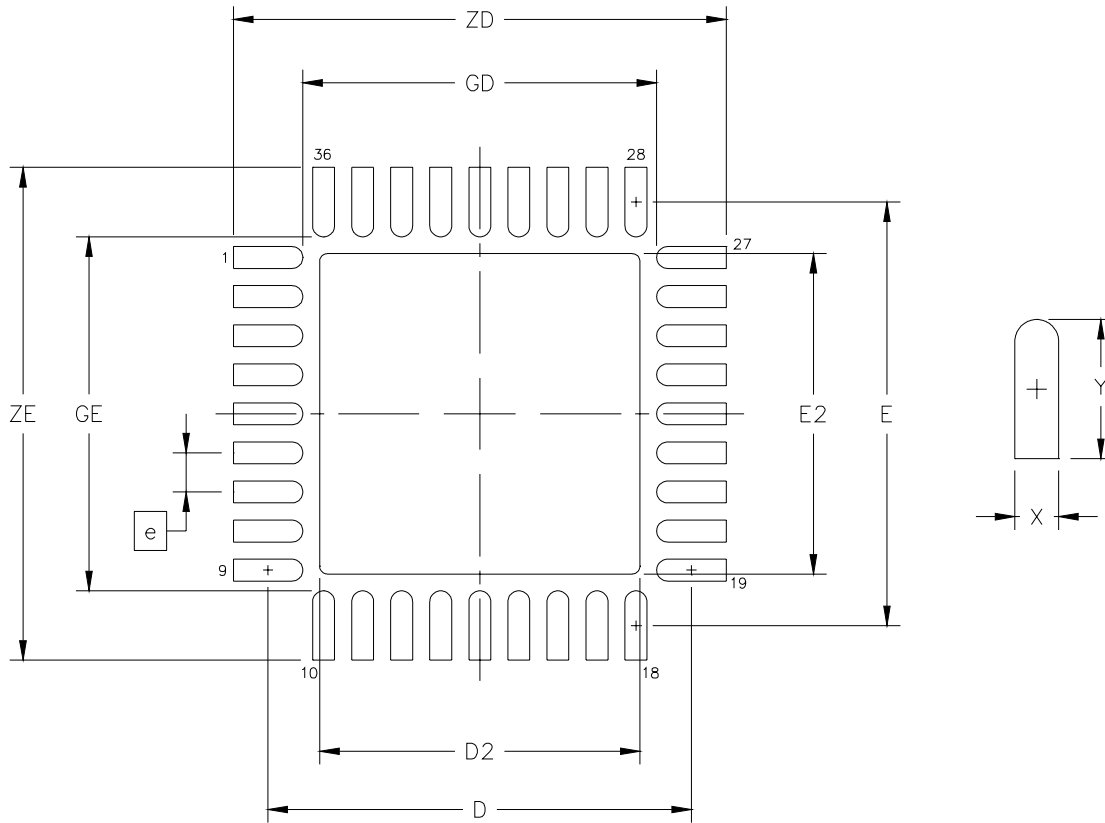
Figure 5. PCB Land Pattern Diagram

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Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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DOCUMENT CHANGE LIST

Revision 0.23 to Revision 0.24

- Clarified that the two outputs have a common, higher frequency source on page 1.
- Changed LVTTL to LVCMOS in Table 2, "Absolute Maximum Ratings," on page 3.
- Added Figure 1, "Typical Phase Noise Plot," on page 4.
- Updated "2. Pin Descriptions: Si5325".
  - Removed references to latency control, INC, and DEC.
  - Changed font for register names to underlined italics.
- Updated "3. Ordering Guide" on page 10.
- Added "5. Recommended PCB Layout".

Revision 0.24 to Revision 0.25

- Updated Section "2. Pin Descriptions: Si5325" on page 7.

Revision 0.25 to Revision 0.26

- Removed Figure 1. "Typical Phase Noise Plot."
- Changed pins 11 and 15 from NC to VDD in "2. Pin Descriptions: Si5325".

Revision 0.26 to Revision 0.3

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 2.
- Updated Table 2 on page 3.
- Added page 4.
- Updated "1. Functional Description" on page 6.
- Clarified "2. Pin Descriptions: Si5325" on page 7 including pull-up/pull-down.

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NOTES:

Si5325

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