

DIFFERENTIAL OUTPUT SILICON OSCILLATOR

Features

- Quartz-free silicon oscillator
- Any-rate output frequencies from 0.9 to 200 MHz
- Quick turn delivery
- Highly reliable startup and operation
- Tri-state or power down operation
- 1.8, 2.5, or 3.3 V options
- LVPECL, LVDS, HCSL, differential CMOS, and differential SSTL versions available
- 3.2 x 4.0 mm footprint compatible with industry-standard 3.2 x 5.0 mm pinout
- Low power
- Pb-free and RoHS compliant



Specifications

Parameters	Condition	Min	Typ	Max	Units
Frequency Range		0.9	—	200	MHz
Frequency Stability	See Note 1.	—	—	±150	ppm
Operating Temperature		0	—	+70	C°
Storage Temperature		-55	—	+125	C°
Supply Voltage	1.8 V option	1.71	—	1.98	V
	2.5 V option	2.25	—	2.75	V
	3.3 V option	2.97	—	3.63	V
Supply Current	LVPECL	—	34.0	36.0	mA
	Low Power LVPECL	—	19.3	22.2	mA
	LVDS	—	14.9	16.5	mA
	HCSL	—	25.3	29.3	mA
	Differential CMOS(3.3 V option,10 pF,200 MHz)	—	29.0	31.8	mA
	Differential SSTL-3	—	24.5	27.7	mA
	Differential SSTL-2	—	24.3	26.7	mA
	Differential SSTL-18	—	22.2	25	mA
	Tri-State	—	9.7	10.7	mA
Powerdown	—	1.0	1.9	mA	
Output Symmetry	$V_{DIFF} = 0$	$46 - 13 \text{ ns}/T_{CLK}$	—	$54 + 13 \text{ ns}/T_{CLK}$	%
Rise and Fall Times (20/80%) ²	LVPECL/LVDS	—	—	460	ps
	HCSL/Differential SSTL	—	—	800	ps
	Differential CMOS, 15 pF, ≥80 MHz	—	1.1	1.6	ns
LVPECL Output Option (DC coupling, 50 Ω to $V_{DD} - 2.0 \text{ V}$) ²	Mid-level	$V_{DD} - 1.5$	—	$V_{DD} - 1.34$	V
	Diff swing	.720	—	.880	V_{PK}
Low Power LVPECL Output Option (AC coupling, 100 Ω Differential Load) ²	Mid-level	—	N/A	—	V
	Diff swing	.68	—	.95	V_{PK}
LVDS Output Option (2.5/3.3 V) ($R_{TERM} = 100 \Omega \text{ diff}$) ²	Mid-level	1.15	—	1.26	V
	Diff swing	0.25	—	0.45	V_{PK}
LVDS Output Option (1.8 V) ($R_{TERM} = 100 \Omega \text{ diff}$) ²	Mid-level	0.85	—	0.96	V
	Diff swing	0.25	—	0.45	V_{PK}
HCSL Output Option ²	Mid-level	0.35	—	.425	V
	Diff swing	0.65	—	.82	V_{PK}
	DC termination per pad	45	—	55	Ω
CMOS Output Voltage ²	V_{OH} , sourcing 9 mA	$V_{DD} - 0.6$	—	—	V
	V_{OL} , sinking 9 mA	—	—	0.6	V
SSTL Output Voltage ²	SSTL-18	$.5 \times V_{DD} + 0.375$	—	$.5 \times V_{DD} - 0.375$	V
	SSTL-2	$.5 \times V_{DD} + 0.48$	—	$.5 \times V_{DD} - 0.48$	V
	SSTL-3	$.45 \times V_{DD} + 0.48$	—	$.45 \times V_{DD} - 0.48$	V
Powerup Time	From time V_{DD} crosses min spec supply	—	—	2	ms
OE Deassertion to Clk Stop		—	—	$250 + 3 \times T_{CLK}$	ns
Return from Output Driver Stopped Mode		—	—	$250 + 3 \times T_{CLK}$	ns
Return From Tri-State Time		—	—	$12 + 3 \times T_{CLK}$	μs
Return From Powerdown Time		—	—	2	ms
Period Jitter (1-sigma)	Non-CMOS	—	1	2	ps RMS
	CMOS, $C_L = 7 \text{ pF}$	—	1	3	ps RMS
Integrated Phase Jitter	1.0 MHz – min(20 MHz, $0.4 \times F_{OUT}$),non-CMOS	—	0.6	1	ps RMS
	1.0 MHz – min(20 MHz, $0.4 \times F_{OUT}$),CMOS format	—	0.7	1.5	ps RMS

Notes:

1. Inclusive of 25 C° initial frequency accuracy, operating temperature range, supply voltage change, output load change, 1st year aging at 25 C°, shock and vibration.
2. See AN409 for further details regarding output clock termination recommendations. SSTL minimum output voltage is minimum V_{OH} . SSTL maximum output voltage is maximum V_{OL} .

Si500D

Package Specifications

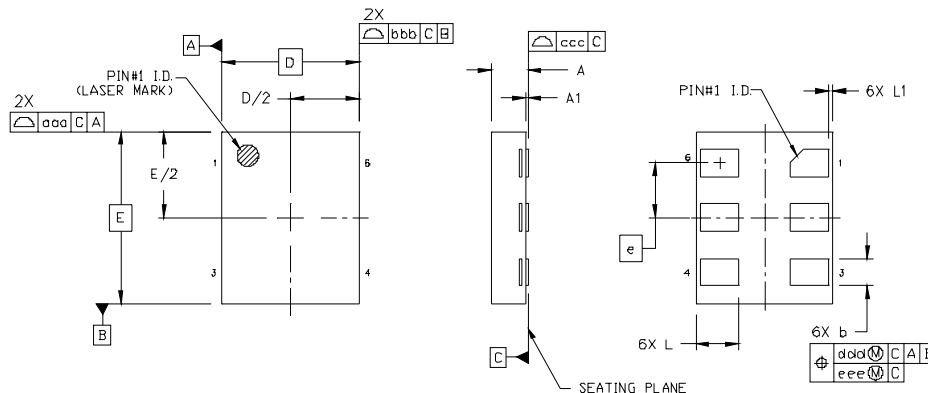


Table 1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.03	0.05
b	0.59	0.64	0.69
D	3.20 BSC.		
e	1.27 BSC.		
E	4.00 BSC.		
L	0.95	1.00	1.05

Dimension	Min	Nom	Max
L1	0.00	0.05	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Table 2. Pad Connections

1	OE
2	NC—Make no external connection to this pin
3	GND
4	Output
5	Complementary Output
6	VDD

Table 3. Tri-State/Powerdown/Driver Stopped Function on OE (3rd Option Code)

	A	B	C	D	E	F
Open	Active	Active	Active	Active	Active	Active
1 Level	Active	Tri-State	Active	Power-down	Active	Driver Stopped
0 Level	Tri-State	Active	Power-down	Active	Driver Stopped	Active

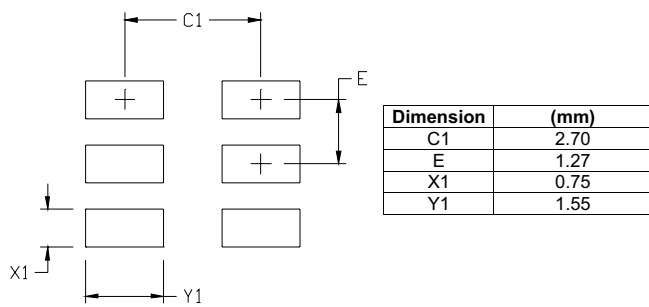
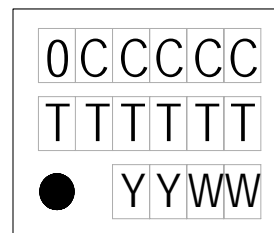


Figure 1. Recommended Land Pattern



0 = Si500
 CCCCC = mark code
 TTTTTT = assembly manufacturing code
 YY = year
 WW = work week

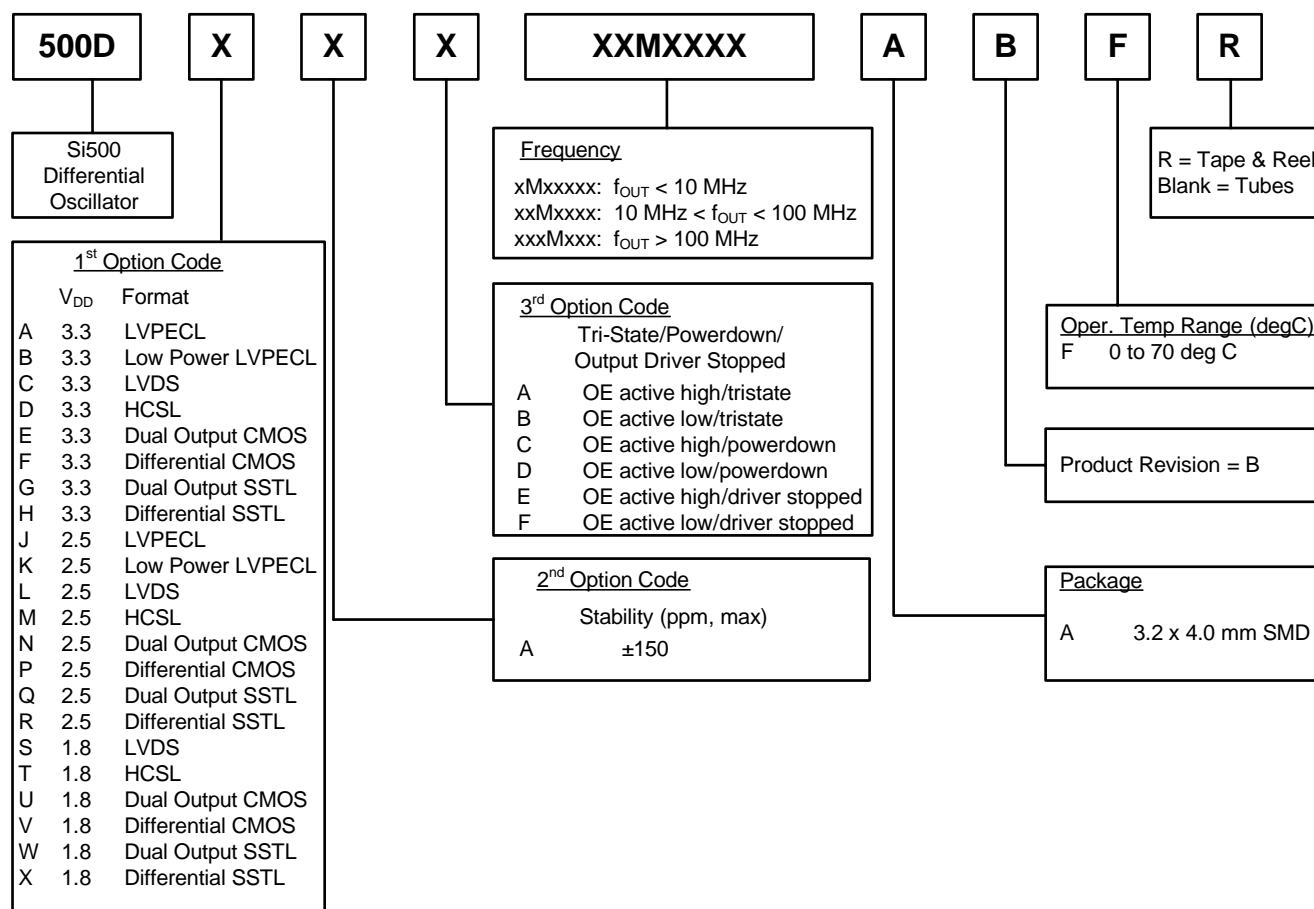
Figure 2. Top Mark

Environmental Compliance

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002.4
Mechanical Vibration	MIL-STD-883, Method 2007.3 A
Resistance to Soldering Heat	MIL-STD-202, 260 C° for 8 seconds
Solderability	MIL-STD-883, Method 2003.8
Damp Heat	IEC 68-2-3
Moisture Sensitivity Level	J-STD-020, MSL 3

Ordering Information

The Si500D supports a variety of options including frequency, output format, supply voltage, and tri-state/powerdown. Specific device configurations are programmed into the Si500D at time of shipment. Configurations are specified using the figure below. Silicon Labs provides a web-based part number utility that can be used to simplify part number configuration. Refer to www.silabs.com/XOPartNumber to access this tool. The Si500D XO series is supplied in a ROHS-compliant, Pb-free, 6-pad, 3.2 x 4.0 mm package. Tape and reel packaging is available as an ordering option.



Si500D

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: XOinfo@silabs.com
Internet: www.silabs.com

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