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April 1, 2003

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## 2SJ574

## Silicon P Channel MOS FET High Speed Switching <br> renesas

ADE-208-739B (Z)
3rd.Edition.
June 1999

## Features

- Low on-resistance

$$
\begin{aligned}
& \mathrm{R}_{\mathrm{DS}}=1.1 \Omega \operatorname{typ} \cdot\left(\mathrm{~V}_{\mathrm{GS}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}\right) \\
& \mathrm{R}_{\mathrm{DS}}=2.2 \Omega \operatorname{typ} \cdot\left(\mathrm{~V}_{\mathrm{GS}}=-4 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}\right)
\end{aligned}
$$

- 4 V gate drive device.
- Small package (MPAK)


## Outline

MPAK


1. Source
2. Gate
3. Drain

## Absolute Maximum Ratings $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Item | Symbol | Ratings | Unit |
| :--- | :--- | :--- | :--- |
| Drain to source voltage | $\mathrm{V}_{\text {DSs }}$ | -30 | V |
| Gate to source voltage | $\mathrm{V}_{\text {Gss }}$ | $\pm 20$ | V |
| Drain current | $\mathrm{I}_{\mathrm{D}}$ | -300 | mA |
| Drain peak current | $\mathrm{I}_{\mathrm{D} \text { (puse) }}$ Note | -1.2 | A |
| Body-drain diode reverse drain current | $\mathrm{I}_{\mathrm{DR}}$ | -300 | mA |
| Channel dissipation | $\mathrm{Pch}^{\text {Note } 2}$ | 400 | mW |
| Channel temperature | Tch | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

Note: 1. PW $\leq 10 \mu \mathrm{~s}$, duty cycle $\leq 1 \%$
2. Value on the alumina ceramic board $(12.5 \times 20 \times 0.7 \mathrm{~mm})$

## Electrical Characteristics $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Drain to source breakdown voltage | $\mathrm{V}_{\text {(BR) }}$ ( ${ }^{\text {ds }}$ | -30 | - | - | V | $\mathrm{I}_{\mathrm{D}}=-100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=0$ |
| Gate to source breakdown voltage | $\mathrm{V}_{(\mathrm{BR}) \mathrm{Gss}}$ | $\pm 20$ | - | - | V | $\mathrm{I}_{\mathrm{G}}= \pm 100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DS}}=0$ |
| Gate to source leak current | $\mathrm{I}_{\text {GSS }}$ | - | - | $\pm 5$ | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {GS }}= \pm 16 \mathrm{~V}, \mathrm{~V}_{\text {DS }}=0$ |
| Zero gate voltege drain current | $\mathrm{I}_{\text {DSS }}$ | - | - | -1 | $\mu \mathrm{A}$ | $V_{\text {DS }}=-30 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0$ |
| Gate to source cutoff voltage | $\mathrm{V}_{\text {GS(off) }}$ | -1.3 | - | -2.3 | V | $\mathrm{I}_{\mathrm{D}}=-10 \mu \mathrm{~A}, \mathrm{~V}_{\text {DS }}=-5 \mathrm{~V}$ |
| Static drain to source on state | $\mathrm{R}_{\text {DS(on) }}$ | - | 1.1 | 1.3 | $\Omega$ | $\mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}, \mathrm{~V}_{\text {GS }}=-10 \mathrm{~V}^{\text {Nole } 3}$ |
| resistance | $\mathrm{R}_{\text {DS(on) }}$ | - | 2.2 | 3.1 | $\Omega$ | $\mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}, \mathrm{~V}_{\mathrm{GS}}=-4 \mathrm{~V}^{\text {Note } 3}$ |
| Forward transfer admittance | $\left\|y_{\text {is }}\right\|$ | 195 | 300 | - | mS | $\mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}, \mathrm{~V}_{\text {DS }}=-10 \mathrm{~V}^{\text {Nole } 3}$ |
| Input capacitance | Ciss | - | 50 | - | pF | $\mathrm{V}_{\text {DS }}=-10 \mathrm{~V}$ |
| Output capacitance | Coss | - | 40 | - | pF | $\mathrm{V}_{\mathrm{GS}}=0$ |
| Reverse transfer capacitance | Crss | - | 15 | - | pF | $\mathrm{f}=1 \mathrm{MHz}$ |
| Turn-on delay time | $\mathrm{t}_{\mathrm{d}(0 n)}$ | - | 20 | - | ns | $\mathrm{I}_{\mathrm{D}}=-150 \mathrm{~mA}, \mathrm{~V}_{\mathrm{GS}}=-10 \mathrm{~V}$ |
| Rise time | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | - | ns | $\mathrm{R}_{\mathrm{L}}=66.6 \Omega$ |
| Turn-off delay time | $\mathrm{t}_{\text {doffif }}$ | - | 110 | - | ns |  |
| Fall time | $\mathrm{t}_{\mathrm{f}}$ | - | 105 | - | ns |  |

Note: 3. Pulse test
4. Marking is BP

## Main Characteristics





Switching Time Test Circuit


## Waveforms



## Package Dimensions



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