Overview

The SM5907AF is a compression and non compression type shock-proof memory controller LSI for compact disc players. The compression level can be set in 4 levels, and external memory can be selected from 4 options (4M, 4M× 2, 16M, 16M× 2). It operates from a 2.4 to 3.6 V supply voltage range.

Features

- 2-channel processing
- Serial data input
  - · 2s complement, 16-bit/MSB first, right-justified format
  - · Wide capture function
    (up to 3 × speed input rate)
- System clock input
  - · 384fs (16.9344 MHz)
- Shock-proof memory controller
  - · ADPCM compression method
  - · 4-level compression mode selectable
    4-bit compression mode 2.78 s/Mbit
    5-bit compression mode 2.22 s/Mbit
    6-bit compression mode 1.85 s/Mbit
    Full-bit non compression mode 0.74 s/Mbit
  - · 4 external DRAM configurations selectable
    1 or 2 × 16M DRAM (4M × 4 bits, refresh cycle = 2048 cycle)
    1 or 2 × 4M DRAM (1M × 4 bits)
- Microcontroller interface
  - · Serial command write and status read-out
  - · Data residual detector:
    15-bit operation, 16-bit output
  - · Forced mute
- Extension I/O
  Microcontroller interface for external control using 5 extension I/O pins
- +2.4 to +3.6 V operating voltage range
- Schmitt inputs
  All input pins (including I/O pins) except CLK (system clock)
- Reset signal noise elimination
  Approximately 3.8 µs or longer (65 system clock pulses) continuous LOW-level reset
- 44-pin QFP package (0.8 mm pin pitch)

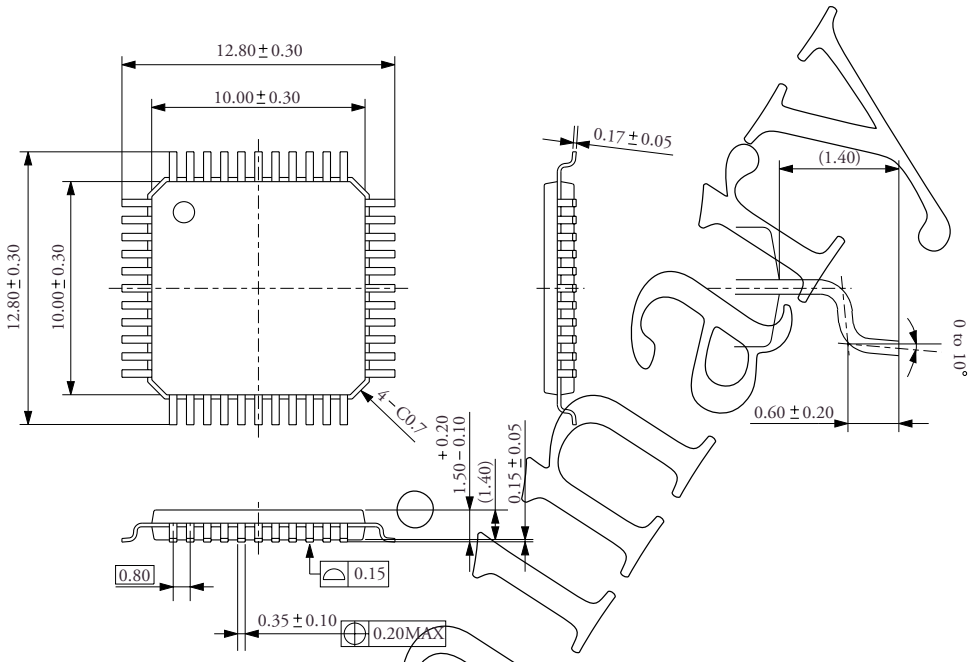
Ordering Information

SM5907AF	**44-pin QFP**

Package dimensions

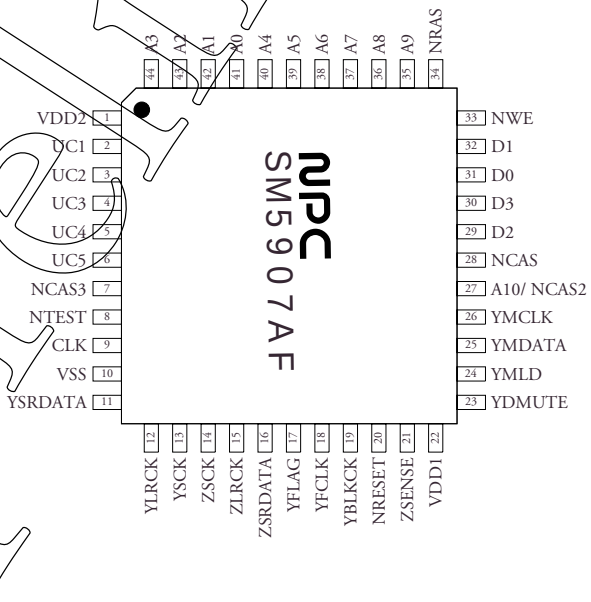
(Unit: mm)

44-pin QFP



Pinout

(Top View)



Pin description

Pin number	Pin name	I/O	Function	Setting	
				H	L
1	VDD2	-	VDD supply pin		
2	UC1	Ip/O	Microcontroller interface extension I/O 1		
3	UC2	Ip/O	Microcontroller interface extension I/O 2		
4	UC3	Ip/O	Microcontroller interface extension I/O 3		
5	UC4	Ip/O	Microcontroller interface extension I/O 4		
6	UC5	Ip/O	Microcontroller interface extension I/O 5		
7	NCAS3	O	DRAM2 $\overline{CAS}$ control (with two 16M DRAMs)		
8	NTEST	Ip	Test pin		Test
9	CLK	I	16.9344 MHz clock input		
10	VSS	-	Ground		
11	YSRDATA	I	Audio serial input data		
12	YLRCK	I	Audio serial input LR clock	Left channel	Right channel
13	YSCK	I	Audio serial input bit clock		
14	ZSCK	O	Audio serial output bit clock		
15	ZLRCK	O	Audio serial output LR clock	Left channel	Right channel
16	ZSRDATA	O	Audio serial output data		
17	YFLAG	I	Signal processor IC RAM overflow flag		Overflow
18	YFCLK	I	Crystal-controlled frame clock		
19	YBLKCK	I	Subcode block clock signal		
20	NRESET	I	System reset pin		Reset
21	ZSENSE	O	Microcontroller interface status output		
22	VDD1	-	VDD supply pin		
23	YDMUTE	I	Forced mute pin	Mute	
24	YMLD	I	Microcontroller interface latch clock		
25	YMDATA	I	Microcontroller interface serial data		
26	YMCLK	I	Microcontroller interface shift clock		
27	A10 (NCAS2)	O O	DRAM address 10 DRAM2 $\overline{CAS}$ control (with two 4M DRAMs)		
28	NCAS	O	DRAM $\overline{CAS}$ control		
29	D2	Ip/O	DRAM data input/output 2		
30	D3	Ip/O	DRAM data input/output 3		
31	D0	Ip/O	DRAM data input/output 0		
32	D1	Ip/O	DRAM data input/output 1		
33	NWE	O	DRAM $\overline{WE}$ control		
34	NRAS	O	DRAM $\overline{RAS}$ control		
35	A9	O	DRAM address 9		
36	A8	O	DRAM address 8		
37	A7	O	DRAM address 7		
38	A6	O	DRAM address 6		
39	A5	O	DRAM address 5		
40	A4	O	DRAM address 4		
41	A0	O	DRAM address 0		
42	A1	O	DRAM address 1		
43	A2	O	DRAM address 2		
44	A3	O	DRAM address 3		

Ip : Input pin with pull-up resistor Ip/O : Input/Output pin (With pull-up resistor when in input mode)

Absolute maximum ratings

(V_{SS} = 0V, VDD1, VDD2 pin voltage = V_{DD})

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	- 0.3 to 4.6	V
Input voltage	V_I	V_{SS} - 0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	- 55 to 125	˚C
Power dissipation	P_D	350	mW

Note. Refer to pin summary on the next page.
Values also apply for supply inrush and switch-off.

Electrical characteristics

Recommended operating conditions

(V_{SS} = 0V, VDD1, VDD2 pin voltage = V_{DD})

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.4 to 3.6	V
Operating temperature	T_{OPR}	- 40 to 85	˚C

DC characteristics

Standard voltage:(V_{DD1} = V_{DD2} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = - 40 to 85 ˚C)

Parameter	Pin	Symbol		Condition	Rating			Unit
					Min	Typ	Max	
Current consumption	VDD	I_{DD}		(*A)SHPRF ON		4.5	8.0	mA
				(*A)Through mode		1.8	3.0	mA
Input voltage	CLK	H level	V_{IH1}		0.7V_{DD}			V
		L level	V_{IL1}				0.3V_{DD}	V
			V_{INAC}	AC coupling	1.0			V_{P-P}
	(*2,3,4)	H level	V_{IH2}		0.7V_{DD}			V
		L level	V_{IL2}				0.3V_{DD}	V
Output voltage	(*4,5)	H level	V_{OH1}	I_{OH} = - 0.5 mA	V_{DD} - 0.4			V
		L level	V_{OL1}	I_{OL} = 0.5 mA			0.4	V
Input current	CLK	I_{IH1}		V_{IN} = V_{DD}	5	25	115	µA
		I_{IL1}		V_{IN} = 0V	5	25	115	µA
	(*3,4)	I_{IL2}		V_{IN} = 0V	1	4	15	µA
Input leakage current	(*2,3,4)	I_{LH}		V_{IN} = V_{DD}			1.0	µA
	(*2)	I_{LL}		V_{IN} = 0V			1.0	µA

(*A) V_{DD1} = V_{DD2} = 3 V, CLK input frequency f_{XTI}= 384fs = 16.9344 MHz, all outputs unloaded,
SHPRF: Shock-proof,
typical values are for V_{DD1} = V_{DD2} = 3 V.

Low-voltage:(V_{DD1} = V_{DD2} = 2.4 to 3.0 V, V_{SS} = 0 V, Ta = - 20 to 70 ˚C)

Parameter	Pin	Symbol		Condition	Rating			Unit
					Min	Typ	Max	
Current consumption	VDD	I_{DD}		(*B)SHPRF ON		4.5	8.0	mA
				(*B)Through mode		1.8	3.0	mA
Input voltage	CLK	H level	V_{IH1}		0.7V_{DD}			V
		L level	V_{IL1}				0.3V_{DD}	V
			V_{INAC}	AC coupling	1.0			V_{P-P}
	(*2,3,4)	H level	V_{IH2}		0.7V_{DD}			V
		L level	V_{IL2}				0.3V_{DD}	V
Output voltage	(*4,5)	H level	V_{OH1}	I_{OH} = - 0.5 mA	V_{DD} - 0.4			V
		L level	V_{OL1}	I_{OL} = 0.5 mA			0.4	V
Input current	CLK	I_{IH1}		V_{IN} = V_{DD}	5	25	115	µA
		I_{IL1}		V_{IN} = 0V	5	25	115	µA
	(*3,4)	I_{IL2}		V_{IN} = 0V	1	4	15	µA
Input leakage current	(*2,3,4)	I_{LH}		V_{IN} = V_{DD}			1.0	µA
	(*2)	I_{LL}		V_{IN} = 0V			1.0	µA

(*B) V_{DD1} = V_{DD2} = 3 V, CLK input frequency f_{XTI}= 384fs = 16.9344 MHz, all outputs unloaded,
SHPRF: Shock-proof,
typical values are for V_{DD1} = V_{DD2} = 3 V.

<Pin summary>

(*1)	Pin function	Clock input pin (AC input)
	Pin name	CLK
(*2)	Pin function	Schmitt input pins
	Pin name	YSRDATA, YLRCK, YSCK, YFLAG, YFCLK, NRESET, YBLKCK, YDMUTE, YMLD, YMDATA, YMCLK
(*3)	Pin function	Schmitt input pin with pull-up
	Pin name	NTEST
(*4)	Pin function	I/O pins (Schmitt input with pull-up in input state)
	Pin name	UC1, UC2, UC3, UC4, UC5, D0, D1, D2, D3
(*5)	Pin function	Outputs
	Pin name	ZSCK, ZLRCK, ZSRDATA, ZSENSE, NCAS, NCAS2, NCAS3, NWE, NRAS, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10

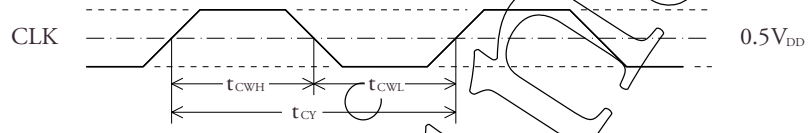
AC characteristics

Standard voltage: V_{DD1} = V_{DD2} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = -40 to 85 ˚C
Low-voltage: V_{DD1} = V_{DD2} = 2.4 to 3.0 V, V_{SS} = 0 V, Ta = -20 to 70 ˚C
(*) Typical values are for fs = 44.1 kHz

System clock (CLK pin)

Parameter	Symbol	Condition	Rating			Unit
		System clock	Min	Typ	Max	
Clock pulsewidth (HIGH level)	t_{CWH}		26	29.5	125	ns
Clock pulsewidth (LOW level)	t_{CWL}		26	29.5	125	ns
Clock pulse cycle	t_{CY}	384fs	58	59	250	ns

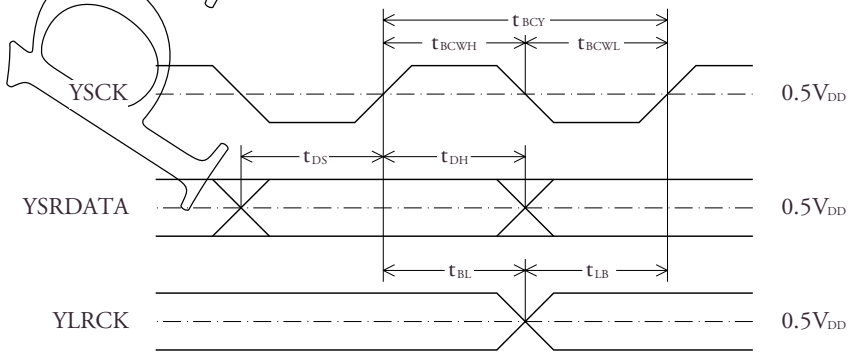
System clock input



Serial input (YSRDATA, YLRCK, YSCK pins)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
YSCK pulsewidth (HIGH level)	t_{BCWH}	75			ns	
YSCK pulsewidth (LOW level)	t_{BCWL}	75			ns	
YSCK pulse cycle	t_{BCY}	150			ns	
YSRDATA setup time	t_{DS}	50			ns	
YSRDATA hold time	t_{DH}	50			ns	
Last YSCK rising edge to YLRCK edge	t_{BL}	50			ns	
YLRCK edge to first YSCK rising edge	t_{LB}	50			ns	
YLRCK pulse frequency See note below.		0		3fs		Memory system ON (MSON=H)
		fs		fs		Memory system OFF (MSON=L)

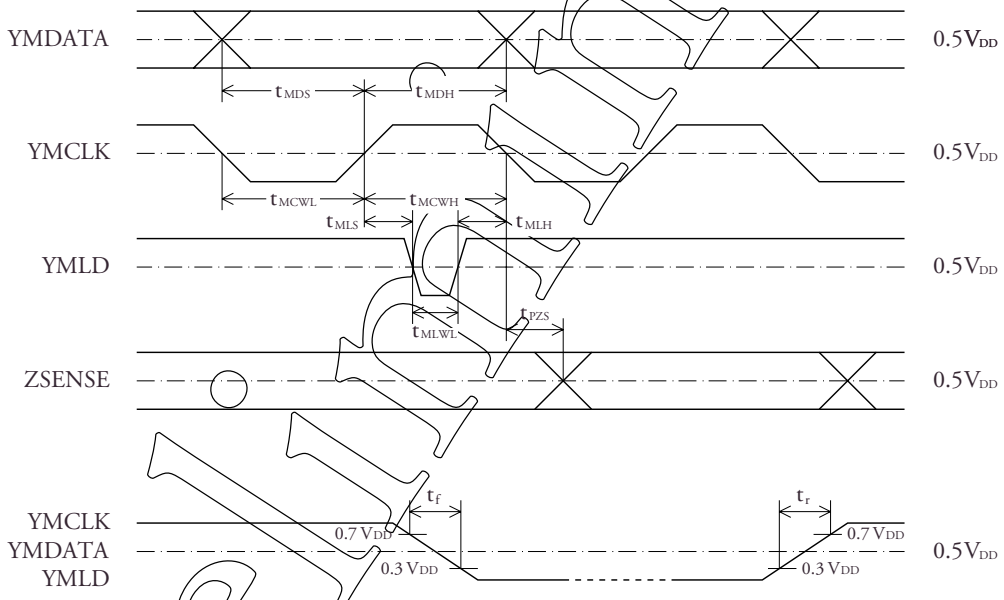
Note. When the memory system is OFF (through mode), the input data rate is synchronized to the system clock input (384fs), so input data needs to be at 1/384 of this frequency. But, this IC can tolerate a certain amount of jitter. For details, refer to Through-mode operation.



Microcontroller interface (YMCLK, YMDATA, YMLD, ZSENSE pins)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
YMCLK LOW-level pulsewidth	t_{MCWL}	30 + 2t_{CY}			ns
YMCLK HIGH-level pulsewidth	t_{MCWH}	30 + 2t_{CY}			ns
YMDATA setup time	t_{MDS}	30 + t_{CY}			ns
YMDATA hold time	t_{MDH}	30 + t_{CY}			ns
YMLD LOW-level pulsewidth	t_{MLWL}	30 + 2t_{CY}			ns
YMLD setup time	t_{MLS}	30 + t_{CY}			ns
YMLD hold time	t_{MLH}	30 + t_{CY}			ns
Rise time	t_r			100	ns
Fall time	t_f			100	ns
ZSENSE output delay	t_{PZS}			100 + 3t_{CY}	ns

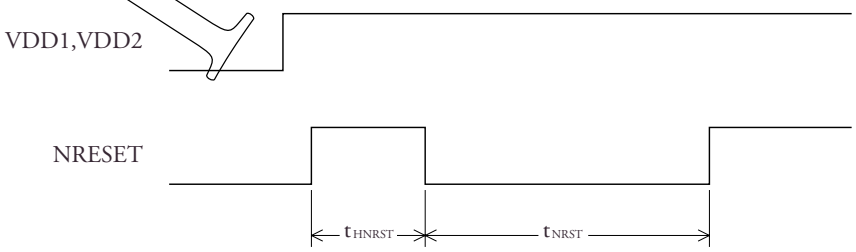
Note. t_{CY} is the system clock cycle time (59ns typ).



Reset input (NRESET pin)

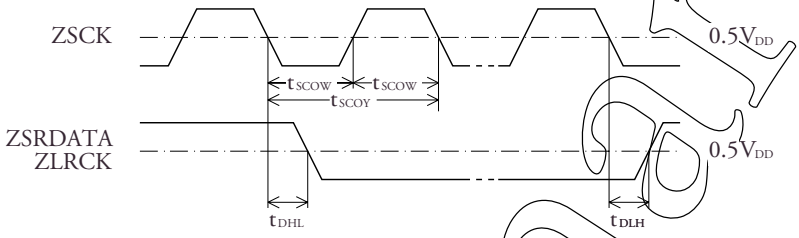
Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
First HIGH-level after supply voltage rising edge	t_{HNRST}	0			t_{CY} (Note)
NRESET pulsewidth	t_{NRST}	64			t_{CY} (Note)

Note. t_{CY} is the system clock (CLK) input (384fs) cycle time.
t_{CY} = 59 ns, t_{NRST} (min) = 3.8 µs when fs = 44.1 kHz



Serial output (ZSRDATA, ZLRCK, ZSCK pins)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
ZSCK pulsewidth	t_{SCOW}	15 pF load		1/96fs		
ZSCK pulse cycle	t_{SCOY}	15 pF load		1/48fs		
ZSRDATA and ZLRCK output delay time	t_{DHL}	15 pF load	0		60	ns
	t_{DLH}	15 pF load	0		60	ns

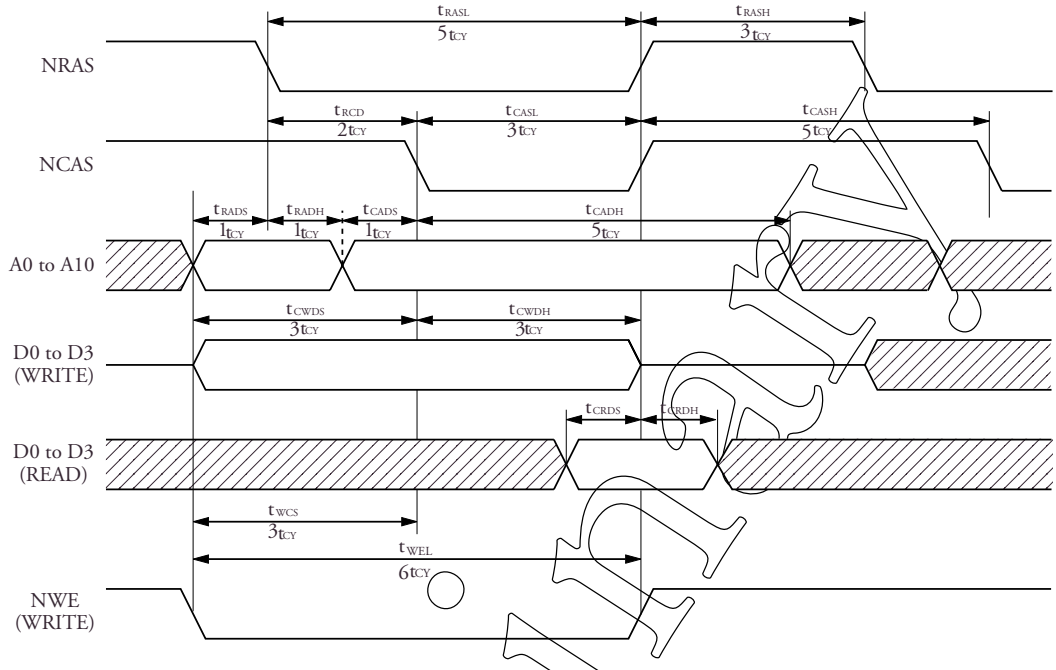


DRAM access timing (NRAS, NCAS, NCAS2, NCAS3, NWE, A0 to A10, D0 to D3)

Parameter		Symbol	Condition		Rating			Unit
					Min	Typ	Max	
NRAS pulsewidth		t_{RASL}	15 pF load			5		t_{CY}(note)
		t_{RASH}	15 pF load		3			t_{CY}
NRAS falling edge to NCAS falling edge		t_{RCD}	15 pF load			2		t_{CY}
NCAS pulsewidth		t_{CASH}	15 pF load		5			t_{CY}
		t_{CASL}	15 pF load			3		t_{CY}
NRAS	Setup time	t_{RADS}	15 pF load			1		t_{CY}
falling edge to address	Hold time	t_{RADH}	15 pF load			1		t_{CY}
NCAS	Setup time	t_{CADS}	15 pF load			1		t_{CY}
falling edge to address	Hold time	t_{CADH}	15 pF load			5		t_{CY}
NCAS	Setup time	t_{CWDS}	15 pF load			3		t_{CY}
falling edge to data write	Hold time	t_{CWDH}	15 pF load			3		t_{CY}
NCAS	Input setup	t_{CRDS}			40			ns
rising edge to data read	Input hold	t_{CRDH}			0			ns
NWE pulsewidth		t_{WEL}	15 pF load			6		t_{CY}
NWE falling edge to NCAS falling edge		t_{WCS}	15 pF load			3		t_{CY}
Refresh cycle (fs = 44.1 kHz playback) Memory system ON Decode sequence operation (RDEN=H)		t_{REF}	4M DRAM × 1 or × 2	Non compression			3.0	ms
				6-bit compression			7.3	ms
				5-bit compression			8.8	ms
				4-bit compression			10.9	ms
			16M DRAM × 1 or × 2	Non compression			5.9	ms
				6-bit compression			14.6	ms
				5-bit compression			17.5	ms
				4-bit compression			21.8	ms

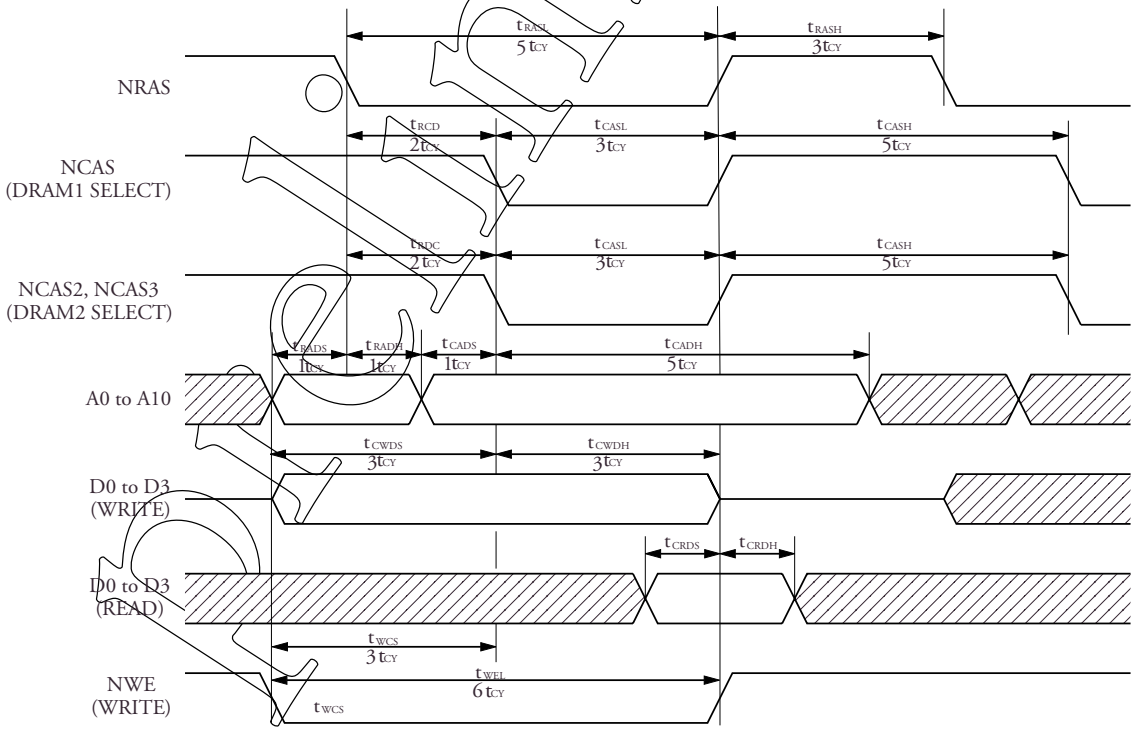
Note. t_{CY} is the system clock (CLK) input (384fs) cycle time. t_{CY} = 59 ns when fs = 44.1 kHz

DRAM access timing (with single DRAM)



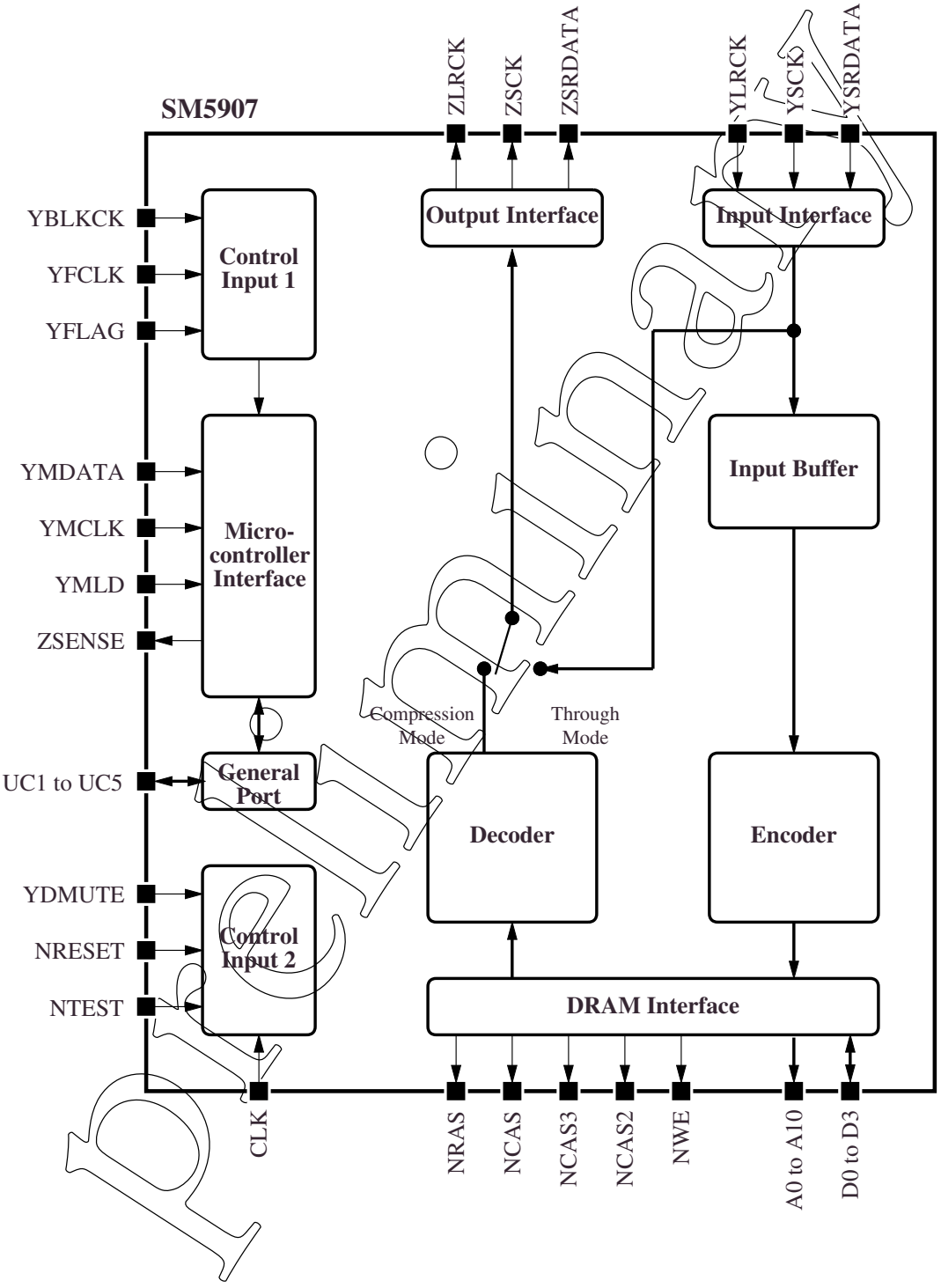
The NWE terminal output is fixed HIGH during read timing.

DRAM access timing (with double DRAMs)



The NWE terminal output is fixed HIGH during read timing.
NCAS terminal output is fixed HIGH when selecting "DRAM2".
NCAS2/NCAS3 terminal outputs are fixed HIGH when selecting "DRAM1".

Block diagram



Functional description

SM5907AF has two modes of operation; shock-proof mode and through mode.

The operating sequences are controlled using commands from a microcontroller.

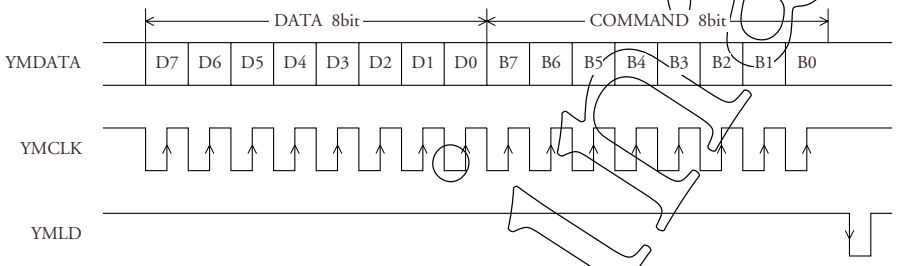
Microcontroller interface

Command format

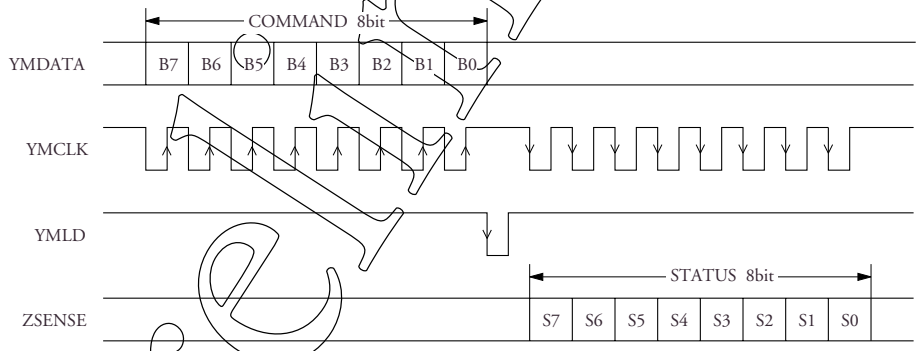
Commands from the microcontroller are input using 3-wire serial interface inputs; data (YMDATA), bit clock (YMCLK) and load signal (YMLD).

In the case of a read command from the microcontroller, bit serial data is output (ZSENSE) synchronized to the bit clock input (YMCLK).

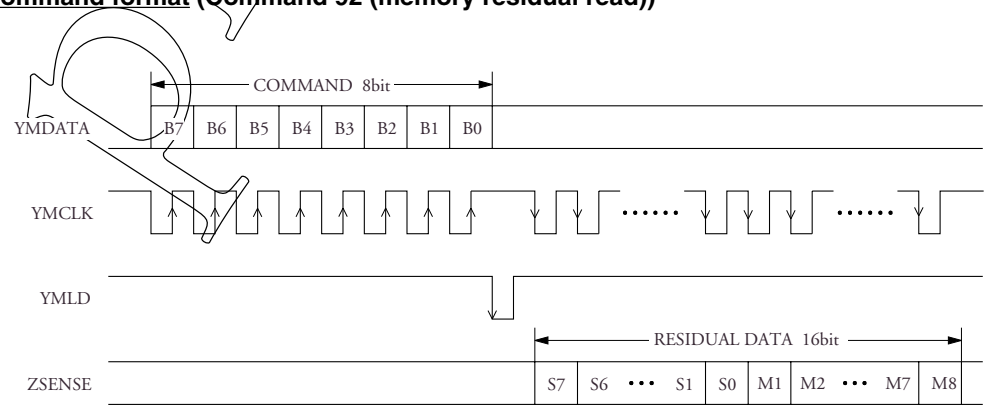
Write command format (Commands 80 to 85)



Read command format (Commands 90, 91, 93)



Read command format (Command 92 (memory residual read))



Command table

Write command summary

MS command 80

Shock-proof memory system settings

80hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0000

Bit	Name	Function	H operation	Reset level
D7	MSWREN	Encode sequence start/stop	Start	L
D6	MSWACL	Write address reset	Reset	L
D5	MSRDEN	Decode sequence start/stop	Start	L
D4	MSRACL	Read address reset	Reset	L
D3	MSDCN2	MSDCN2=H, MSDCN1=H: 3-pair comparison start MSDCN2=H, MSDCN1=L: 2-pair comparison start		L
D2	MSDCN1	MSDCN2=L, MSDCN1=H: Direct-connect start MSDCN2=L, MSDCN1=L: Connect operation stop		L
D1	WAQV	Q data valid	Valid	L
D0	MSON	Memory system ON	ON	L

Extension I/O settings 81

Extension I/O port input/output settings

81hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0001

Bit	Name	Function	H operation	Reset level
D7				
D6				
D5				
D4	UC5OE	Extension I/O port UC5 input/output setting	Output	L
D3	UC4OE	Extension I/O port UC4 input/output setting	Output	L
D2	UC3OE	Extension I/O port UC3 input/output setting	Output	L
D1	UC2OE	Extension I/O port UC2 input/output setting	Output	L
D0	UC1OE	Extension I/O port UC1 input/output setting	Output	L

Extension I/O output data settings 82

Extension port HIGH/LOW output level

A port setting is invalid if that port has already been defined as an input using the 81H command above.

82hex = B7 B6 B5 B4 1000 B3 B2 B1 B0 0010

Bit	Name	Function	H operation	Reset level
D7				
D6				
D5				
D4	UC5WD	Extension I/O port UC5 output data setting	H output	L
D3	UC4WD	Extension I/O port UC4 output data setting	H output	L
D2	UC3WD	Extension I/O port UC3 output data setting	H output	L
D1	UC2WD	Extension I/O port UC2 output data setting	H output	L
D0	UC1WD	Extension I/O port UC1 output data setting	H output	L

MUTE, CMP12 settings 83

83hex = 1000 0011 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	H operation	Reset level
D7				
D6	MUTE	Forced muting (changes instantaneously)	Mute ON	L
D5				
D4				
D3	CMP12	12-bit comparison connect/ 16-bit comparison connect	12-bit comparison	L
D2				
D1				
D0				

Refer to "Force mute", "12-bit comparison connection".

Option settings 85

85hex = 1000 0101 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	H operation	Reset level
D7	RAMS1	DRAM type setting RAMS1=0 RAMS2=0 when 16M DRAM(4M × 4bit) × double RAMS1=1 RAMS2=0 when 4M DRAM(1M × 4bit) × single		L
D6	RAMS2	RAMS1=0 RAMS2=1 when 4M DRAM(1M × 4bit) × double RAMS1=1 RAMS2=1 when 16M DRAM(4M × 4bit) × single		L
D5	YFLGS	FLAG6 set conditions (reset using status read command 90H) - When YFLGS=0, YFCKP=0, YFCLK input falling edge, YFLAG=L - When YFLGS=0, YFCKP=1, YFCLK input rising edge, YFLAG=L		L
D4	YFCKP	- When YFLGS=1, YFCKP=0, YFLAG=L When YFLGS=1, YFCKP=1, YFLAG=H		L
D3	COMPFB	Full-bit compression mode		L
D2	COMP6B	6-bit compression mode		H
D1	COMP5B	5-bit compression mode		L
D0	COMP4B	4-bit compression mode		L

When the number of compression bits is set incorrectly (2 or more bits in D0 to D3 are set to 1 or all bits are set to 0), 6-bit compression mode is selected.

Read command summary

Shock-proof memory status (1) 90

90hex = 1001 0000 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	HIGH-level state
S7	FLAG6	Signal processor IC jitter margin exceeded	Exceeded
S6	MSOVF	Write overflow (Read once only when RA exceeds WA)	DRAM overflow
S5	BOVF	Input buffer memory overflow because sampling rate of input data is too fast	Input buffer memory overflow
S4			
S3	DCOMP	Data compare-connect sequence operating	Compare-connect sequence operating
S2	MSWIH	Encode sequence stop due to internal factors	Encoding stopped
S1	MSRIH	Decode sequence stop due to internal factors	Decoding stopped
S0			

Refer to "Status flag operation summary".

Shock-proof memory status (2) 91

91hex = 1001 0001 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	HIGH-level state
S7	MSEMP	Valid data empty state (Always HIGH when RA exceeds VWA)	No valid data
S6	OVFL	Write overflow state (Always HIGH when WA exceeds RA)	Memory full
S5	ENCOD	Encode sequence operating state	Encoding
S4	DECOD	Decode sequence operating state	Decoding
S3			
S2			
S1			
S0			

Refer to "Status flag operation summary".

Shock-proof memory valid data residual 92

92hex = 1001 0010 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	4M×1, 4M×2, 16M×1	16M×2
S7	AM21	Valid data accumulated VWA-RA (MSB)	8M bits	16M bits
S6	AM20		4M bits	8M bits
S5	AM19		2M bits	4M bits
S4	AM18		1M bits	2M bits
S3	AM17		512k bits	1M bits
S2	AM16		256k bits	512k bits
S1	AM15		128k bits	256k bits
S0	AM14		64k bits	128k bits
M1	AM13		32k bits	64k bits
M2	AM12		16k bits	32k bits
M3	AM11		8k bits	16k bits
M4	AM10		4k bits	8k bits
M5	AM09		2k bits	4k bits
M6	AM08		1k bits	2k bits
M7	AM07		512 bits	1k bits
M8	AM06		256 bits	512 bits

Note. The time conversion factor varies depending on the compression bit mode.(M = 1,048,576 K= 1,024)

Residual time (sec) = Valid data residual (Mbits) × Time conversion value K

where the Time conversion value K (sec/Mbit) ≈ 2.78(4 bits), 2.22 (5 bits), 1.85 (6 bits) and 0.74 (Full bits).

Extension I/O inputs 93

Input data entering (or output data from) an extension port terminal is echoed to the microcontroller.
(That is, the input data entering an I/O port configured as an input port using the 81H command,
OR the output data from a pin configured as an output port using the 82H command.)

93hex = 1001 0011 (B7 B6 B5 B4 B3 B2 B1 B0)

Bit	Name	Function	HIGH-level state
S7			
S6			
S5			
S4	UC5RD		
S3	UC4RD		
S2	UC3RD		
S1	UC2RD		
S0	UC1RD		

Status flag operation summary

Flag name	Read method		
FLAG6	READ 90H bit 7	Meaning	- Indicates to the CD signal processor DSP (used for error correction, de-interleaving) that a disturbance has exceeded the RAM jitter margin.
		Set	- Set according to the YFLAG input and the operating state of YFCKP and YFLGS. FLAG6 set conditions When YFLGS=0, YFCKP=0, YFCLK input falling edge, YFLAG=L When YFLGS=0, YFCKP=1, YFCLK input rising edge, YFLAG=L When YFLGS=1, YFCKP=0, YFLAG=L When YFLGS=1, YFCKP=1, YFLAG=H
		Reset	- By 90H status read - By 80H command when MSON=ON - After external reset
MSOVF	READ 90H bit 6	Meaning	- Indicates once only that a write to external DRAM has caused an overflow. (When reset by the 90H status read command, this flag is reset even if the overflow condition continues.)
		Set	- When the write address (WA) exceeds the read address (RA)
		Reset	- By 90H status read - When a read address clear (MSRACL) or write address clear (MSWACL) command is issued - After external reset
BOVF	READ 90H bit 5	Meaning	- Indicates input data rate was too fast causing buffer overflow and loss of data
		Set	- When inputs a data during a buffer memory overflow
		Reset	- By 90H status read - When a read address clear (MSRACL) or write address clear (MSWACL) command is issued - After external reset
DCOMP	READ 90H bit 3	Meaning	- Indicates that a compare-connect sequence is operating
		Set	- When a (3-pair or 2-pair) compare-connect start command is received (MSDCN2=1) - When a direct connect command is received (MSDCN2=0, MSDCN1=1)
		Reset	- When a (3-pair or 2-pair) comparison detects conforming data - When the connect has been performed after receiving a direct connect command - When a compare-connect stop command (MSDCN2=0, MSDCN1=0) is received - When a MSWREN=1 command is received (However, if a compare-connect command is received at the same time, the compare-connect command has priority.) - After external reset
MSWIH	READ 90H bit 2	Meaning	- Indicates that the encode sequence has stopped due to internal factors (not microcontroller commands)
		Set	- When FLAG6 (above) is set - When BOVF (above) is set - When MSOVF (above) is set
		Reset	- When conforming data is detected after receiving a compare-connect start command - When the connect has been performed after receiving a direct connect command - When a read address clear (MSRACL) or write address clear (MSWACL) command is received - After external reset
MSRIH	READ 90H bit 1	Meaning	- Indicates that the decode sequence has stopped due to internal factors (not microcontroller commands)
		Set	- When the valid data residual becomes 0
		Reset	- By 90H status read - When a read address clear (MSRACL) or write address clear (MSWACL) command is issued - After external reset

Flag name	Read method		
MSEMP	READ 91H bit 7	Meaning	- Indicates that the valid data residual has become 0
		Set	- When the VWA (final valid data's next address) = RA (address from which the next read would take place)
		Reset	- Whenever the above does not apply
OVFL	READ 91H bit 6	Meaning	- Indicates a write to external DRAM overflow state
		Set	- When the write address (WA) exceeds the read address (RA). (Note: This flag is not set when WA=RA through an address initialize or reset operation.)
		Reset	- When the read address (RA) is advanced by the decode sequence - When a read address clear (MSRACL) or write address clear (MSWACL) command is issued - After external reset
ENCOD	READ 91H bit 5	Meaning	- Indicates that the encode sequence (input data entry, encoding, DRAM write) is operating
		Set	- By the 80H command when MSWREN=1 - When conforming data is detected during compare-connect operation - When the connect has been performed after receiving a direct connect command
		Reset	- When the FLAG6 flag=1 (above) - When the OVFL flag=1 (above) - By the 80H command when MSWREN=0 - By the 80H command when MSDCN1=1 or MSDCN2=1 (compare-connect start command) - By the 80H command when MSON=0 - After external reset Note. Reset conditions have priority over set conditions. For example, if the 80H command has MSWREN=1 and MSDCN1=1, the ENCOD flag is reset and compare-connect operation starts.
DECOD	READ 91H bit 4	Meaning	- Indicates that the decode sequence (read from DRAM, decoding, attenuation, data output) is operating
		Set	- By a new 80H command when MSRDEN=1 and the MSEMP flag=0 (above)
		Reset	- Whenever the above does not apply

Write command supplementary information

80H (MS command)

- MSWREN

When 1: Encode sequence starts

Invalid when MSON is not 1 within the same 80H command

Invalid when FLAG6=1

Invalid when OVFL=1

Invalid when a compare-connect start command (MSDCN2=1 or MSDCN1=1) occurs simultaneously

Direct connect if a compare-connect sequence is already operating

When 0: Encode sequence stops

- MSWACL

When 1: Initializes the write address (WA)

When 0: No operation

- MSRDEN

When 1: Decode sequence starts

Does not perform decode sequence if MSON=1.If there is no valid data, decode sequence temporarily stops. But, because the MSRDEN flag setting is maintained as is, the sequence automatically re-starts when valid data appears.

When 0: Decode sequence stops

-MSRACL

When 1: Initializes the read address (RA)

When 0: No operation

- MSDCN2, MSDCN1

When 1 and 1: 3-pair compare-connect sequence starts

When 1 and 0: 2-pair compare-connect sequence starts

When 0 and 1: Direct connect sequence starts

When 0 and 0: Compare-connect sequence stops. No operation if a compare-connect sequence is not operating.

- WAQV

When 1: The immediately preceding YBLKCK falling-edge timing WA (write address) becomes the VWA (valid write address).

When 0: No operation

- MSON

When 1: Memory system turns ON and shock-proof operation starts

When 0: Memory system turns OFF and through-mode playback starts. (In this mode, the attenuator is still active.)

81H (Extension I/O port settings)

82H (Extension I/O port output data settings)

83H (MUTE, 12-bit comparison connection settings)

- MUTE (forced muting)

When 1: Outputs are instantaneously muted to 0.(note 1)

Same effect as taking the YDMUTE pin HIGH.

When 0: No muting(note 1)

(note1) Effective at the start left-channel output data.

- MUTE, YDMUTE relationship

When all mute inputs are 0, mute is released.

- CMP12 (12-bit comparison connection)

When 1: Performs comparison connection using only the most significant 12 bits of input data.

When 0: Performs comparison connection using all 16 bits of input data.

85H (option settings)

- RAMS1, RAMS2

When 0 and 0 : 16M DRAM (4M×4 bits)×double

When 1 and 0 : 4M DRAM (1M×4 bits)×single

When 0 and 1 : 4M DRAM (1M×4 bits)×double

When 1 and 1 : 16M DRAM (4M×4 bits)×single

- YFLGS, YFCKP

When 0 and 0: Sets FLAG6 on the falling edge of YFCLK when YFLAG=0

When 0 and 1: Sets FLAG6 on the rising edge of YFCLK when YFLAG=0

When 1 and 0: Sets FLAG6 when YFLAG=0

When 1 and 1: Sets FLAG6 when YFLAG=1

- COMPFB, COMP6B, COMP5B, COMP4B

When 0, 0, 0 and 1: Selects 4-bit compression mode

When 0, 0, 1 and 0: Selects 5-bit compression mode

When 1, 0, 0 and 0: Selects full-bit compression mode

In all other cases: Selects 6-bit compression mode

Changing mode without initializing during operation is possible.

Shock-proof operation overview

Shock-proof mode is the mode that realizes shock-proof operation using external DRAM. Shock-proof mode is invoked by setting MSON=H in microcontroller command 80H.

This mode comprises the following 3 sequences.

- Encode sequence

1. Input data from a signal processor IC is stored in internal buffers.
2. Encoder starts after a fixed number of data have been received.
3. The encoder, after the most suitable predicting filter type and quantization steps have been determined, performs ADPCM encoding and then writes to external DRAM.

- Decode sequence

1. Reads compressed data stored in external buffer RAM at rate fs.
2. Decoder starts, using the predicting filter type and quantization levels used when encoded.
3. Outputs the result.

- Compare-connect sequence

1. Encoding immediately stops when either external buffer RAM overflows or when a CD read error occurs due to shock vibrations.
2. Then, using microcontroller command 80H, the compare-connect start command is executed and compare-connect sequence starts.
3. Compares data re-read from the CD with the processed final valid data stored in RAM (confirms its correctness).
4. As soon as the comparison detects conforming data, compare-connect sequence stops and encode sequence re-starts, connecting the data directly behind previous valid data.

RAM addresses

The SM5907AF uses either 1 or 2 external 4M or 16M DRAMs as external buffers.

Three kinds of addresses are used for external RAM control.

WA (write address)

RA (read address)

VWA (valid write address)

Among these, VWA is the write address for conforming data whose validity has been confirmed. Determination of the correctness of data read from the CD is delayed relative to the encode write processing, so VWA is always delayed relative to WA.

The region available for valid data is the area between VWA-RA.

- Connect data work area

This is an area of memory reserved for connect data. This area is 4k bits if using 4M DRAMs or 8k bits if using 16M DRAMs.

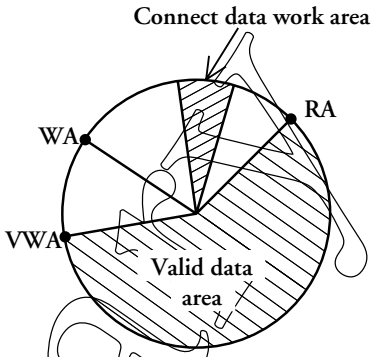


Fig 1. RAM addresses

VWA (valid write address)

The VWA is determined according to the YBLKCK pin and WAQV command. Refer to the timing chart below.

1.YBLKCK is a 75 Hz clock(HIGH for 136 µs) when used for normal read mode and it is a 150 Hz clock when used for double-speed read mode, synchronized to the CD format block end timing.

When this clock goes LOW, WA which is the write address of internal encode sequence, is stored (see note 2).

2.The microcontroller checks the subcode and, if confirmed to be correct, generates a WAQV command (80H).

3.When the WAQV command is received, the previously latched WA is stored as the VWA.

(note 2) Actually, there is a small time difference, or gap, between the input data and YBLKCK. This gap serves to preserves the preceding WA to protect against incorrect operation.

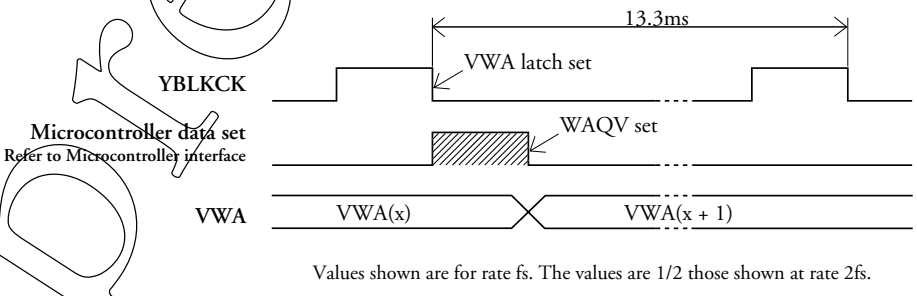


Fig 2. YBLKCK and VWA relationship

YFLAG, YFCLK, FLAG6

Correct data demodulation becomes impossible for the CD signal processor IC when a disturbance exceeding the RAM jitter margin occurs. The YFLAG signal input pin is used to indicate when such a condition has occurred.

The YFCLK is a 7.35 kHz clock synchronized to the CD format frame 1.

The IC checks the YFLAG input and stops the encode sequence when such a disturbance has occurred, and then makes FLAG6 active.

The YFLAG check method used changes depending on the YFLGS flag and YFCKP flag (85H command). See table1.

If YFLAGS is set to 1, then YFCLK should be tied either High or Low.

85H command			FLAG6 set conditions		FLAG6 reset conditions
	YFLGS	YFCKP			
1	0	0	When YFLAG=LOW on YFCLK input falling edge		- By status read (90H command)
2		1	When YFLAG=LOW on YFCLK input rising edge		- When MSON=LOW
3	1	0	When YFLAG=LOW	YFCLK be tied either High or Low	- After system reset
4		1	When YFLAG=HIGH		

Table 1. YFLAG signal check method

Compare-connect sequence

The SM5907AF supports three kinds of connect modes; 3-pair compare-connect, 2-pair compare-connect and direct connect.

Note that the SM5907AF can also operate in 12-bit comparison connect mode using only the most significant 12 bits of data for connection operation.

In 3-pair compare-connect mode, the final 6 valid data (3 pairs of left- and right-channel data input before encode processing) and the most recently input data are compared until three continuous data pairs all conform. At this point, the encode sequence is re-started and data is written to VWA.

In 2-pair compare-connect mode, comparison occurs just as for 3-pair comparison except that only 2 pairs from the three compared need to conform with the valid data. At this point, the encode sequence is re-started and data is written to VWA.

In direct-connect mode, comparison is not performed at all, and encode sequence starts and data is written to the VWA. This mode is for systems that cannot perform compare-connect operation.

- Compare-connect preparation time

1. Comparison data preparation time

Internally, when the compare-connect start command is issued, a sequence starts to restore the data for comparison. The time required for this preparation after receiving the command is approximately 2.5 × (1/fs). (approximately 60 µs when fs = 44.1 kHz)

2. After the above preparation is finished, data is input beginning from the left-channel data and comparison starts.

3. If the compare-connect command is issued again, the preparation time above is not necessary and operation starts from step 2.

4. The same sequence takes place in direct-connect mode also. However, at the point when 3 words have been input, all data is directly connected as if comparison and conformance had taken place.

- Compare-connect sequence stop

If a compare-connect stop command (80H with MSDCN1= 1, MSDCN2= 0) is input from the microcontroller, compare-connect sequence stops.

If compare-connect sequence was not operating, the compare-connect stop command performs no operation. However, make sure that the other bit settings within the same 80H command are valid.

Encode sequence temporary stop

- When RAM becomes full, MSWREN is set LOW using the 80H command and encode sequence stops. (For details of the stop conditions, refer to the description of the ENCOD flag.)

- Then, if MSWREN is set HIGH without issuing a compare-connect start command, the encode sequence re-starts. At this time, new input data is written not to VWA, but to WA. In this way, the data already written to the region between VWA and WA is not lost.

- But if the MSWREN is set HIGH (80H command) after using the compare-connect start command even only once, data is written to VWA. If data is input before comparison and conformance is detected, the same operation as direct-connect mode takes place when the command is issued. After comparison and conformance are detected, no operation is performed because the encode sequence has already been started. However, make sure that the other bit settings within the same 80H command are valid.

DRAM refresh

- DRAM initialization refresh

A 15-cycle RAS-only refresh is carried out for DRAM initialization under the following conditions.

When MSON changes from 0 to 1 using command 80H.

When from MSON=1, MSRDEN=0 and MSWREN=0 states only MSWREN changes to 1. In this case, encode sequence immediately starts and initial data is written (at 2fs rate input) after a delay of 0.7ms.

- Refresh during Shock-proof mode operation

In this IC, a data access operation to any address also serves as a data refresh. Accordingly, there are no specific refresh cycles other than the initialization refresh cycle (described above).

This has the resulting effect of saving on DRAM power dissipation.

A data access to DRAM can occur in an encode sequence write operation or in a decode sequence read operation. Write sequence write operation stops during a connect operation whereas a read sequence read operation always continues while data is output to the D/A. The refresh rate for each DRAM during decode sequence is shown in the table below.

The decode sequence, set by MSON=1 and MSRDEN=1, operates when valid data is in DRAM (when MSEMP=0).

- When MSON=0, DRAM is not refreshed because no data is being accessed. Although MSON=1, DRAM is not refreshed if ENCOD=0 and DECOD=0 (both encode and decode sequence are stopped).

	DRAMs used (same for 1 or 2 DRAMs)	
Data compression mode	4M (1M×4 bits)	16M(4M×4 bits)
4 bit	10.88 ms	21.77ms
5 bit	8.71 ms	17.42ms
6 bit	7.26 ms	14.52ms
Full bit	2.72 ms	5.81ms

Table 2. Decode sequence refresh rate

Through-mode operation

If MSON is set LOW (80H command), an operating mode that does not perform shock-proof functions becomes active. In this case, input data is passed as-is (except Force mute operation) to the output. External DRAM is not accessed.

- In this case, input data needs to be at a rate fs and the input word clock must be synchronized to the CLK input (384fs). However, short-range jitter can be tolerated (jitter-free system).

- Jitter-free system timing starts from the first YLRCK rising edge after either (A) a reset (NRESET= 0) release by taking the reset input from LOW to HIGH or (B) by taking MSON from HIGH to LOW. Accordingly, to provide for the largest possible jitter margin, it is necessary that the YLRCK clock be at rate fs by the time jitter-free timing starts.

The jitter margin is 0.2/ fs (80 clock cycles).

This jitter margin is the allowable difference between the system clock (CLK) divided by 384 (fs rate clock) and the YLRCK input clock.

If the timing difference exceeds the jitter margin, irregular operation like data being output twice or, conversely, incomplete data output may occur. In the worst case, a click noise may also be generated.

When switching from shock-proof mode to through mode, an output noise may be generated, and it is therefore recommended to use the YDMUTE setting to mute ZSRDATA until just before data output.

Force mute

Serial output data is muted by setting the YDMUTE pin input HIGH or by setting the MUTE flag to 1. Mute starts and finishes on the leading left-channel bit.

When MSON is HIGH and valid data is empty (MSEMP=H), the output is automatically forced into the mute state.

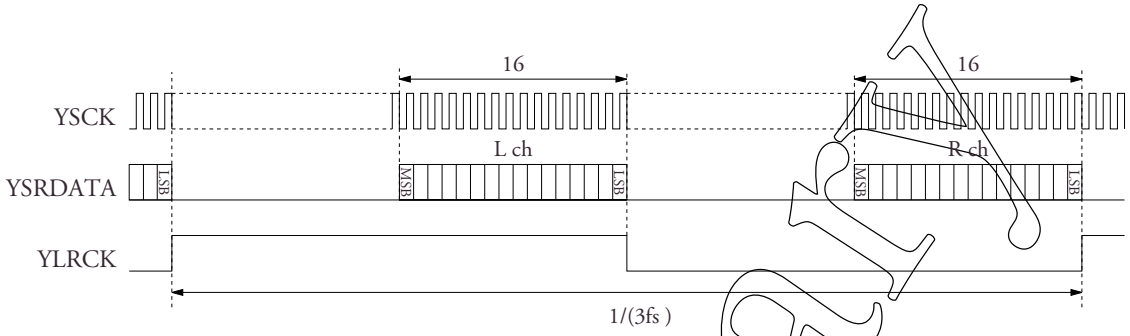
12-bit comparison connection

When the CMP12 flag is set to 1, the least significant 4 bits of the 16-bit comparison connection input data are discarded and comparison connection is performed using the remaining 12 bits.

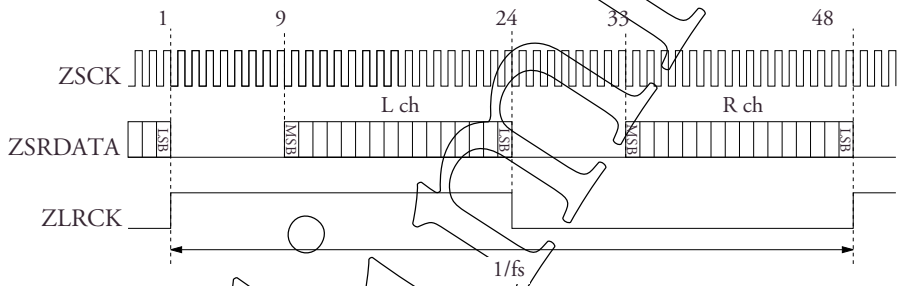
Note that if the CMP12 flag is set to 1 during a comparison connection operation, only the most significant 12 bits are used for comparison connection from that point on.

Timing charts

Input timing (YSCK, YSRDATA, YLRCK)

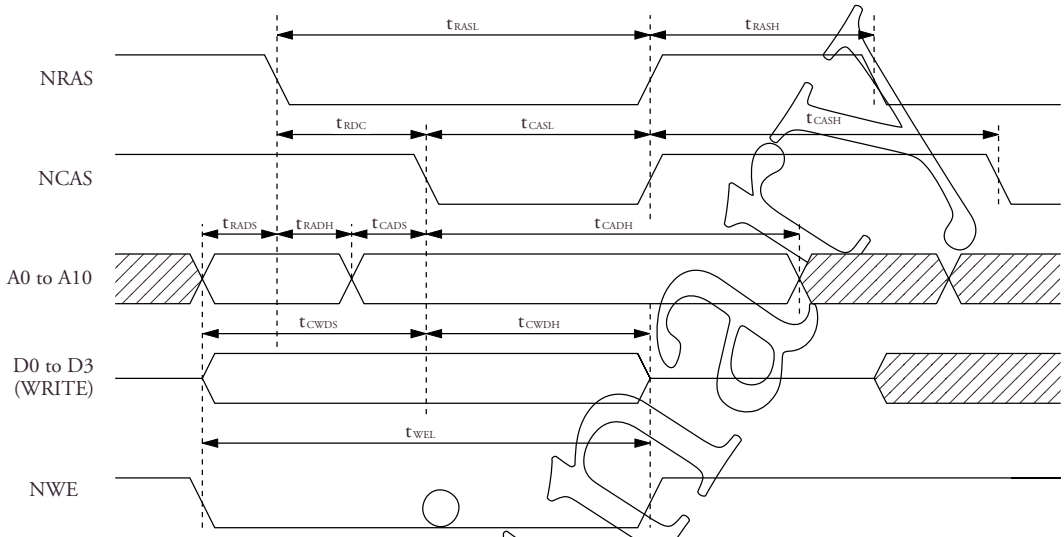


Output timing (ZSCK, ZSRDATA, ZLRCK)

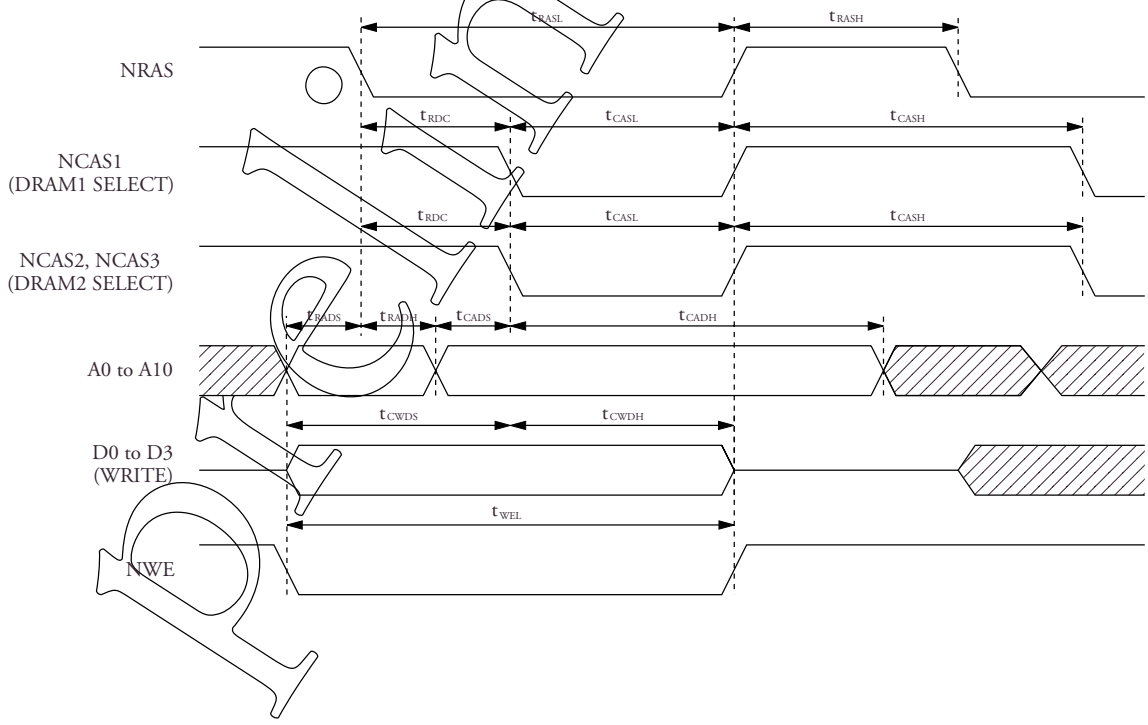


DRAM write timing (NRAS, NCAS, NCAS2, NCAS3, NWE, A0 to A10, D0 to D3)

Write timing (with single DRAM)

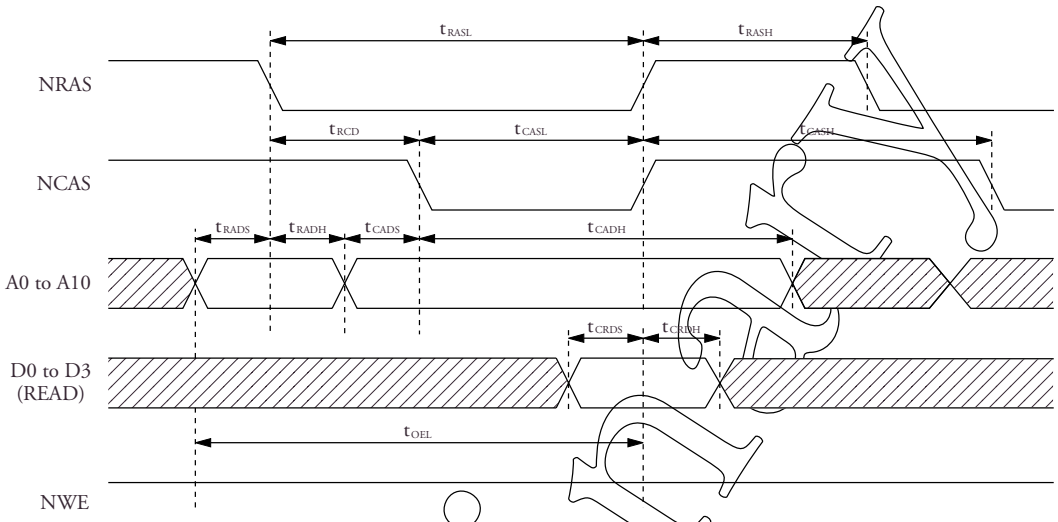


Write timing (with double DRAMs)

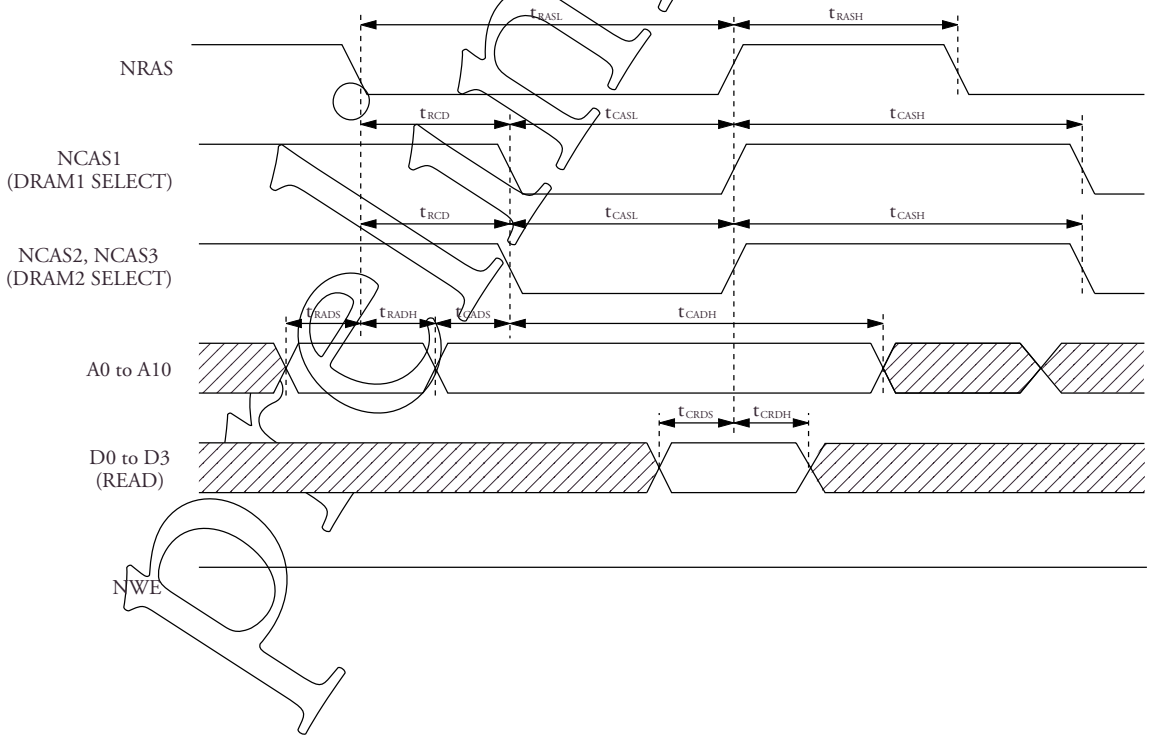


DRAM read timing (NRAS, NCAS, NCAS2, NCAS3, NWE, A0 to A10, D0 to D3)

Read timing (with single DRAM)

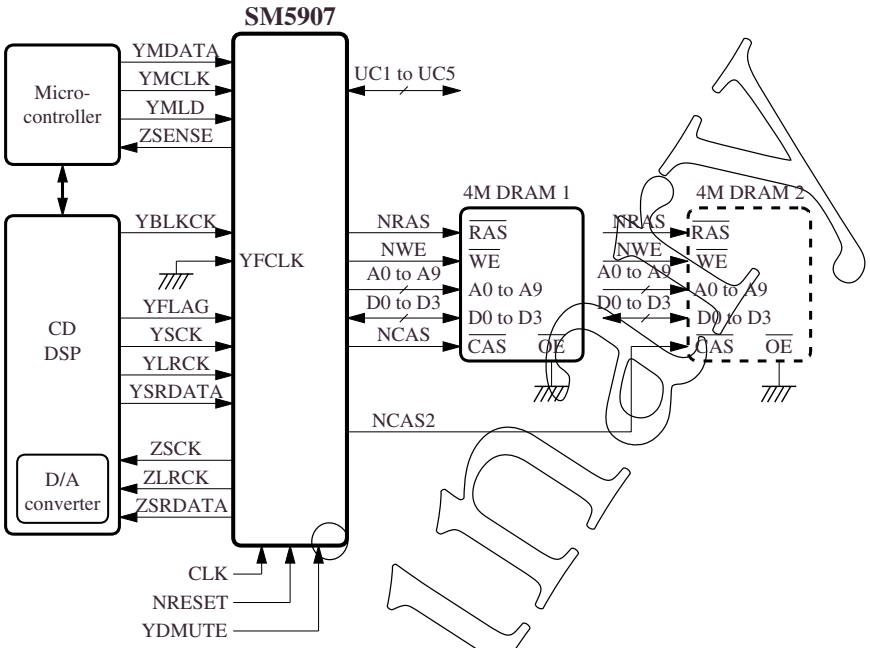


Read timing (with double DRAMs)

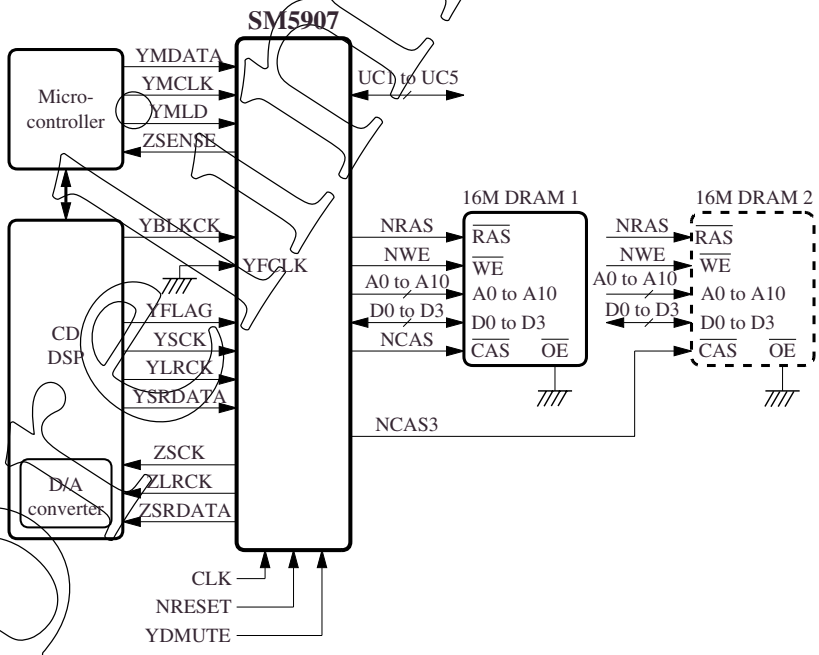


Connection example

4M DRAM × 1 or 2 typical connection



16M DRAM × 1 or 2 typical connection



DRAM $\overline{OE}$ pin is tied LOW.

In response to the YFLAG input, the 85H command (option settings) should be:

D5: YFLGS =1, D4: YFCKP set to the YFLAG active level.

If YFLAG is active LOW, set YFCKP=0. If YFLAG is active HIGH, set YFCKP=1.

If 4M DRAM × 2 are used, use A10/NCAS2 pin.

If 16M DRAM × 2 are used, use NCAS3 pin.

Device comparison with SM5903BF

Pin difference

Pin No.	SM5903BF	SM5907AF
7 pin	N.C.	NCAS3

Microcontroller interface functions

85H (RAMS1=0, RAMS2=0)

SM5903BF: 1M DRAM × 1

SM5907AF: 16M DRAM × 2

92H (valid residual)

In the SM5907AF, if 16M DRAM × 2 configuration is selected using the 85H command (85H RAMS1=0, RAMS2=0), the residual data is 1-bit shifted in order to represent the maximum 32Mbits.

As pin 7 on the SM5903BF is not connected internally, the possible DRAM configurations are 4M × 1, 4M × 2, and 16M × 1, all of which are completely compatible with the SM5907AF.

Note that the chip process is different, and hence some DC characteristics are different.

When 16M × 2 configuration is used, the microcontroller interface valid residual memory is different (92H status read). See "Read command summary".

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