OVERVIEW

The SM5953A is a dedicated surround effects processor LSI that has a function that adds surround effects to digital audio signals. The surround effects can be varied continuously from the microcontroller interface. It also features a built-in power-down function for low power dissipation in standby mode.

FEATURES

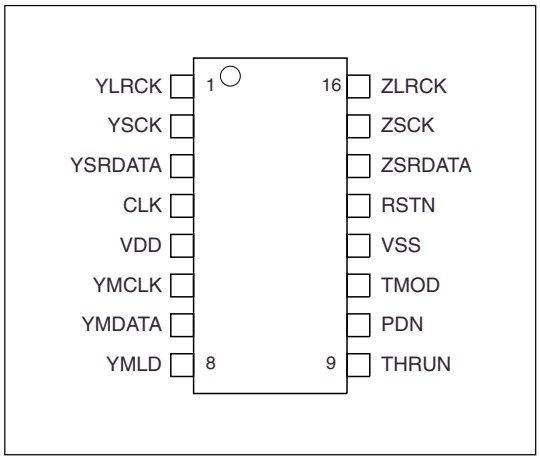
- Left/Right-channel processing (stereo)
- Serial data input
  2s-complement, 16-bit MSB-first, right-justified format
- System clock input: 384fs (16.9344MHz)
- Microcontroller interface
  3-wire serial control
  Surround volume: Separate microcontroller interface controls for each parameter:
  - ATP : L + R component input attenuator
  - ATM : L – R component input attenuator
  - DS : Delay scaling
  - GP : L + R component gain
  - GM : L – R component gain
  - GPR : L + R component reverb gain
  - GMR : L – R component reverb gain
  - GO : Raw signal impressed gain
- Power-down function
- Direct mute function
- Data through-mode function
- 2.5V single voltage supply
- 16-pin VSOP package

ORDERING INFORMATION

Device	Package
SM5953AV	16-pin VSOP

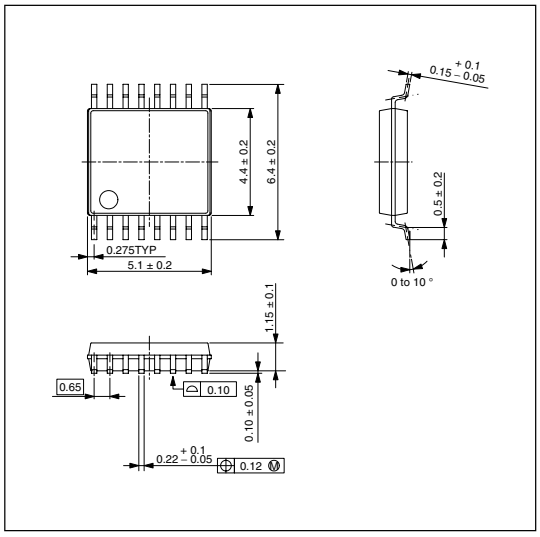
PINOUT

(Top view)



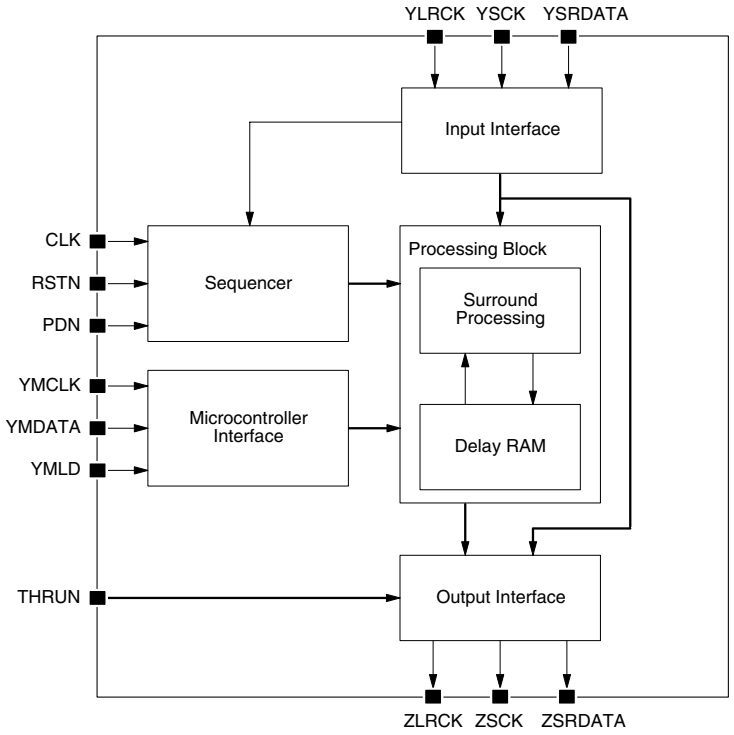
PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.070g



Note: Dimensions without tolerances are reference values only.

BLOCK DIAGRAM



PIN DESCRIPTION

No.	Name	I/O[1]	Function	HIGH	LOW
1	YLRCK	Is	Word clock input (fs)		
2	YSCK	Is	Bit clock input (32fs to 64fs)		
3	YSRDATA	Is	Data input		
4	CLK	I	System clock input		
5	VDD	–	2.5V supply		
6	YMCLK	Is	Microcontroller clock input		
7	YMDATA	Is	Microcontroller data input		
8	YMLD	Is	Microcontroller latch enable input		
9	THRUN	Is	Through-mode select		Through mode
10	PDN	Is	Power-down select		Power-down
11	TMOD	Isd	Test mode pin (tie LOW or leave open-circuit)	Test	Normal
12	VSS	–	0V supply ground		
13	RSTN	Is	Reset input		Reset
14	ZSRDATA	O[2]	Data output		
15	ZSCK	O[2]	Bit clock output (48fs fixed)		
16	ZLRCK	O[2]	Word clock output		

1. I = CMOS input, O = output, Is = Schmitt input, Isd = Schmitt input with pull-down
2. Outputs are pulled-down when PDN = LOW or RSTN = LOW

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to 3.6	V
Input voltage	V_I	–0.3 to 3.6	V
Output voltage	V_O	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	165	mW
Storage temperature	T_{STG}	–55 to 125	°C

Note. Ratings also apply when power is applied or disconnected.

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	2.25	2.5	2.75	V
Operating temperature	T_{OPR}	–40	25	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0V, V_{DD} = 2.25 to 2.75V, Ta = –40 to 85°C unless otherwise noted

Parameter	Pin	Symbol	Condition	Rating			Unit
				min	typ	max	
Current consumption	VDD	I_{DD}	(*A)	–	4.5	9.0	mA
Input voltage	(*1)	V_{IH}		0.8V_{DD}	–	V_{DD}	V
		V_{IL}		0	–	0.2V_{DD}	V
		V_{INAC}	AC coupling	0.4	–	–	V_{PP}
	(*2)(*3)	V_{IH}		0.8V_{DD}	–	V_{DD}	V
		V_{IL}		0	–	0.2V_{DD}	V
Output voltage	(*3)	V_{OH}	I_{OH} = –2.0mA	1.85	–	V_{DD}	V
		V_{OL}	I_{OL} = 2.0mA	0	–	0.4	V
Input leakage current	(*1)(*2)	I_{LH}	V_{IN} = V_{DD}	–10	–	10	µA
		I_{IH}	V_{IN} = V_{DD}	40	80	160	µA
		I_{LL}	V_{IN} = 0V	–10	–	10	µA

(*A): All outputs unloaded, system clock frequency F_{CLK} = 16.9344MHz, input word clock frequency F_{YLRCK} = 44.1kHz, supply voltage V_{DD} = 2.5V, V_{IH} = 0.8V_{DD} = 1.875V, V_{IL} = 0.2V_{DD} = 0.5V
Note. See pin classification table below.

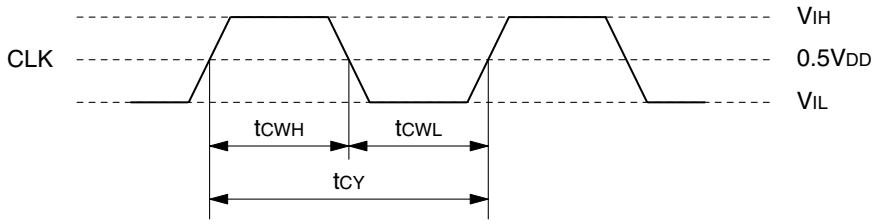
<Pin classification>

Symbol	Class	Pins
(*1)	Inputs	CLK
(*2)	Schmitt inputs	YLRCK, YSCK, YSRDATA, YMCLK, YMDATA, YMLD, RSTN, PDN, THRUN
(*3)	Inputs with pull-down	TMOD
(*4)	Outputs with pull-down	ZLRCK, ZSCK, ZSRDATA (Outputs are pulled-down when PDN = LOW or RSTN = LOW only)

AC Characteristics

System clock (CLK)

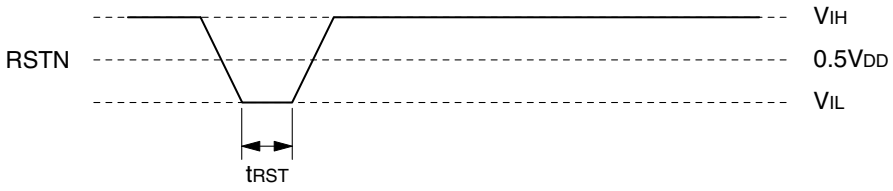
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock pulse cycle time	t_{CY}		54	59	65.1	ns
HIGH-level clock pulsewidth	t_{CWH}	t_{CY} = 59ns	21.6	–	39.1	ns
LOW-level clock pulsewidth	t_{CWL}	t_{CY} = 59ns	21.6	–	39.1	ns
Clock pulse duty			40	–	60	%



Reset (RSTN)

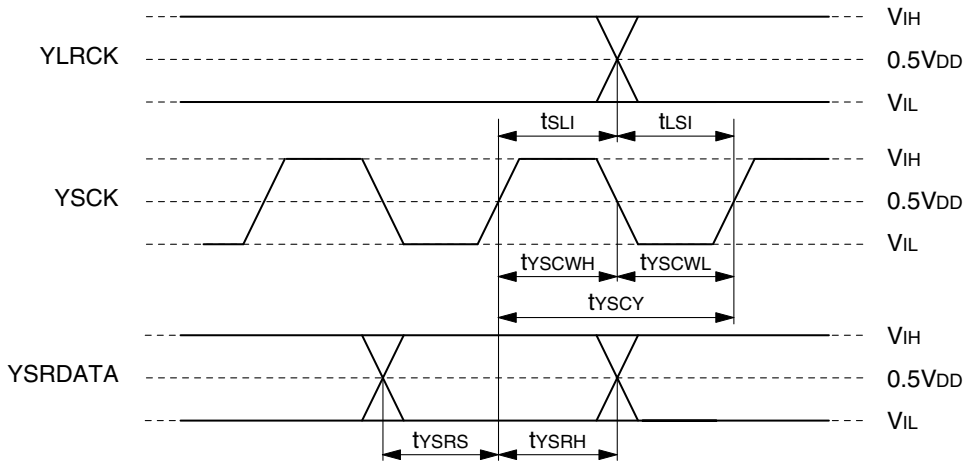
Parameter	Symbol	Condition	Rating			Unit[1]
			min	typ	max	
RSTN pulsewidth	t_{RST}		4	–	–	t_{CY}

1. t_{CY} is the system clock cycle time of 59ns (typ).



Serial inputs (YLRCK, YSCK, YSRDATA)

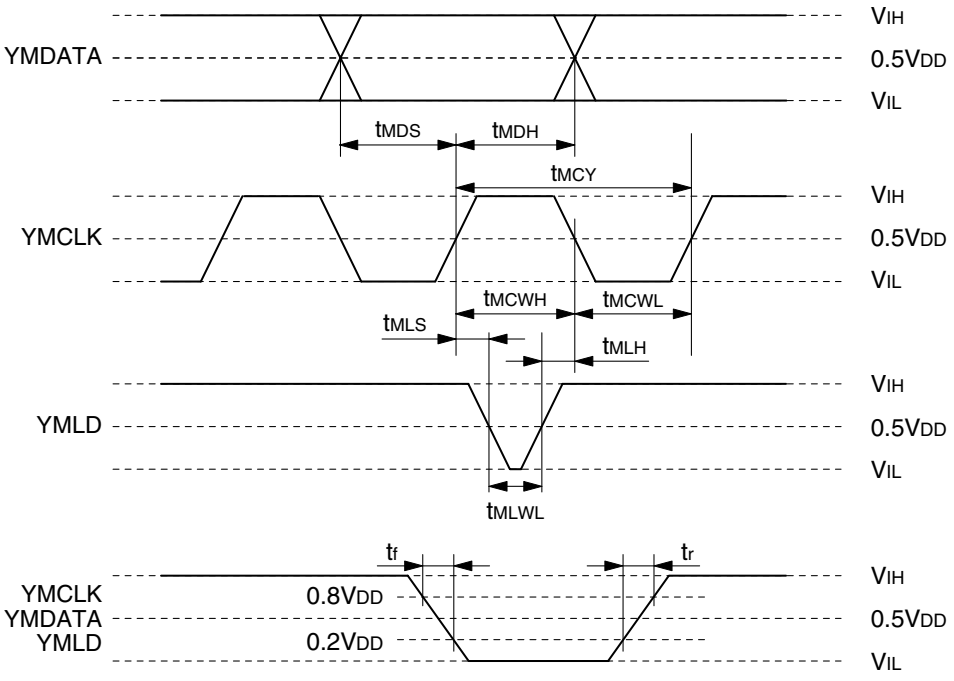
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
YLRCK cycle time	t_{YLCY}		20.8	–	25	µs
YSCK pulse cycle time	t_{YSCY}		324	–	390.6	ns
YSCK HIGH-level pulsewidth	t_{YSCWH}		160	–	–	ns
YSCK LOW-level pulsewidth	t_{YSCWL}		160	–	–	ns
YSRDATA setup time	t_{YSRS}		80	–	–	ns
YSRDATA hold time	t_{YSRH}		80	–	–	ns
Last YSCK rising edge → YLRCK edge	t_{SLI}		80	–	–	ns
YLRCK edge → first YSCK rising edge	t_{LSI}		80	–	–	ns



Microcontroller interface (YMCLK, YMDATA, YMLD)

Parameter	Symbol	Condition	Rating			Unit
			min[1]	typ	max	
YMCLK cycle time	t_{MCY}		$60 + 4t_{CY}$	–	–	ns
YMCLK HIGH-level pulsewidth	t_{MCWH}		$30 + 2t_{CY}$	–	–	ns
YMCLK LOW-level pulsewidth	t_{MCWL}		$30 + 2t_{CY}$	–	–	ns
YMDATA setup time	t_{MDS}		$30 + t_{CY}$	–	–	ns
YMDATA hold time	t_{MDH}		$30 + t_{CY}$	–	–	ns
YMLD LOW-level pulsewidth	t_{MLWL}		$30 + 2t_{CY}$	–	–	ns
YMLD setup time	t_{MLS}		$30 + t_{CY}$	–	–	ns
YMLD hold time	t_{MLH}		$30 + t_{CY}$	–	–	ns
Rise time	t_r		–	–	100	ns
Fall time	t_f		–	–	100	ns

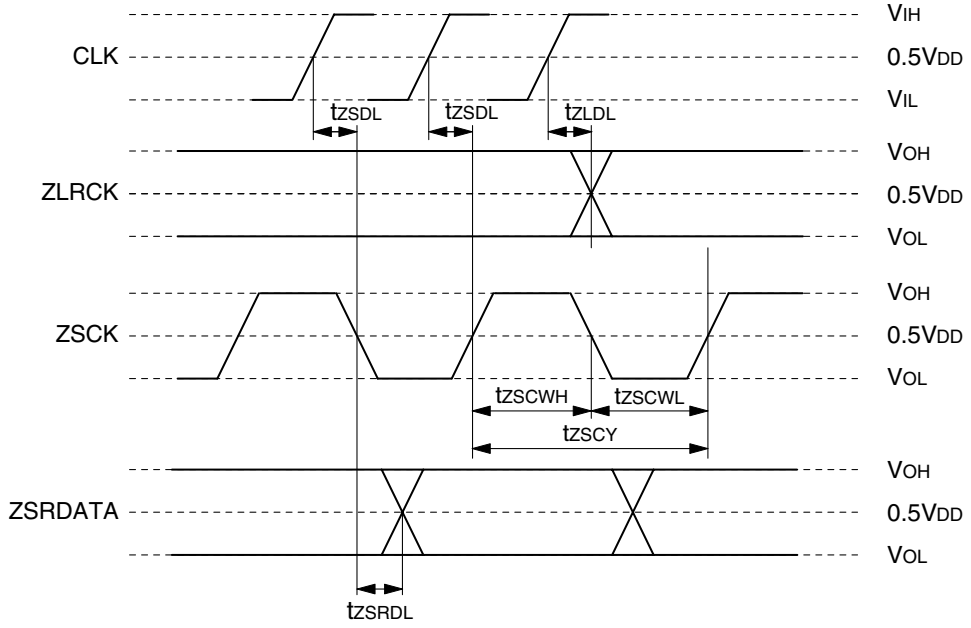
1. t_{CY} is the system clock cycle time of 59ns (typ).



Serial outputs (ZLRCK, ZSCK, ZSRDATA)

Parameter	Symbol	Condition	Rating			Unit[1]
			min	typ	max	
ZLRCK cycle time	t_{ZLCY}		–	384	–	t_{CY}
ZLRCK HIGH-level pulsewidth	t_{ZLCWH}		–	192	–	t_{CY}
ZLRCK LOW-level pulsewidth	t_{ZLCWL}		–	192	–	t_{CY}
ZSCK pulse cycle time	t_{ZSCY}		–	8	–	t_{CY}
ZSCK HIGH-level pulsewidth	t_{ZSCWH}		–	4	–	t_{CY}
ZSCK LOW-level pulsewidth	t_{ZSCWL}		–	4	–	t_{CY}
ZSCK output delay	t_{ZSDL}	C_L = 15pF	–	–	30	ns
ZLRCK output delay	t_{ZLDL}	C_L = 15pF	–	–	30	ns
ZSRDATA output delay	t_{ZSRDL}	C_L = 15pF	–	–	30	ns

1. t_{CY} is the system clock cycle time of 59ns (typ).

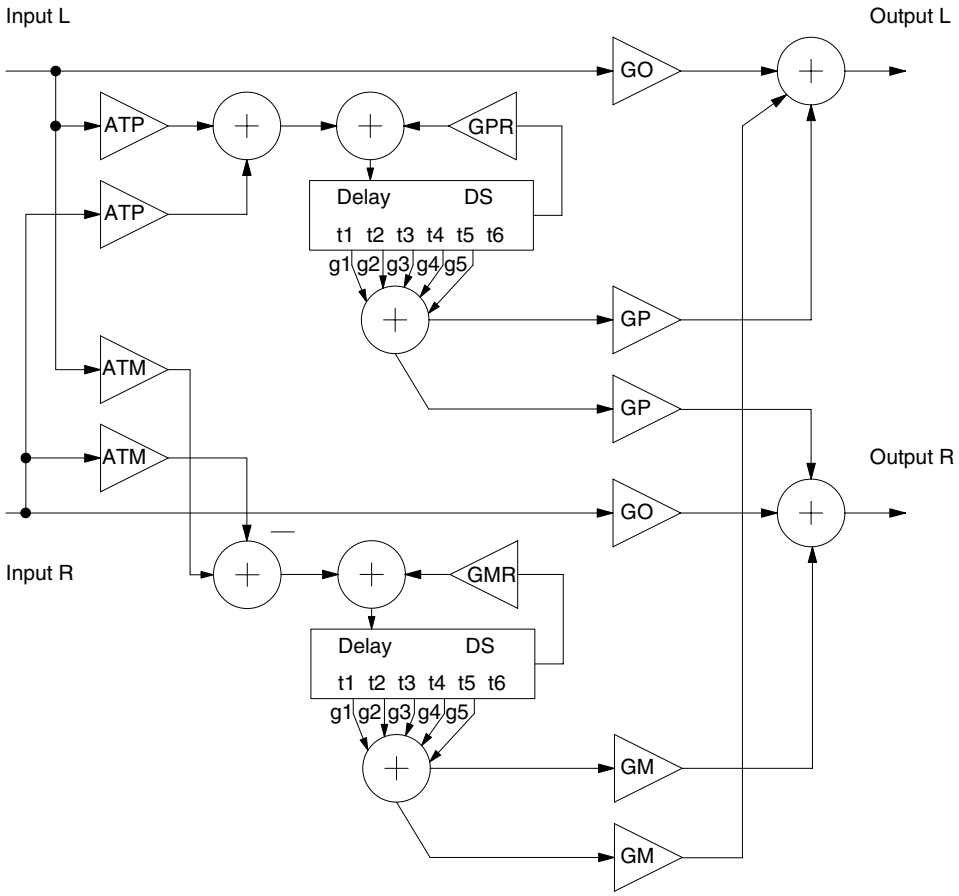


FUNCTIONAL DESCRIPTION

Surround Function

The SM5953A adds reflected sound components, internally delayed signals stored in SRAM, to the raw data direct sound components in order to achieve surround sound effects. The L + R and L – R reflected sound components are read out from the address determined by the delay scaling value set over the microcontroller interface, multiplied by a gain factor likewise set over the microcontroller interface, and then added to the direct sound components. The following 8 parameters can be controlled using the microcontroller interface.

- L + R component input attenuator ATP : 0 to 255/1 step
- L – R component input attenuator ATM : 0 to 255/1 step
- Delay scaling parameter DS : 0 to 14/1 step
- L + R component gain parameter GP : 0 to 1.875/0.125 step
- L – R component gain parameter GM : 0 to 1.875/0.125 step
- L + R component reverb gain parameter GPR : 0 to 1.875/0.125 step
- L – R component reverb gain parameter GMR : 0 to 1.875/0.125 step
- Raw signal impressed gain parameter GO : 0 to 1.875/0.125 step

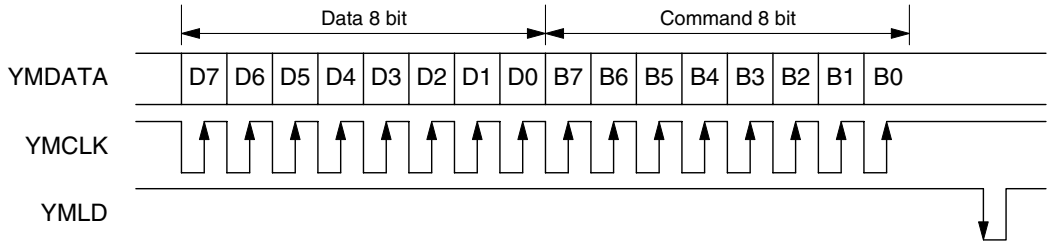


Microcontroller Interface (YMDATA, YMCLK, YMLD)

The SM5953A is controlled using commands issued over the microcontroller interface.

Command format

Commands from the microcontroller are input in bit serial format over a 3-wire interface comprising a data input (YMDATA), bit clock (YMCLK), and load signal latch enable input (YMLD). The write command format for commands A0 to A5 is shown below.



Register table

■ Command A0

Bit	Flag name	Description	Default
D7	ATP7	ATP7 to ATP0: L + R component input attenuator parameter Attenuation = $20 \times \log_{10}(ATP/256)$ [dB] "1111 1111" → –0.03dB "1000 0000" → –6.02dB "0000 0001" → –48.16dB "0000 0000" → –∞dB	0
D6	ATP6		1
D5	ATP5		0
D4	ATP4		1
D3	ATP3		0
D2	ATP2		0
D1	ATP1		0
D0	ATP0		0

■ Command A1

Bit	Flag name	Description	Default
D7	ATM7	ATM7 to ATM0: L – R component input attenuator parameter Attenuation = $20 \times \log_{10}(ATM/256)$ [dB] "1111 1111" → –0.03dB "1000 0000" → –6.02dB "0000 0001" → –48.16dB "0000 0000" → –∞dB	0
D6	ATM6		1
D5	ATM5		0
D4	ATM4		1
D3	ATM3		0
D2	ATM2		0
D1	ATM1		0
D0	ATM0		0

■ Command A2

Bit	Flag name	Description	Default
D7	DS3	DS3 to DS0: Delay scaling parameter[1] "0000" → × 1 "0001" → × 2 "1110" → × 14 "1111" (F hex) is prohibited.	1
D6	DS2		0
D5	DS1		1
D4	DS0		0
D3	GO3	GO3 to GO0: Raw component gain parameter "0000" → × 0.0 "0001" → × 0.0625 "1111" → × 0.9375	0
D2	GO2		1
D1	GO1		0
D0	GO0		1

1. When switching DS, the difference in delay signal level may be audible. In dynamically-switching applications, the system outputs should be muted.

■ Command A3

Bit	Flag name	Description	Default
D7	GP3	GP3 to GP0: L + R component gain parameter "0000" → × 0.0 "0001" → × 0.125 "1111" → × 1.875	0
D6	GP2		1
D5	GP1		1
D4	GP0		0
D3	GM3	GM3 to GM0: L – R component gain parameter "0000" → × 0.0 "0001" → × 0.125 "1111" → × 1.875	1
D2	GM2		1
D1	GM1		0
D0	GM0		0

■ Command A4

Bit	Flag name	Description	Default
D7	GPR3	GPR3 to GPR0: L + R component reverb gain parameter "0000" → × 0.0 "0001" → × 0.125 "1111" → × 1.875	0
D6	GPR2		1
D5	GPR1		0
D4	GPR0		0
D3	GMR3	GMR3 to GMR0: L – R component reverb gain parameter "0000" → × 0.0 "0001" → × 0.125 "1111" → × 1.875	0
D2	GMR2		1
D1	GMR1		0
D0	GMR0		0

■ Command A5

Bit	Flag name	Description	Default
D7	DMUTE	Direct mute flag (HIGH → mute)	0
D6	PDN	Power-down flag (LOW → power-down)	1
D5	THRUN	Through-mode flag (LOW → through mode)	1
D4	–		0
D3	TEST3	Test mode setting (set LOW for normal operation)	0
D2	TEST2	Test mode setting (set LOW for normal operation)	0
D1	TEST1	Test mode setting (set LOW for normal operation)	0
D0	TEST0	Test mode setting (set LOW for normal operation)	0

Direct Mute (DMUTE Flag)

The SM5953A can directly mute the outputs by setting the microcontroller interface DMUTE flag to 1. In direct muting, the outputs are muted starting from the word synchronized to the next ZLRCK clock rising edge after the DMUTE flag is set to 1. Similarly, direct muting is released starting from the word synchronized to the next ZLRCK clock rising edge after the DMUTE flag is set to 0. When direct muting is selected, the device is simultaneously initialized and delay memory data is cleared. The initialization operation takes 128/fs time (2.902ms @ 44.1kHz).

Power-Down (PDN Pin and PDN Flag)

The SM5953A can power-down either by setting the PDN input LOW or by setting the microcontroller interface PDN flag to 0. At power-down, all circuit internal signals stop (with the exception of the microcontroller interface circuits) and the outputs are tied LOW to suppress power consumption. When power-down is selected or released, the system outputs should also be muted to prevent noise from occurring. Power-down should be selected only after muting is selected, and muting should be released only after power-down is released. When power-down is released, the initialization sequence becomes active and all internal SRAM data is cleared. The YLRCK, YSCK, and CLK input clocks must also be supplied and stable for the initialization sequence to operate when power-down is released.

Through-Mode (THRUN Pin and THRUN Flag)

The SM5953A can take the input signals (YLRCK, YSCK, YSRDATA) and pass them directly to the outputs (ZLRCK, ZSCK, ZSRDATA) either by setting the THRUN input LOW or by setting the microcontroller interface THRUN flag to 0. In through mode, all circuits stop (except for the connection from inputs to outputs and the microcontroller interface), reducing the power consumption to a minimum. When returning from through mode to normal mode of operation, the initialization sequence for all circuits becomes active and internal SRAM data is cleared. The YLRCK, YSCK, and CLK input clocks must also be supplied and stable for the initialization sequence to operate when through mode is released.

Note: When switching between through mode and normal mode, YLRCK and ZLRCK become discontinuous and an output noise may occur. Consequently, the system outputs should be muted.

System Reset (RSTN Pin)

At power-ON, the SM5953A must be reset. The device is reset by applying a LOW-level pulse on the RSTN input. When the supply voltage is stable and the YLRCK, YSCK, CLK clocks are stable, system reset is released by taking RSTN from LOW to HIGH. If YLRCK, YSCK, or CLK stop during normal operation, a system reset must be performed after the clocks have restabilized. When the system reset is released, the initialization sequence operates and the internal SRAM data is cleared. The initialization operation takes 128/fs time (2.902ms @ 44.1kHz).

TIMING DIAGRAMS

Input Timing (YLRCK, YSCK, YSRDATA)

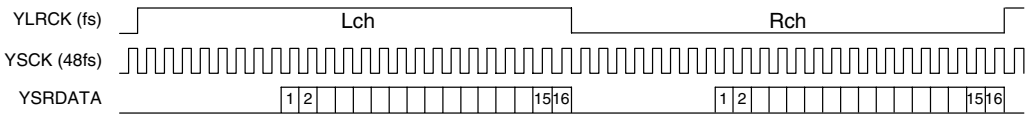


Figure 1. 16-bit MSB-first right-justified (BCKI = 32fs to 64fs)

Output Timing (ZLRCK, ZSCK, ZSRDATA)

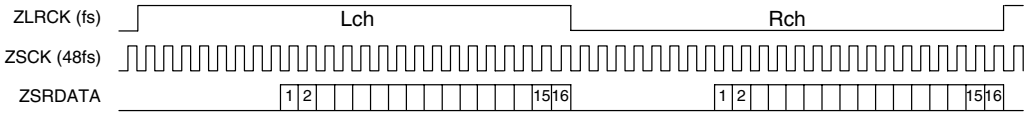
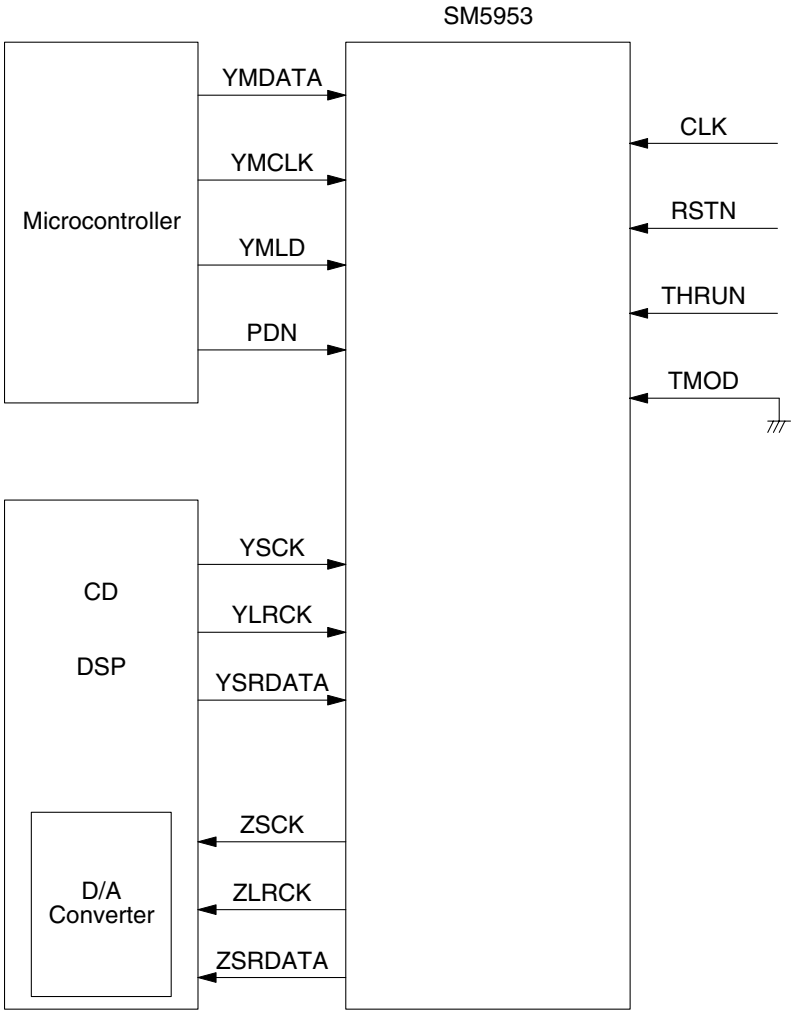


Figure 2. 16-bit MSB-first right-justified (BCKI = 48fs fixed)

TYPICAL APPLICATION CIRCUIT

Typical Connection



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NC0321BE 2006.04