NPC

SM5351AF1

Audio Video Switch

OVERVIEW

The SM5351AF1 is an Audio Video (AV) switch with built-in 4-system CVBS input switch, 2-system S-video input switch, 2-system component video input switch, and 5-system audio switch. It has built-in 8-system cable connecting discriminator function, 2-system S2 discriminator function, and 1-system D-terminal discriminator function, and these discriminated status can read via I^2C-BUS*1. The input switching and output muting function can be controlled individually for each block using the I^2C-BUS. The I^2C-BUS slave address is set using the ADS pin, allowing a maximum of two SM5351AF1 devices to be controlled simultaneously.

*1. I^2C-BUS is a registered trademark of NXP B.V.

FEATURES

- Supply voltages
  - Video block: 4.75 to 5.25V
  - Audio block: 8.0 to 10.0V
- 4-system input/1-system output: CVBS input switch
- 2-system input/1-system output: S-video input switch
- 2-system input/1-system output: Component video input switch
  - Passband: 80MHz (typ)
- Output muting function
- 5-system input/1-system output: Stereo audio input switch
  - Maximum input level: $2.1V_{RMS}$ (THD < 1%)
- 8-system cable connecting discriminator function built-in
  (4-system for CVBS, 2-system for S-video, 2-system for D-terminal)
- 2-system S2 discriminator function built-in
- 1-system D-terminal discriminator function built-in
- I/O pins for I^2C-BUS (SCL, SDA) are maintain high-impedance when power supply (V_{CC}, V_{DD}) goes OFF
- Slave address: 90h, 92h (selected by ADS input)
- Operating ambient temperature range: –20 to 70°C
- Package: 64-pin LQFP

APPLICATIONS

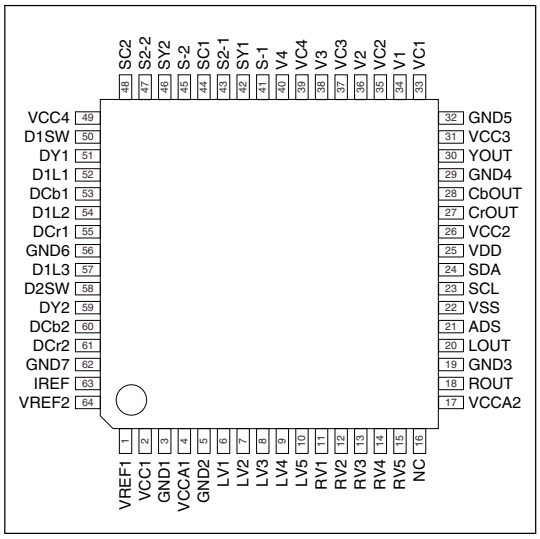
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5351AF1	64-pin LQFP

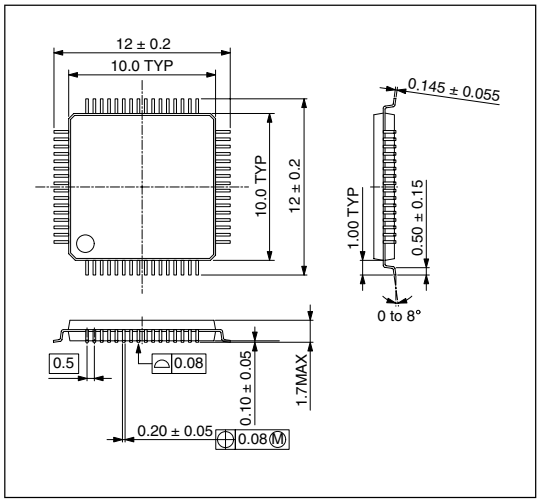
PINOUT

(Top view)

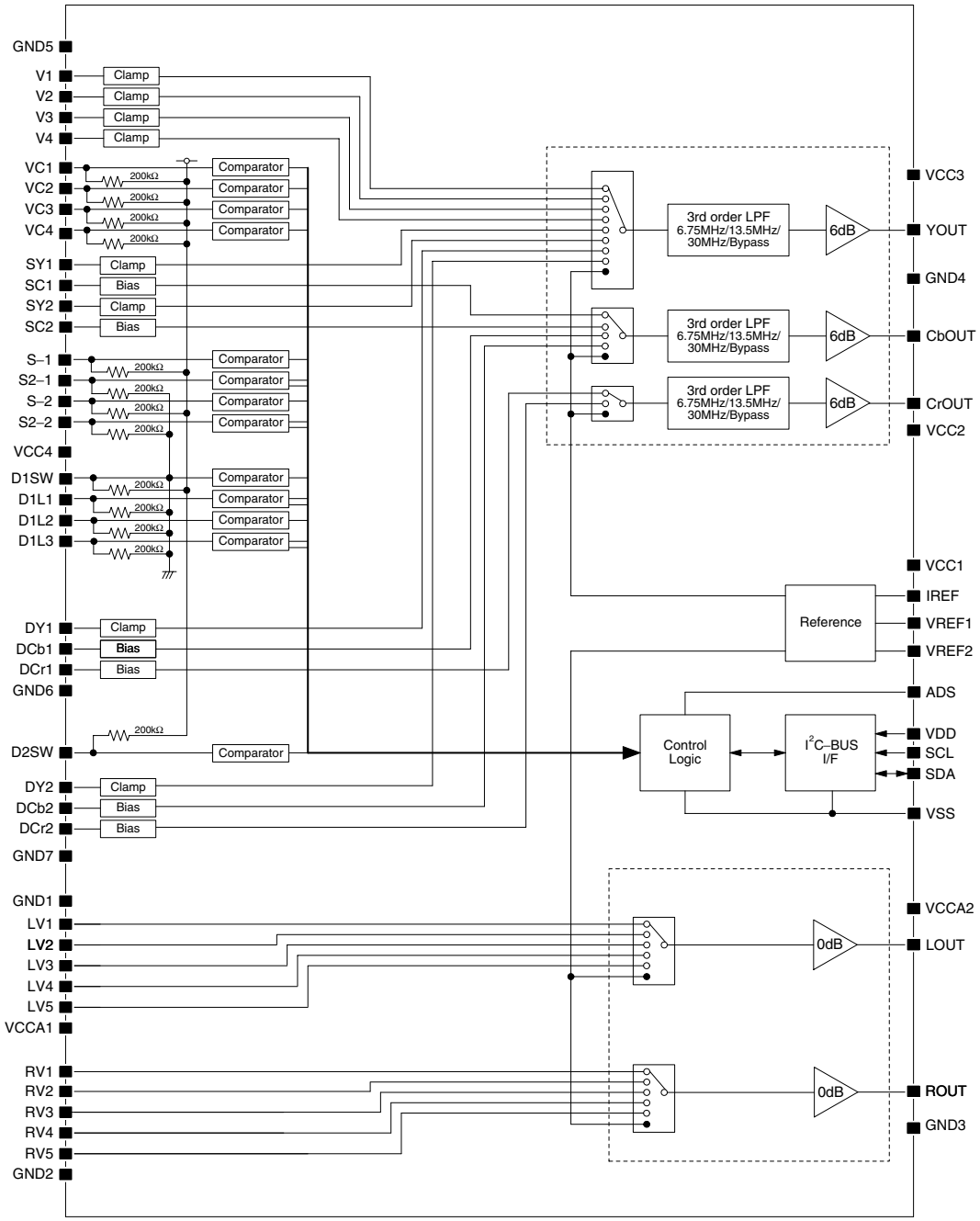


PACKAGE DIMENSION

(Unit: mm)



BLOCK DIAGRAM



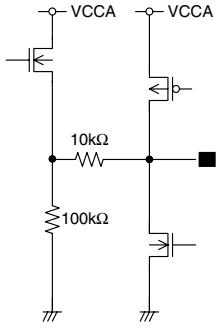
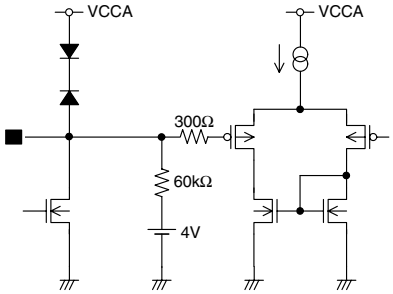
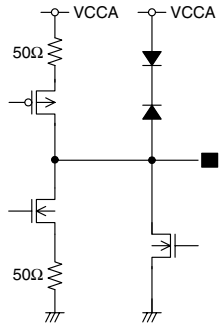
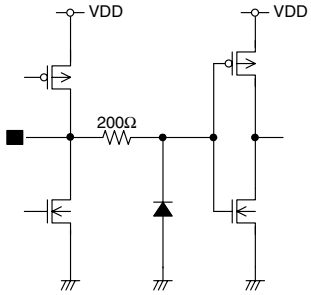
PIN DESCRIPTION

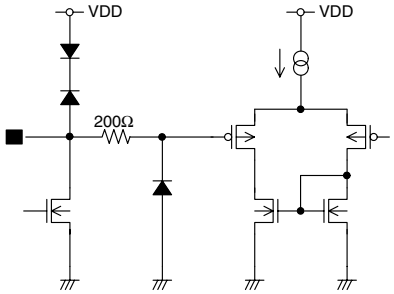
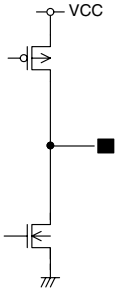
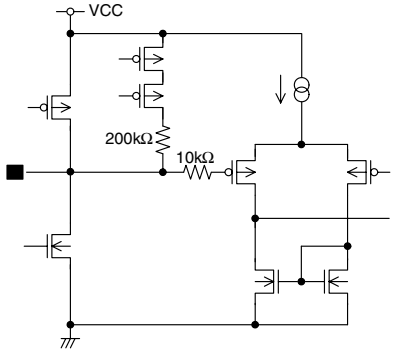
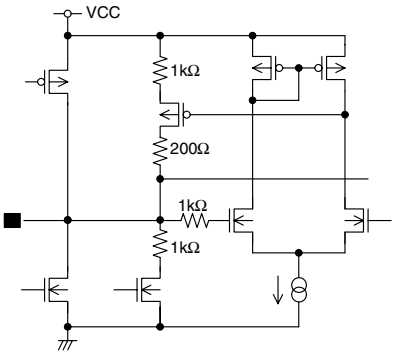
Number	Name	I/O*1	A/D*2	Description
1	VREF1	O	A	Internal reference voltage pin 1 (audio block)
2	VCC1	P	A	Video block supply pin 1
3	GND1	GND	A	Analog ground pin 1
4	VCCA1	P	A	Audio block supply pin 1
5	GND2	GND	A	Analog ground pin 2
6	LV1	I	A	L-channel audio input pin 1
7	LV2	I	A	L-channel audio input pin 2
8	LV3	I	A	L-channel audio input pin 3
9	LV4	I	A	L-channel audio input pin 4
10	LV5	I	A	L-channel audio input pin 5
11	RV1	I	A	R-channel audio input pin 1
12	RV2	I	A	R-channel audio input pin 2
13	RV3	I	A	R-channel audio input pin 3
14	RV4	I	A	R-channel audio input pin 4
15	RV5	I	A	R-channel audio input pin 5
16	NC	–	–	No connection
17	VCCA2	P	A	Audio block supply pin 2
18	ROUT	O	A	R-channel audio output pin
19	GND3	GND	A	Analog ground pin 3
20	LOUT	O	A	L-channel audio output pin
21	ADS	I	D	Address select pin. Select the I^2C-BUS slave address. (L: 90h/91h, H: 92h/93h)
22	VSS	GND	D	Digital ground pin
23	SCL	I	D	I^2C-BUS clock signal pin. Connect pull-up to supply line of I^2C-BUS. The SM5351AF1 corresponds to the I^2C-BUS of 2.7V to 3.6V supply voltage.
24	SDA	I/O	D	I^2C-BUS data signal pin. Connect pull-up to supply line of I^2C-BUS. The SM5351AF1 corresponds to the I^2C-BUS of 2.7V to 3.6V supply voltage. The output is open-drain.
25	VDD	P	D	I^2C-BUS interface-stage supply pin
26	VCC2	P	A	Video block supply pin 2
27	CrOUT	O	A	Component video output pin 1 (Cr)
28	CbOUT	O	A	Component video output pin 1 (Cb)
29	GND4	GND	A	Analog ground pin 4
30	YOUT	O	A	Component video output pin 1 (Y)
31	VCC3	P	A	Video block supply pin 3
32	GND5	GND	A	Analog ground pin 5
33	VC1	I	D	Composite video signal connecting discriminator input pin 1
34	V1	I	A	Composite video signal input pin 1
35	VC2	I	D	Composite video signal connecting discriminator input pin 2
36	V2	I	A	Composite video signal input pin 2
37	VC3	I	D	Composite video signal connecting discriminator input pin 3

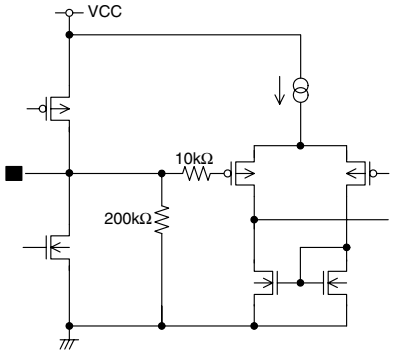
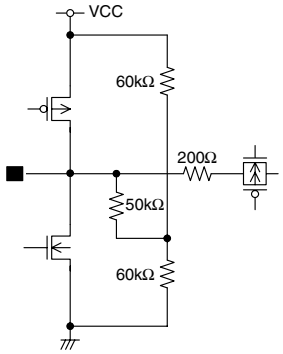
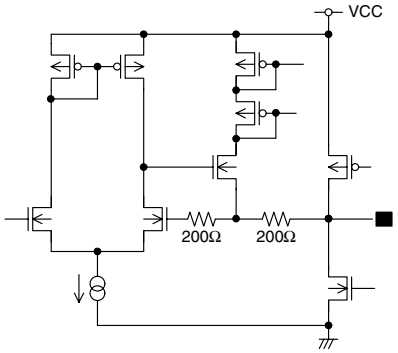
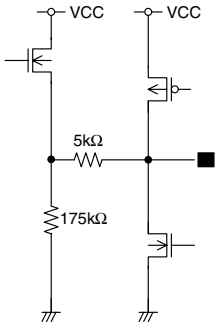
Number	Name	I/O*1	A/D*2	Description
38	V3	I	A	Composite video signal input pin 3
39	VC4	I	D	Composite video signal connecting discriminator input pin 4
40	V4	I	A	Composite video signal input pin 4
41	S-1	I	D	S-video terminal connecting discriminator pin 1
42	SY1	I	A	S-video signal input pin 1 (Y)
43	S2-1	I	A	S2 signal discriminator input pin 1. 3-state input
44	SC1	I	A	S-video signal input pin 1 (C)
45	S-2	I	D	S-video terminal connecting discriminator pin 2
46	SY2	I	A	S-video signal input pin 2 (Y)
47	S2-2	I	A	S2 signal discriminator input pin 2. 3-state input
48	SC2	I	A	S-video signal input pin 2 (C)
49	VCC4	P	A	Video block supply pin 4
50	D1SW	I	D	D-terminal connecting discriminator input pin 1
51	DY1	I	A	Component video input pin 1 (Y)
52	D1L1	I	D	D-terminal signal discriminator input pin 1. 3-state input
53	DCb1	I	A	Component video input pin 1 (Cb)
54	D1L2	I	D	D-terminal signal discriminator input pin 2
55	DCr1	I	A	Component video input pin 1 (Cr)
56	GND6	GND	A	Analog ground pin 6
57	D1L3	I	D	D-terminal signal discriminator input pin 3. 3-state input
58	D2SW	I	D	D-terminal connecting discriminator input pin 2
59	DY2	I	A	Component video input pin 2 (Y)
60	DCb2	I	A	Component video input pin 2 (Cb)
61	DCr2	I	A	Component video input pin 2 (Cr)
62	GND7	GND	A	Analog ground pin 7
63	IREF	O	A	Internal reference current control pin. Connect a 39kΩ ±1% resistor between this pin and GND.
64	VREF2	O	A	Internal reference voltage pin 2 (video block)

*1. I: input, O: output, P: Power supply, GND: Ground
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O*1	Equivalent circuit
1	VREF1	O	
6 7 8 9 10 11 12 13 14 15	LV1 LV2 LV3 LV4 LV5 RV1 RV2 RV3 RV4 RV5	I	
18 20	ROUT LOUT	O	
21	ADS	I	

Number	Name	I/O*1	Equivalent circuit
23 24	SCL SDA	I I/O	
27 28 30	CrOUT CbOUT YOUT	O	
33 35 37 39 41 45 50 58	VC1 VC2 VC3 VC4 S-1 S-2 D1SW D2SW	I	
34 36 38 40 42 46 51 59	V1 V2 V3 V4 SY1 SY2 DY1 DY2	I	

Number	Name	I/O*1	Equivalent circuit
43 47 52 54 57	S2-1 S2-2 D1L1 D1L2 D1L3	I	
44 48 53 55 60 61	SC1 SC2 DCb1 DCr1 DCb2 DCr2	I	
63	IREF	O	
64	VREF2	O	

*1. I: input, O: output

Note. Resistance values in the equivalent circuits indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

GND1 = GND2 = GND3 = GND4 = GND5 = GND6 = GND7 = VSS = 0V,
VCC1 = VCC2 = VCC3 = VCC4 = VDD = V_{CC}, VCCA1 = VCCA2 = V_{CCA}, unless otherwise noted.

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC1, VCC2, VCC3, VCC4, VDD	–0.3 to 7.0	V
Supply voltage 2	V_{CCA}	VCCA1, VCCA2	–0.3 to 12.0	V
Input voltage 1	V_{IN1}	V1, V2, V3, V4, SY1, SC1, SY2, SC2, DY1, DCb1, DCr1, DY2, DCb2, DCr2, VC1, VC2, VC3, VC4, S-1, S2-1, S-2, S2-2, D1SW, D1L1, D1L2, D1L3, D2SW, ADS, SCL, SDA	GND – 0.3 to V_{CC} + 0.3	V
Input voltage 2	V_{IN2}	LV1, LV2, LV3, LV4, LV5, RV1, RV2, RV3, RV4, RV5	GND – 0.3 to V_{CCA} + 0.3	V
Storage temperature range	T_{STG}		–55 to +125	°C
Power dissipation	P_D	θ_{ja} *1= 117.9°C/W (Ta = 25°C)	0.42	W
Junction temperature	T_J		125	°C

*1. θ_{ja} is measured value in the mounting condition which NPC specified.

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC1, VCC2, VCC3, VCC4, VDD	4.75 to 5.25	V
Supply voltage 2	V_{CCA}	VCCA1, VCCA2	8.0 to 10.0	V
Operating ambient temperature	Ta	Wiring factor = 150%, wind velocity = 0m/s	–20 to 70	°C

Electrical Characteristics

DC Characteristics

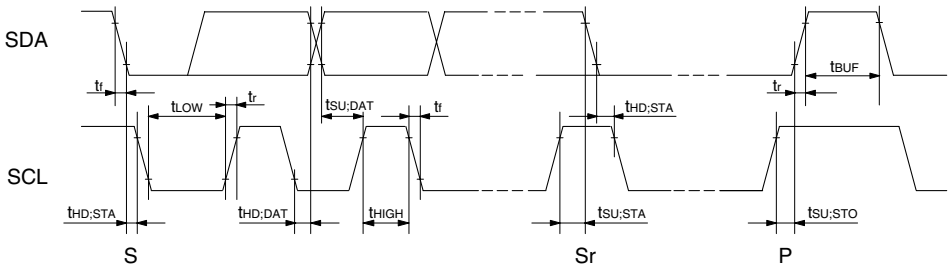
Ta = 25°C, R_{IREF} = 39kΩ, video block; V_{CC} = 5.0V, fin = 100kHz, V_{IN} = 1.0Vp-p, R_L = 300Ω, audio block; V_{CCA} = 9.0V, fin = 1kHz, V_{IN} = 1.0V_{RMS}, R_L = 600Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption 1	I_{CC1}	Filter = 00h, 01h, 02h, Video block (V_{CC}) V_{IN} = 0Vp-p	–	45	60	mA	I
Current consumption 2	I_{CC2}	Audio block (V_{CCA}) V_{IN} = 0V_{RMS}	–	5	8	mA	I
HIGH-level input voltage 1	V_{IH1}	ADS	0.8 V_{CC}	–	–	V	I
LOW-level Input voltage 1	V_{IL1}		–	–	0.2 V_{CC}	V	I
HIGH-level input voltage 2	V_{IH2}	SDA, SCL V_{CC} = 4.75V to 5.25V	1.89	–	–	V	I
LOW-level input voltage 2	V_{IL2}		–	–	1.08	V	I
Input hysteresis voltage	V_{HYS}		0.18	–	–	V	I
HIGH-level input voltage 3	V_{IH3}	S-1, S-2	3.2	–	–	V	I
LOW-level input voltage 3	V_{IL3}		–	–	1.8	V	I
HIGH-level input voltage 4	V_{IH4}	VC1, VC2, VC3, VC4	3.2	–	–	V	I
LOW-level Input voltage 4	V_{IL4}		–	–	1.8	V	I
HIGH-level input voltage 5	V_{IH5}	S2-1, S2-2	3.5	–	–	V	I
Middle-level input voltage 5	V_{IM5}		1.4	–	2.4	V	I
LOW-level Input voltage 5	V_{IL5}		–	–	0.8	V	I
HIGH-level input voltage 6	V_{IH6}	D1L1, D1L3	3.5	–	–	V	I
Middle-level input voltage 6	V_{IM6}		1.4	–	2.4	V	I
LOW-level Input voltage 6	V_{IL6}		–	–	0.8	V	I
HIGH-level input voltage 7	V_{IH7}	D1L2	3.5	–	–	V	I
LOW-level Input voltage 7	V_{IL7}		–	–	2.4	V	I
HIGH-level input voltage 8	V_{IH8}	D1SW, D2SW	3.2	–	–	V	I
LOW-level Input voltage 8	V_{IL8}		–	–	1.8	V	I
HIGH-level input leakage current	I_{LH}	SDA, SCL, V_{IN} = V_{CC}	–	–	± 1.0	µA	I
LOW-level input leakage current	I_{LL}	SDA, SCL, V_{IN} = 0V	–	–	± 1.0	µA	I
LOW-level output voltage 1	V_{OL1}	SDA = LOW, sink current = 3mA	0.0	–	0.4	V	I

I²C-BUS AC Characteristics

V_{CC} = 4.75 to 5.25V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL clock LOW-level pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL clock HIGH-level pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0	–	0.9	µs	II
SDA data hold time (output delay time)	$t_{HDO;DAT}$	SDA output hold delay time referred to V_{IH2} minimum level of SCL falling	0.3	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
Bus free time (between stop condition to start condition)	t_{BUF}		1.3	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II



Note. S, Sr: start condition, P: stop condition

Figure 1. I²C-BUS AC characteristics timing chart

Video Block Analog Input Characteristics

V_{CC} = 5.0V, Ta = 25°C, R_{IREF} = 39kΩ, fin = 100kHz, V_{IN} = 1.0Vp-p, R_L = 300Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage	V_{CLAMP}	V1, V2, V3, V4, SY1, SY2, DY1, DY2	–	1.8	–	V	I
Bias voltage	V_{BIAS}	SC1, SC2, DCb1, DCr1, DCb2, DCr2	–	2.3	–	V	I
Input resistance	R_{IBIAS}	SC1, SC2, DCb1, DCr1, DCb2, DCr2	–	80	–	kΩ	II
Input voltage	V_{AI}	THD < 1.0%	–	–	1.4	Vp-p	I

Video Block Analog Output Characteristics

V_{CC} = 5.0V, Ta = 25°C, R_{IREF} = 39kΩ, fin = 100kHz, V_{IN} = 1.0Vp-p, R_L = 300Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Output gain	A_V		5.5	6.0	6.5	dB	I
Channel to channel gain error	dA_V	Between any two channels	–	–	± 0.2	dB	I
Output voltage	V_{OUT}	THD < 1.0%	–	–	2.8	Vp-p	I
Channel to channel crosstalk	$XTLK_{CH}$	V_{IN} = 1.0Vp-p, fin = 1MHz, between any two channels	–	–72	–	dB	II
Input multiplexer crosstalk	$XTLK_{MUX}$	V_{IN} = 1.0Vp-p, fin = 1MHz, between each input system	–	–72	–	dB	II
Drive load resistance	R_L	YOUT, CbOUT, CrOUT	300	–	–	Ω	I
I^2C response time	t_{IIC}	Response time from the SCL rising in the ACK bit, when modifying setting using I^2C-BUS	–	–	1	µs	II

Filter Frequency Characteristics

V_{CC} = 5.0V, Ta = 25°C, R_{IREF} = 39kΩ, fin = 100kHz, V_{IN} = 1.0Vp-p, R_L = 300Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Passband attenuation (30MHz)	A_{PB30}	Filter = 02h, fin = 30MHz/100kHz, YOUT, CbOUT, CrOUT	–1.0	0	+1.0	dB	I
Passband attenuation (13.5MHz)	A_{PB13}	Filter = 01h, fin = 13.5MHz/100kHz, YOUT, CbOUT, CrOUT	–1.0	0	+1.0	dB	I
Passband attenuation (6.75MHz)	A_{PB7}	Filter = 00h, fin = 6.75MHz/100kHz, YOUT, CbOUT, CrOUT	–1.0	0	+1.0	dB	I
Stopband attenuation (30MHz)	A_{SB30}	Filter = 02h, fin = 120MHz/100kHz, YOUT, CbOUT, CrOUT	–	–20	–	dB	II
Stopband attenuation (13.5MHz)	A_{SB13}	Filter = 01h, fin = 54MHz/100kHz, YOUT, CbOUT, CrOUT	–	–20	–	dB	II
Stopband attenuation (6.75MHz)	A_{SB7}	Filter = 00h, fin = 27MHz/100kHz, YOUT, CbOUT, CrOUT	–	–20	–10	dB	I
Filter bypass mode bandwidth	f_{BP}	Filter = 03h, V_{IN} = 0.7Vp-p, at –1dB falling from the gain of fin = 100kHz, YOUT, CbOUT, CrOUT	74.25	80	–	MHz	II

Audio Block Analog Characteristics

V_{CC} = 5.0V, V_{CCA} = 9.0V, Ta = 25°C, R_{IREF} = 39kΩ, fin = 1kHz, V_{IN} = 1.0V_{RMS}, R_L = 600Ω, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Input voltage	V_{AI}	THD < 1.0%	–	–	2.1	V_{RMS}	I
Output gain	A_V		–0.5	0.0	0.5	dB	I
Output voltage	V_{OUT}	THD < 1.0%	–	2.1	–	V_{RMS}	I
Channel to channel gain error	dA_V	Between any two channels	–	–	± 0.2	dB	I
Channel to channel crosstalk	$XTLK_{CH}$	V_{IN} = 1.0V_{RMS}, fin = 1kHz, between any two channels	–	–90	–	dB	II
Input multiplexer crosstalk	$XTLK_{MUX}$	V_{IN} = 1.0V_{RMS}, fin = 1kHz, between each input system	–	–90	–	dB	II
S/N	S/N	V_{IN} = 1.0V_{RMS}, fin = 1kHz	–	100	–	dB	II
Passband	F_{BW}	V_{IN} = 1.0V_{RMS}, gain = –3dB	25	–	–	kHz	I
Total harmonic distortion	THD + N	V_{IN} = 1.0V_{RMS}, fin = 1kHz	–	0.005	0.01	%	I

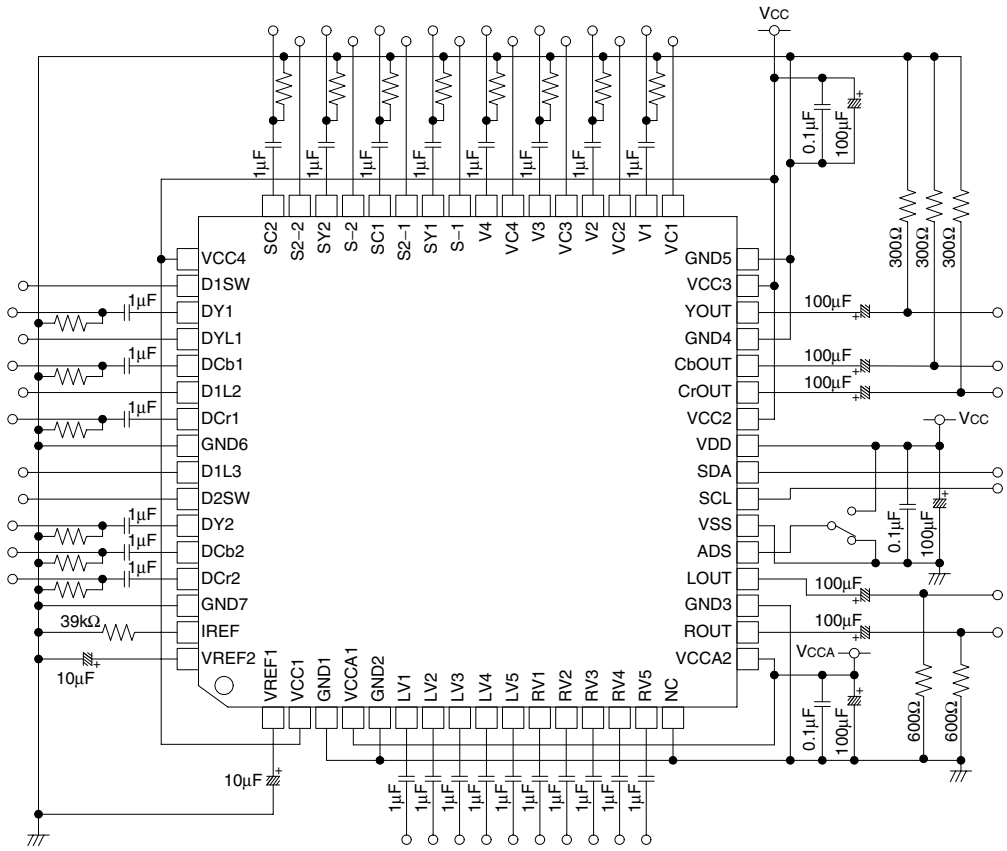
Test Level

The definition of “Test Level” shown in the electric characteristic table is as follows.

I : 100% of products tested at Ta = + 25°C.

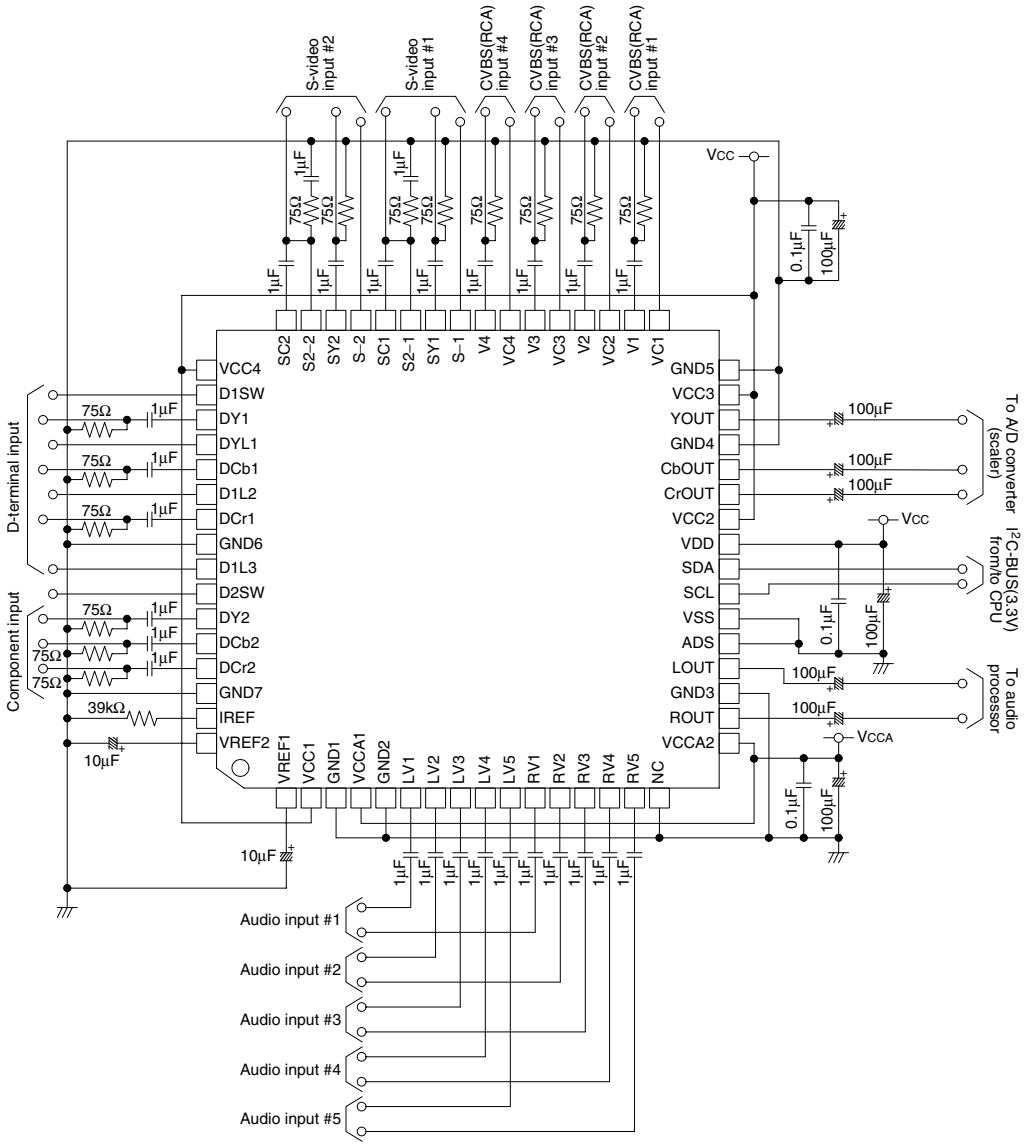
II : Guaranteed as result of design and characteristics evaluation.

Measurement Circuit



Note. This figure is a circuit only for the evaluation board of an electric characteristics. (It is not a recommended application circuit.)

TYPICAL APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

I²C-BUS Control

The SM5351AF1 uses the I²C-BUS interface to control the following functions:

1) Input switch select
2) Output mute settings

In addition, the interface is used to read the following status parameters:

3) Cable connecting status of each connector
4) S2 signal and D-terminal signals discriminate result

The transfer speed is compatible with fast mode (400kbit/s). The SM5351AF1 corresponds to the I²C-BUS of 2.7V to 3.6V supply voltage. (It is independent on voltage of VDD pin.)

Basic Cycle

The write sequence is: SM5351AF1 slave address → specific control register sub-address → write data. Data can be written to the SM5351AF1 in successive bytes, as the sub-address for the register is incremented automatically after each byte. However, if the sub-address exceeds the address of the last register (02h), data write operation to the SM5351AF1 register stops and the acknowledge signal is not returned.

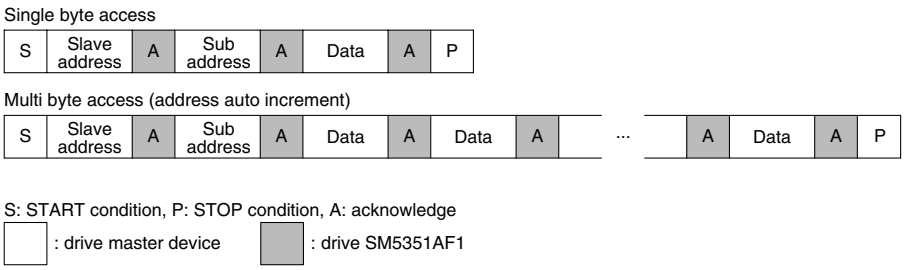


Figure 2. Write sequence

The read sequence is: SM5351AF1 slave address → sub-address 0 status register value → sub-address 1 status register value → sub-address 2 status register value. In status register read-out, the data of all 3 bytes should be red out. A specific status register sub-address cannot be assigned for a read operation.

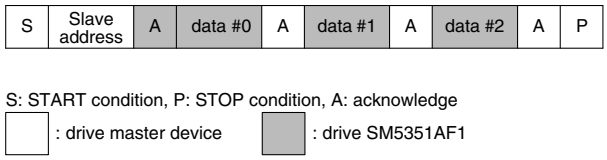


Figure 3. Read sequence

Slave Address, Sub-address

The 7-bit slave address is selected using the ADS pin. When ADS = “L” the address is 48h (1001000b), and when ADS = “H” the address is 49h (1001001b). A maximum of two SM5351AF1 devices can be connected to one I^2C-BUS simultaneously, and controlled independently by setting the slave address of each using the ADS pin. In order to writing register, continuing in slave address, transmit the sub-address of the control register. (When reading the status register, it is unnecessary to write sub-address.)

SLAVE ADDRESS for Status Register Read (1st byte)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SLAVE ADDRESS							R/W		
Value	1	0	0	1	0	0	0	1	91h	Indicate to read when device's slave address is 48h (ADS = "L")
	1	0	0	1	0	0	1	1	93h	Indicate to read when device's slave address is 49h (ADS = "H")

SLAVE ADDRESS for Control Register Write (1st byte)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SLAVE ADDRESS							R/W		
Value	1	0	0	1	0	0	0	0	90h	Indicate to write when device's slave address is 48h (ADS = "L")
	1	0	0	1	0	0	1	0	92h	Indicate to write when device's slave address is 49h (ADS = "H")

SUB ADDRESS for Control Register Write (2nd byte)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SUB ADDRESS							R/W		
Value	0	0	0	0	0	0	0	0	00h	Indicate to write control register 00h
	0	0	0	0	0	0	0	1	01h	Indicate to write control register 01h
	0	0	0	0	0	0	1	0	02h	Indicate to write control register 02h

Control Register

The SM5351AF1 has a 3-byte control register.

sub addr.	Register assign								default	Description
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	
00h	0	0	0	0	VIDEO				00h	YOUT, CbOUT, CrOUT video output and standby select
01h	0	0	0	0	AUDIO				00h	LOUT, ROUT audio output and standby select
02h	0	0	0	0	0	0	Filter		00h	YOUT, CbOUT, CrOUT video output filter select

The function of each byte in the control register is described in the following tables.

Register name: VIDEO
Sub-address: 00h, bit3 to bit0

Control Register sub addr. 00h					OUTPUT			Description
bit3	bit2	bit1	bit0	(Hex)	YOUT	CbOUT	CrOUT	
0	0	0	0	0h	mute	mute	mute	mute (default)
0	0	0	1	1h	V1	mute	mute	V1 input select
0	0	1	0	2h	V2	mute	mute	V2 input select
0	0	1	1	3h	V3	mute	mute	V3 input select
0	1	0	0	4h	V4	mute	mute	V4 input select
1	0	0	0	8h	SY1	SC1	mute	S-video 1 (SY1, SC1) input select
1	0	0	1	9h	SY2	SC2	mute	S-video 2 (SY2, SC2) input select
1	1	0	0	Ch	DY1	DCb1	DCr1	D-terminal 1 (DY1, DCb1, DCr1) input select
1	1	0	1	Dh	DY2	DCb2	DCr2	D-terminal 2 (DY2, DCb2, DCr2) input select

Select video signal source for output (YOUT, CbOUT, CrOUT).

Register name: AUDIO
Sub-address: 01h, bit3 to bit0

Control Register sub addr. 01h					OUTPUT		Description
bit3	bit2	bit1	bit0	(Hex)	LOUT	ROUT	
0	0	0	0	0h	mute	mute	mute (default)
0	0	0	1	1h	LV1	RV1	LV1, RV1 input select
0	0	1	0	2h	LV2	RV2	LV2, RV2 input select
0	0	1	1	3h	LV3	RV3	LV3, RV3 input select
0	1	0	0	4h	LV4	RV4	LV4, RV4 input select
0	1	0	1	5h	LV5	RV5	LV5, RV5 input select

Select audio signal source for output.

Register name: Filter
Sub-address: 02h, bit1 to bit0

Control Register sub addr. 02h			Filter			Description
bit1	bit0	(Hex)	YOUT	CbOUT	CrOUT	
0	0	0h	6.75MHz	6.75MHz	6.75MHz	Passband: 6.75MHz
0	1	1h	13.5MHz	13.5MHz	13.5MHz	Passband: 13.5MHz
1	0	2h	30MHz	30MHz	30MHz	Passband: 30MHz
1	1	3h	Bypass	Bypass	Bypass	Filter bypass

Sets the cutoff frequency of lowpass filter for video output (YOUT, CbOUT, CrOUT).

Status Register

SM5351AF1 has a 3-byte status register.

sub addr.	Register assign								Description
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
00h	VC1	VC2	VC3	VC4	S-1	S-2	D1SW	D2SW	Connections condition
01h	S2-1		D1L1		D1L2		D1L3		S2-1 or D1 discriminate result
02h	S2-2		0	0	0	0	0	0	S2-2 discriminate result

The function of each byte in the status register is described in the following tables.

Register name: VC1, VC2, VC3, VC4
Sub-address: 00h, bit7 to bit4

Status Register sub addr. 00h	INPUT pin DC level	Description
bit7	VC1	
0	> 3.2V	RCA connector of V1 is disconnected.
1	< 1.8V	RCA connector of V1 is connected.

Status Register sub addr. 00h	INPUT pin DC level	Description
bit6	VC2	
0	> 3.2V	RCA connector of V2 is disconnected.
1	< 1.8V	RCA connector of V2 is connected.

Status Register sub addr. 00h	INPUT pin DC level	Description
bit5	VC3	
0	> 3.2V	RCA connector of V3 is disconnected.
1	< 1.8V	RCA connector of V3 is connected.

Status Register sub addr. 00h	INPUT pin DC level	Description
bit4	VC4	
0	> 3.2V	RCA connector of V4 is disconnected.
1	< 1.8V	RCA connector of V4 is connected.

Returns the connections condition of CVBS input RCA connector.
(It discriminates DC voltage of VC1, VC2, VC3 or VC4 pin. These pins are pulled-up in IC internally.)

Register name: S-1, S-2
Sub-address: 00h, bit3 to bit2

Status Register sub addr. 00h	INPUT pin DC level	Description
bit3	S-1	
0	> 3.2V	Connector of S-video terminal 1 is disconnected.
1	< 1.8V	Connector of S-video terminal 1 is connected.

Status Register sub addr. 00h	INPUT pin DC level	Description
bit2	S-2	
0	> 3.2V	Connector of S-video terminal 2 is disconnected.
1	< 1.8V	Connector of S-video terminal 2 is connected.

Returns the connections condition of S-video terminal connectors.
(It discriminates DC voltage of S-1 or S-2 pin. These pins are pulled-up in IC internally.)

Register name: D1SW, D2SW
Sub-address: 00h, bit1 to bit0

Status Register sub addr. 00h	INPUT pin DC level	Description
bit1	D1SW	
0	> 3.2V	Connector of D-terminal 1 is disconnected.
1	< 1.8V	Connector of D-terminal 1 is connected.

Status Register sub addr. 00h	INPUT pin DC level	Description
bit0	D2SW	
0	> 3.2V	Connector of D-terminal 2 is disconnected.
1	< 1.8V	Connector of D-terminal 2 is connected.

Returns the connections condition of D-terminal connectors.
(It discriminates DC voltage of D1SW or D2SW pin. These pins are pulled-up in IC internally.)

Register name: S2-1, S2-2
Sub-address: 01h to 02h, bit7 to bit6

Status Register sub addr. 01h		INPUT pin DC level		Description
bit7	bit6	S2-1	S-1	
0	0	< 0.8V	< 1.8V	Video signal of S-video terminal 1 is '4:3'.
0	1	> 1.4V and < 2.4V	< 1.8V	Video signal of S-video terminal 1 is '4:3 letter box'.
1	0	> 3.5V	< 1.8V	Video signal of S-video terminal 1 is '16:9 squeeze'.
1	1	(don't care)	> 3.2V	Connector of S-video terminal 1 is disconnected.

Status Register sub addr. 02h		INPUT pin DC level		Description
bit7	bit6	S2-2	S-2	
0	0	< 0.8V	< 1.8V	Video signal of S-video terminal 2 is '4:3'.
0	1	> 1.4V and < 2.4V	< 1.8V	Video signal of S-video terminal 2 is '4:3 letter box'.
1	0	> 3.5V	< 1.8V	Video signal of S-video terminal 2 is '16:9 squeeze'.
1	1	(don't care)	> 3.2V	Connector of S-video terminal 2 is disconnected.

Returns the discriminated result of S2 signals.
(It discriminates DC voltage of S2-1 or S2-2 pin. These pins are pulled-down in IC internally.)

Register name: D1L1, D1L2, D1L3
Sub-address: 01h, bit5 to bit0

Status Register sub addr. 01h		INPUT pin DC level	Description
bit5	bit4	D1L1	
0	0	< 0.8V	Video signal of D-terminal 1 is '480 line'.
0	1	> 1.4V and < 2.4V	Video signal of D-terminal 1 is '720 line'.
1	0	> 3.5V	Video signal of D-terminal 1 is '1080 line'.
1	1	–	(undefined)

Status Register sub addr. 01h		INPUT pin DC level	Description
bit3	bit2	D1L2	
0	0	< 2.4V	Video signal of D-terminal 1 is '60i'.
1	0	> 3.5V	Video signal of D-terminal 1 is '60p'.

Status Register sub addr. 01h		INPUT pin DC level	Description
bit1	bit0	D1L3	
0	0	< 0.8V	Video signal of D-terminal 1 is '4:3'.
0	1	> 1.4V and < 2.4V	Video signal of D-terminal 1 is '4:3 letter box'.
1	0	> 3.5V	Video signal of D-terminal 1 is '16:9 squeeze'.
1	1	–	(undefined)

Returns the discriminated result of D-terminal signals.
(It discriminates DC voltage of D1L1, D1L2 or D1L3 pin. These pins are pulled-down in IC internally.)

Caution of Register Setting

The control register should be writing the value as defined in this specification. If undefined value is written, SM5351AF1 might operate abnormally.

Power Supply Pin

To using the function of audio block, input V_{CC} = 4.75V to 5.25V to the VCC1, VCC2, VCC3, VCC4 and VDD pins, and input V_{CCA} = 8V to 10V, to the VCCA1 and VCCA2 pins. To using only the function of video block, input V_{CC} = 4.75V to 5.25V to the VCC1, VCC2, VCC3, VCC4 and VDD pins. It is not necessary to input V_{CCA} power supply. There is no relationship in the order of the startup or fall of V_{CC} power supply and V_{CCA} power supply. I^2C-BUS interface (SDA and SCL pin) and control logic circuit uses V_{CC} power supply (VDD pin). The SM5351AF1 corresponds to the I^2C-BUS of 2.7V to 3.6V, but VDD pin should be set the same as V_{CC} power supply (4.75V to 5.25V). When V_{CC} power supply rises, control register is reset to initial value.

IREF Pin

It should be connected a 3.9kΩ ± 1% resistor between IREF pin and GND, because it control internal reference current. The current flows into the IREF pin in normal operating mode and during output muting.

VREF Pins

The VREF1 and VREF2 pins are the internal reference voltage output. To ensure IC operating stability, it is recommended that capacitors connects between VREF1 and GND, and connects between VREF2 and GND. The recommended value is 10µF of each. The voltages on VREF1 and VREF2 are output in normal operating mode and during output muting.

TYPICAL PERFORMANCE

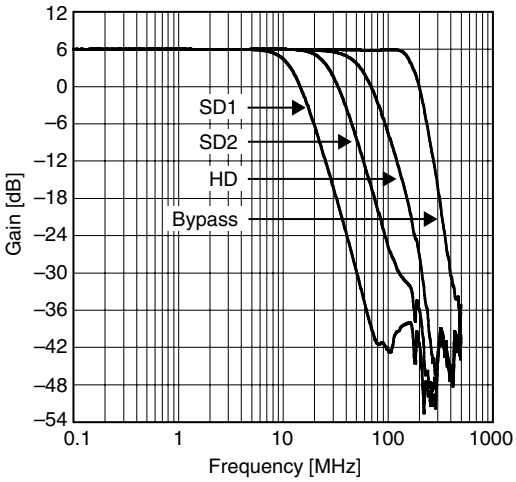


Figure 4. Video block: gain vs. frequency

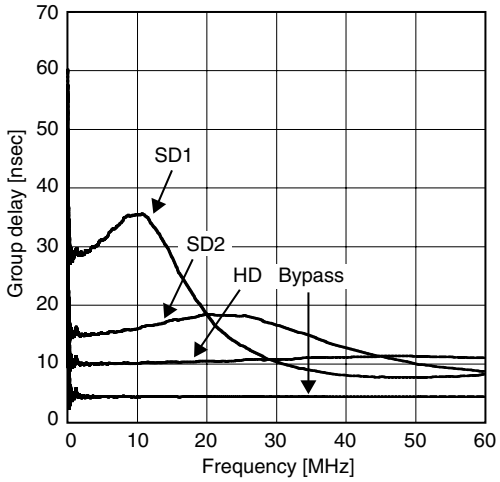


Figure 5. Video block: group delay vs. frequency

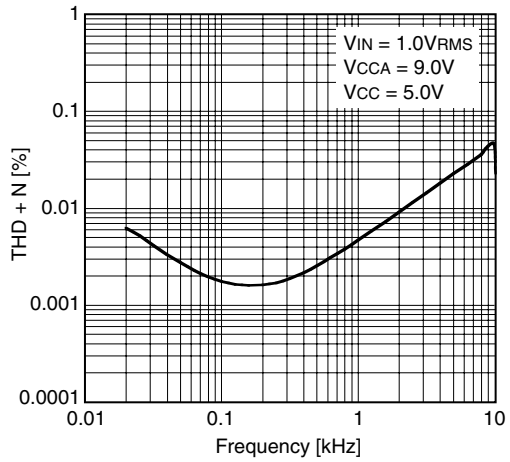


Figure 6. Audio block: THD + N vs. frequency

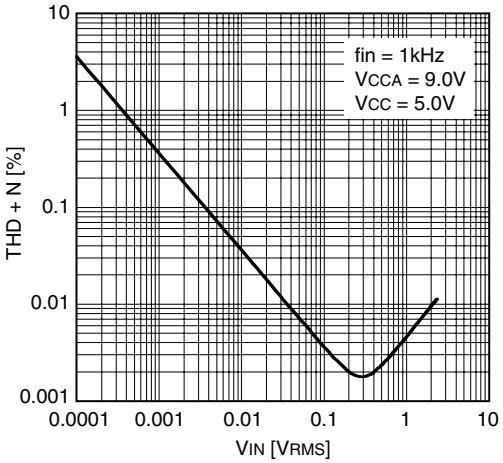


Figure 7. Audio block: THD + N vs. V_{IN}

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