International
IOR Rectifier

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# IR1155S

## PROGRAMMABLE FREQUENCY, ONE CYCLE CONTROL PFC IC

### Features

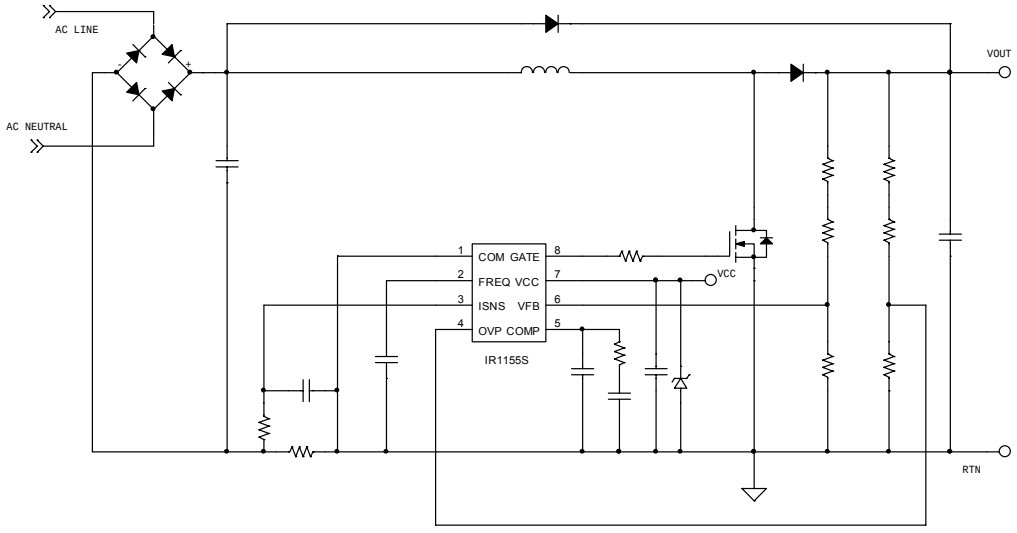
- PFC IC with IR proprietary “One Cycle Control”
- Continuous conduction mode boost type PFC
- Programmable switching frequency (48k-200kHz)
- Average current mode control
- Output overvoltage protection
- Open loop protection
- Cycle by cycle peak current limit
- VCC under voltage lockout
- Programmable soft start
- Micropower startup
- User initiated micropower “Sleep Mode”
- OVP/EN pin internal filtering for higher noise immunity
- 1.5A peak gate drive
- Latch immunity and ESD protection

### Description

The µPFC IR1155 power factor correction IC, based on IR proprietary "One Cycle Control" (OCC) technique, provides for high PF, low THD and excellent DC Bus regulation while enabling drastic reduction in component count, PCB area and design time as compared to traditional solutions. The IC is designed to operate in continuous conduction mode Boost PFC converters with average current mode control over 85-264VAC input line voltage range. Switching frequency can be programmed to anywhere between 48kHz to 200kHz based on the specific application requirement. In addition, IR1155 offers several advanced system-enabling and protective features such as dedicated pin for over voltage protection, cycle by cycle peak current limitation, open loop protection, $V_{CC}$ UVLO, soft-start and micropower startup/sleep-mode with IC current consumption less than 200µA. The sleep mode, invoked by pulling the OVP/EN pin low, enables compliance with standby power requirements mandated by regulations such as Energy Star, Green Power, Blue Angel etc.

### Package


### IR1155 Application Diagram



**Qualification Information**

| | | |
|---|---|---|
| Qualification Level | | Industrial<br>Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |
| Moisture Sensitivity Level | | MSL2 260°C<br>(per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class A<br>(per JEDEC standard JESD22-A115) |
| | Human Body Model | Class 1B (passes 500V)<br>(per EIA/JEDEC standard EIA/JESD22-A114) |
| IC Latch-Up Test | | Class I, Level A<br>(per JESD78) |
| RoHS Compliant | | Yes |

**Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Units | Remarks |
|---|---|---|---|---|---|
| VCC Voltage | $V_{CC}$ | -0.3 | 20 | V | |
| FREQ Voltage | $V_{FREQ}$ | -0.3 | 6.5 | V | |
| ISNS Voltage | $V_{ISNS}$ | -10 | 0.3 | V | |
| VFB, OVP Voltage | $V_{FB}$, $V_{OVP}$ | -0.3 | 6.5 | V | |
| COMP Voltage | $V_{COMP}$ | -0.3 | 6.5 | V | |
| GATE Voltage | $V_{GATE}$ | -0.3 | 18 | V | |
| ISNS Current | $I_{ISNS}$ | -2 | 2 | mA | |
| Junction Temperature | $T_J$ | -40 | 150 | °C | |
| Storage Temperature | $T_S$ | -55 | 150 | °C | |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | 128 | °C/W | |
| Package Power Dissipation | $P_D$ | | 976 | mW | $T_{AMB}$ = 25°C |

**Recommended Operating Conditions**

Recommended operating conditions for reliable operation with margin

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 12 | | 19 | V | |
| Junction Temperature | $T_J$ | -25 | | 125 | °C | |
| Switching Frequency | $F_{SW}$ | 48 | | 200 | kHz | |

## Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range $T_J$ from –25 °C to 125°C. Typical values represent the median values, which are related to 25°C. **If not otherwise stated, a supply voltage of $V_{CC}$ =15V is assumed for test condition**.

### Supply Section

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| VCC Turn On Threshold | $V_{CC\ ON}$ | 10.65 | 11.3 | 11.95 | V | |
| VCC Turn Off Threshold (Under Voltage Lock Out) | $V_{CC\ UVLO}$ | 9.2 | 9.8 | 10.4 | V | |
| VCC Turn On/Off Hysteresis | $V_{CC\ HYST}$ | | 1.5 | | V | |
| Operating Current | $I_{CC}$ | | 10 | 13 | mA | $C_{load}$=1nF, $F_{SW}$=181kHz |
| | | | 6 | 8 | mA | **Standby Mode** (Inactive Gate, Inactive Internal Oscillator) $V_{FB}<V_{OLP}$ See State Transition Diagram |
| Startup Current | $I_{CCSTART}$ | | | 175 | uA | $V_{CC}=V_{CC\ ON}$ - 0.1V |
| Sleep Current | $I_{SLEEP}$ | | 125 | 200 | uA | **Sleep Mode** (Inactive Gate, Inactive Oscillator) - $V_{OVP}<V_{SLEEP,OFF}$ See State Transition Diagram |
| Sleep Mode Threshold (Enable) | $V_{SLEEP,ON}$ | 0.80 | 0.90 | 1.00 | V | IC Enable threshold, Bias on OVP pin |
| Sleep Mode Threshold (Disable) | $V_{SLEEP,OFF}$ | 0.53 | 0.60 | 0.67 | V | IC Disable threshold, Bias on OVP pin |

**Oscillator Section**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Switching Frequency | $F_{SW}$ | 48 | | 200 | kHz | 200khz:C=430pF approx.<br>48kHz: C=2nF approx. |
| Oscillator Charge Current | $I_{OSC(CHG)}$ | | 200 | | µA | |
| Oscillator Discharge Current | $I_{OSC(DCHG)}$ | | 6.6 | | mA | |
| Oscillator Peak | $V_{OSC\ PK}$ | | 4 | | V | |
| Oscillator Valley | $V_{OSC\ VAL}$ | | 2 | | V | |
| Initial Accuracy | $F_{SW\ ACC}$ | | | 5 | % | C=2nF, $T_A$ = 25°C |
| | | | | 8 | % | C=500pF, $T_A$ = 25°C |
| Voltage Stability | $V_{STAB}$ | | 0.2 | 1 | % | 14V < $V_{CC}$ < 19V |
| Temperature Stability | $T_{STAB}$ | | 2 | | % | -25°C ≤ $T_J$ ≤ 125°C |
| Total Variation | $F_{VT}$ | | 10 | | % | Line & Temperature |
| Maximum Duty Cycle | $D_{MAX}$ | 94 | | 99 | % | |
| Minimum Duty Cycle | $D_{MIN}$ | | | 0 | % | Pulse Skipping |

**Protection Section**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Open Loop Protection (OLP) $V_{FB}$ Threshold | $V_{OLP}$ | 17 | 19 | 21 | % $V_{REF}$ | Bias on VFB pin |
| Output Over Voltage Protection (OVP) | $V_{OVP}$ | 104.5 | 106.5 | 108.5 | % $V_{REF}$ | Bias on OVP/EN pin |
| Output Over Voltage Protection (OVP) Reset | $V_{OVP(RST)}$ | 100.2 | 102.2 | 104.2 | % $V_{REF}$ | Bias on OVP/EN pin |
| Peak Current Limit Protection (IPK LMT) $I_{SNS}$ Voltage Threshold | $V_{ISNS}$ | -0.85 | -0.77 | -0.69 | V | Bias on ISNS pin |
| OVP Input Bias Current | $I_{OVP(Bias)}$ | | | -0.2 | µA | |

### Internal Voltage Reference Section

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Reference Voltage | $V_{REF}$ | 4.9 | 5 | 5.1 | V | $T_A$ = 25°C |
| Line Regulation | $R_{REG}$ | | 10 | 20 | mV | 14 V < $V_{CC}$ < 19V |
| Temp Stability | $T_{STAB}$ | | 0.4 | | % | -25°C ≤ $T_{AMB}$ ≤ 125°C |
| Total Variation | $\Delta V_{TOT}$ | 4.85 | | 5.1 | V | Line & Temperature |

### Voltage Error Amplifier Section

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Transconductance | $g_m$ | 35 | 50 | 65 | µS | |
| Source Current | $I_{OVEA(SRC)}$ | 30 | 44 | 58 | µA | $T_{AMB}$ = 25°C |
| | | 20 | 44 | 90 | | -25°C ≤$T_{AMB}$≤ 125°C |
| Sink Current | $I_{OVEA(SNK)}$ | -57 | -43 | -30 | µA | $T_{AMB}$ = 25°C |
| | | -90 | -43 | -20 | | -25°C ≤$T_{AMB}$≤ 125°C |
| Soft Start Delay Time | $t_{SS}$ | | 35 | | msec | $R_{GAIN}$ = 1kΩ, $C_{ZERO}$ = 0.33uF, $C_{POLE}$ = 0.01uF |
| $V_{COMP}$ Voltage (Fault) | $V_{COMP\ FLT}$ | | 1 | 1.4 | V | @ 100µA steady state current |
| Effective $V_{COMP}$ Voltage | $V_{COMP\ EFF}$ | 4.6 | 4.9 | 5.2 | V | |
| VFB Input Bias Current | $I_{IB(Bias)}$ | | | -0.2 | µA | $V_{FB}$=4.9V |
| Output Low Voltage | $V_{OL}$ | | | 0.25 | V | |
| Output High Voltage | $V_{OH}$ | 5 | | 5.4 | V | |
| $V_{COMP}$ Start Voltage | $V_{COMP\ START}$ | 240 | 340 | 460 | mV | |

**Current Amplifier Section**

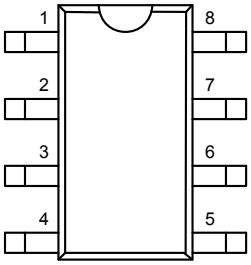
| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| DC Gain | $g_{DC}$ | | 3.1 | | V/V | |
| Corner Frequency | $f_C$ | | 5 | | kHz | - Average current mode, Note 1 |
| Input Offset Voltage | $V_{IO}$ | | 4 | 16 | mV | Note 1 |
| $I_{SNS}$ Bias Current | $I_{ISNS(Bias)}$ | -57 | | -13 | µA | |
| Blanking Time | $T_{BLANK}$ | 220 | 370 | 520 | ns | |

**Gate Driver Section**

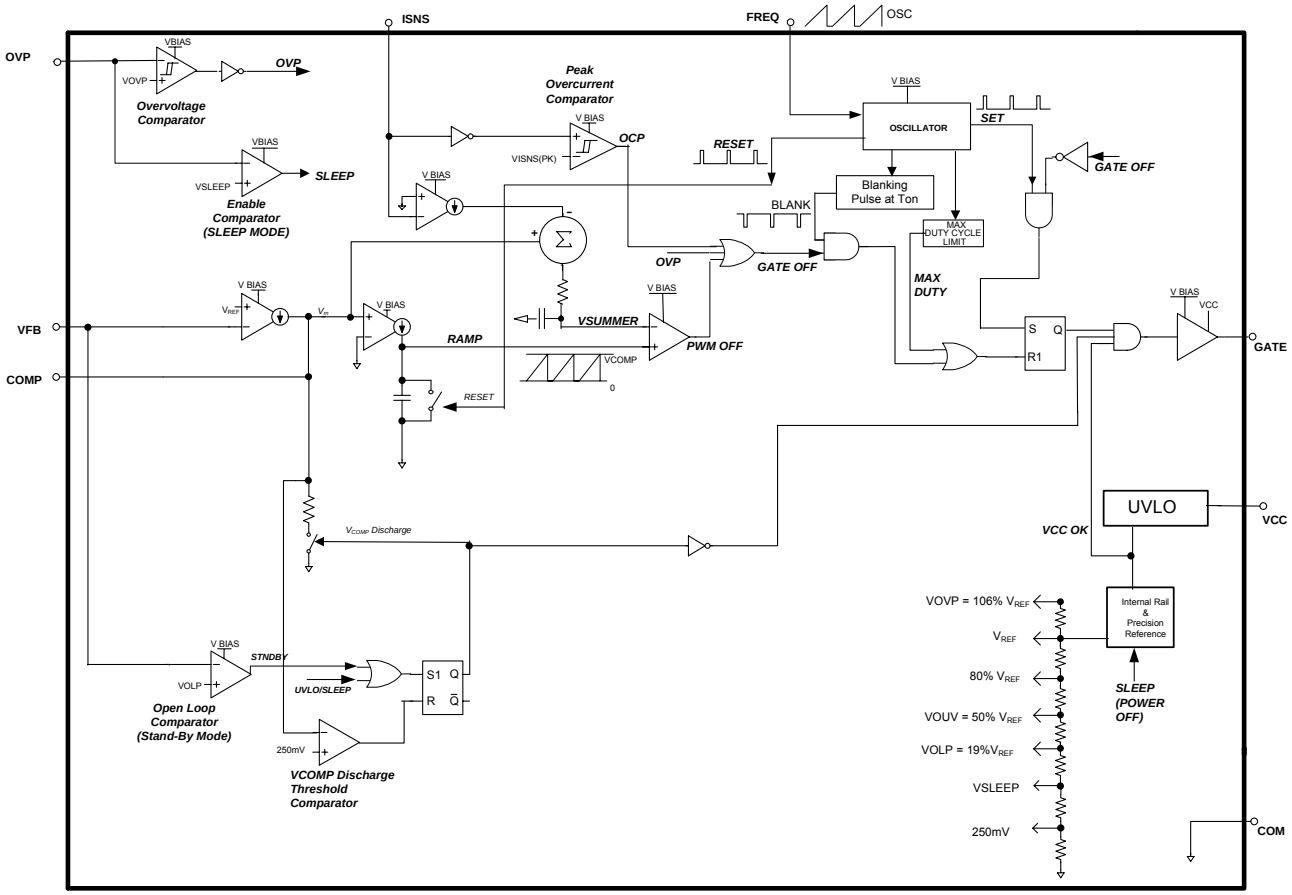
| Parameter | Symbol | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| Gate Low Voltage | $V_{GLO}$ | | | 0.8 | V | $I_{GATE}$=200mA |
| Gate High Voltage | $V_{GTH}$ | 12 | 13 | 14 | V | Internal Gate clamp |
| | | 10 | | | V | $V_{CC}$ = 11.5V |
| Rise Time | $t_r$ | | 20 | | ns | $C_{LOAD}$ = 1nF |
| Fall Time | $t_f$ | | 20 | | ns | $C_{LOAD}$ = 1nF |
| Output Peak Current | $I_{OPK}$ | 1.5 | | | A | $C_{LOAD}$ = 10nF, Note 1 |
| Gate Voltage @ Fault | $V_{G\ fault}$ | | | 0.08 | V | $I_{GATE}$ = 20mA |

**Note 1** – Guaranteed by design, but Not tested in production

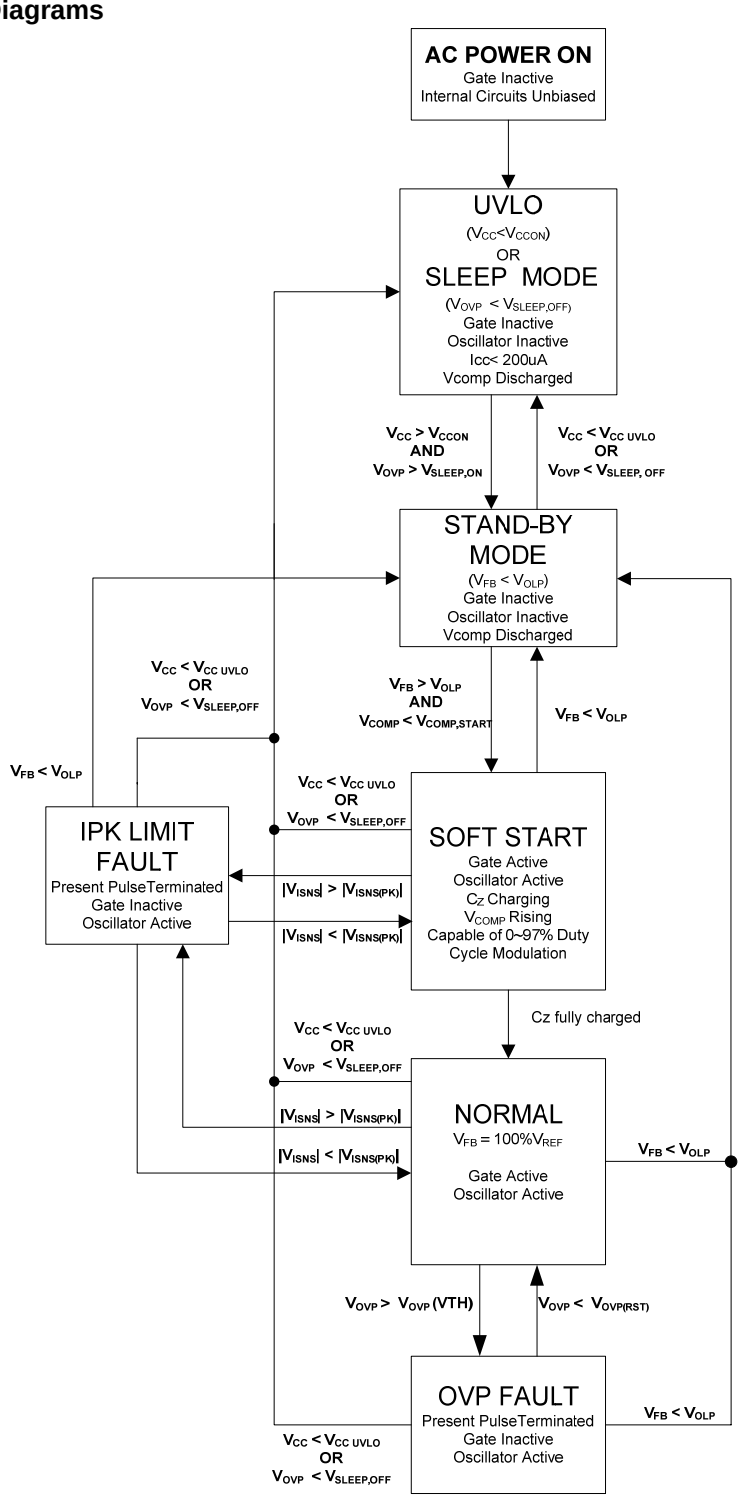
### Lead Assignments & Definitions

| Lead Assignment | Pin# | Symbol | Description |
|---|---|---|---|
|  | 1 | COM | Ground |
| | 2 | FREQ | Frequency Set |
| | 3 | ISNS | Current Sense |
| | 4 | OVP | Output Over Voltage Detect / Enable |
| | 5 | COMP | Voltage Loop Compensation |
| | 6 | VFB | Output Voltage Sense |
| | 7 | VCC | IC Supply Voltage |
| | 8 | GATE | Gate Drive Output |

## Block Diagram

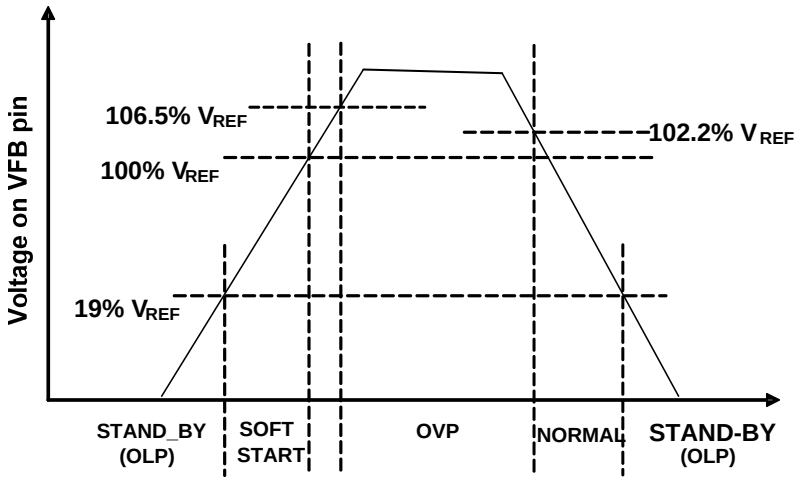


**State & Transition Diagrams**

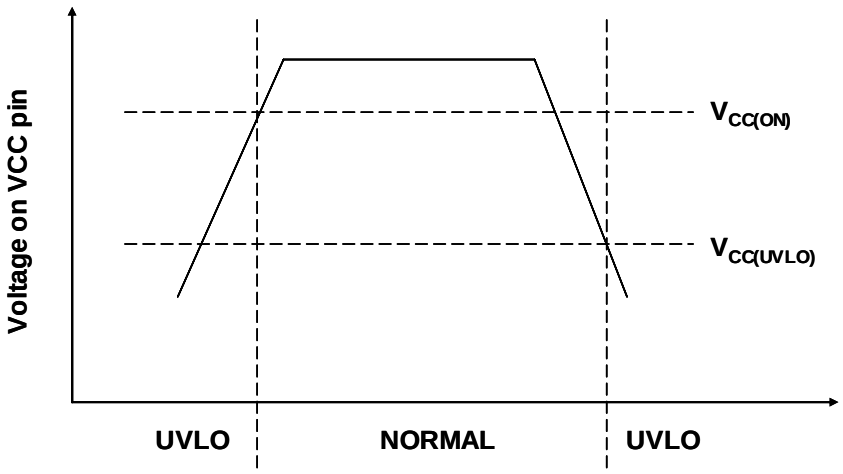



**Note:** Soft-Start & Normal modes are essentially the same (differentiation above is for purpose of clarity only)

**Timing Diagrams**




**Output Protection**




**VCC Undervoltage Lockout**

## IR1155 General Description

The µPFC IR1155 IC is intended for power factor correction in continuous conduction mode Boost PFC converters operating at fixed switching frequency with average current mode control. The switching frequency is programmable any where from 48kHz to 200khz. The IC operates according to IR's proprietary "One Cycle Control" (OCC) PFC algorithm, which is based on the re-settable integrator principle. When operating a AC-DC Boost converter, power factor correction can be achieved using this algorithm without AC input line sensing.

## Theory of Operation

The OCC algorithm works using two loops - a slow outer voltage loop and a fast inner current loop. The outer voltage loop monitors the VFB pin to maintain regulation of boost converter output voltage and generates a constant error signal. The inner current loop exploits the embedded input voltage information in the boost converter duty cycle to generate a current reference for power factor correction. The combination of the two control elements forces the amplitude and shape of the input current to be proportional to and in phase with the input voltage while maintaining output voltage regulation. This is true so long as operation in continuous conduction mode is maintained. Average current mode operation is envisaged by filtering the switching frequency ripple from the current sense signal in the current loop using an on-chip filter.

The IC determines the boost converter instantaneous duty cycle using the voltage feedback loop error signal $V_m$ and the current sense signal $V_{ISNS}$, which is the voltage at the current sense pin of the IC. The PWM ramp is generated using a resettable integrator that tracks $V_m$ every switching cycle. The current sense signal is amplified by the current amplifier averaged to remove the ripple component and fed into the summing node where it is subtracted from the voltage error signal, $V_m$. The resulting voltage ($V_m$ - $g_{DC}.V_{ISNS}$) is compared with the PWM ramp signal by the PWM comparator to determine the gate drive duty cycle. The instantaneous duty cycle is mathematically given by:

$D = (V_m - g_{DC}.V_{ISNS}) / V_m$

A more detailed description of IR1155 theory of operation is available in Application Note.

## Feature set

The IR1155 offers a host of advanced features and system protections functions, which makes it the most feature-intensive IC in PFC market in a compact 8-pin package.

*User-Programmable Switching Frequency*

IR1155 IC operates under fixed switching frequency. The switching frequency is user-programmed by inserting a capacitor between FREQ & COM pins. A pair of current sources inside the IC source/sink current in/out of the capacitor alternately thus generating a constant-slope saw-tooth ramp signal between a pre-determined peak & valley voltage pair (typically between 2V to 4V). This saw-tooth signal is the oscillator signal of the IC. The frequency of operation of the IC can be programmed anywhere between 48kHz and 200kHz by suitably sizing the capacitor. The oscillator signal is a key control signal and is used by the resettable integrator block of the IC to generate the internal PWM ramp every switching cycle.

*IC Supply Circuit & Low start-up current*

The IR1155 UVLO circuit maintains the IC in UVLO mode during start-up if VCC pin voltage is less than the VCC turn-on threshold, $V_{CC,ON}$ and current consumption is less than $I_{CC,START}$. Should VCC pin voltage should drop below UVLO threshold $V_{CC,\ UVLO}$ anytime after start-up, the IC is pushed back into UVLO mode (VCOMP pin is discharged) and VCC pin has to exceed $V_{CC,ON}$ again to re-start operation. It is noted that there is no internal clamping of the VCC pin.

*User initiated Micropower Sleep mode*

The IC can be actively pushed into a micropower sleep mode where current consumption is less than $I_{CC,SLEEP}$ by pulling OVP/EN pin below the Sleep threshold, $V_{SLEEP(OFF)}$, even while VCC is above $V_{CC,ON}$. This allows the user to disable PFC during application stand-by situations in order to meet regulations (Blue Angel, Green Power etc). When OVP/EN pin is pulled low, the VCOMP pin of the IC is actively discharged as the IC is relegated to the Sleep mode. This enables the IC to go through soft-start when the IC is re-enabled. Since $V_{SLEEP(OFF)}$ is less than 1V, even logic level signals can be employed to disable and enable the IC.

**IR1155 General Description**

*Programmable Soft Start*
The soft start process controls the rate of rise of the voltage feedback loop error signal thus providing a linear control on RMS input current that the PFC converter will admit. The soft start time is essentially controlled by voltage error amplifier compensation components selected and is therefore user programmable to some degree based on desired loop crossover frequency.

*Gate Drive Capability*
The gate drive output stage of the IC is a totem pole driver with 1.5A peak current drive capability. The gate drive is internally clamped at 13V (Typ). Gate drive buffer circuits can be easily driven with the GATE pin of the IC to suit any system power level.

*System Protection Features*
IR1155 protection features include DC bus Overvoltage protection (OVP) via a dedicated pin, Open-loop protection (OLP), Cycle-by-cycle peak current limit (IPK LIMIT), Soft-current limit and VCC under voltage lock-out (UVLO).

- Overvoltage voltage protection (OVP) feature in IR1155 is achieved using a dedicated pin called the OVP/EN pin. The input of OVP comparator is connected the OVP pin. When the OVP pin voltage exceeds $V_{OVP}$, an overvoltage situation is detected and the gate drive is immediately terminated. The gate drive is re-enabled only after OVP pin voltage drops below $V_{OVP(RST)}$. The use of a dedicated OVP/EN pin ensures that the system is protected from catastrophic overvoltages, even if the feed-back loop (connected to the VFB pin) encounters any failure. This ensures the best possible system overvoltage protection against extremes of situations.

- Open Loop Protection (OLP) is activated whenever the VFB pin voltage falls below $V_{OLP}$ threshold. The gate drive is then immediately disabled, VCOMP is actively discharged and the IC is pushed into Stand-by mode. The IC will re-start (with soft-start) once the VFB pin voltage exceeds $V_{OLP}$ again. There is no voltage hysteresis associated with this feature. During start-up the IC is held in Stand-by until this pin exceeds $V_{OLP}$.

- Soft-current limit is an output voltage fold-back type protection feature that is encountered when the RMS current in the PFC converter exceeds a certain magnitude that causes the internal error signal of the voltage feedback, $V_m$ to saturate at its highest value. Amplitude of $V_m$ signal is directly proportional to the RMS input current admitted into the PFC converter. In effect, once $V_m$ saturates, the maximum RMS current admissible into the PFC converter has been encountered. Any attempt to increase the RMS current beyond this limit causes the IC to limit the duty cycle delivered to the PFC converter, which then has the effect of causing the DC bus voltage to droop i.e. output voltage folds-back. The current level at which $V_m$ saturates is closely related to the value of the current sense resistor selected for the PFC converter. In one way, this feature can be perceived to offer an overpower limitation of sorts at the conditions at which current sense design is performed (minimum VAC & maximum output power). For details, please refer to IR1155 Application Note.

- Cycle-by-cycle peak current limit protection instantaneously turns-off the gate output whenever the ISNS pin voltage exceeds $V_{ISNS(PK)}$ threshold in magnitude. The gate drive output is re-enabled only after the magnitude of the ISNS pin voltage drops below the $V_{ISNS(PK)}$ threshold. It is clarified that even though the IC operates based on average current mode control, since the averaging circuit is decoupled from the peak current limit comparator input, the IC is still able to provide instantaneous response to a system overcurrent condition. This protection feature incorporates a leading edge blanking circuit following the comparator to improve noise immunity.

- VCC Under Voltage Lockout protection maintains the IC in a low current consumption, UVLO mode during start-up if VCC pin voltage is less than the VCC turn-on threshold, $V_{CC,ON}$. In UVLO mode the current consumption is less than $I_{CC,START}$ which is typically about 200uA. Should VCC pin voltage should drop below UVLO threshold $V_{CC,\ UVLO}$ anytime after start-up, the IC is pushed back into UVLO mode (VCOMP pin is discharged) and VCC pin has to exceed $V_{CC,ON}$ again to re-start operation.

**IR1155 Pin Description**

**Pin COM:** This is ground potential pin of the IC. All internal devices are referenced to this point. A star-connection point, very close to this pin, is recommended in PCB lay-out in order to reference the return traces of the various control loops to the COM potential of the IC.

**Pin COMP:** External circuitry from this pin to ground compensates the system voltage loop and programs the soft start time. The COMP pin is essentially the output of the voltage error amplifier. VCOMP is actively discharged using an internal switch & resistance inside the IC whenever the IC is pushed into Stand-by mode (Open Loop Condition) or UVLO/Sleep mode. The IC is designed not to start-up (from UVLO, Sleep or Stand-by modes) when there is a pre-bias on VCOMP pin that is greater than $V_{COMP,START}$. The VCOMP-COM loop represents a very important control loop to the IC and hence a dedicated PCB trace loop is recommended for layout (star-connection to GND potential) for noise free, stable operation.

**Pin ISNS:** ISNS pin is the inverting input to the current sense amplifier of the IC. The voltage at this pin is the negative voltage drop sensed across the system current sense resistor and thus represents the inductor current sense signal to the IC for determining gate drive duty cycle. ISNS pin is also the inverting input to the cycle-by-cycle peak current limit comparator. Whenever this pin voltage exceeds $V_{ISNS(PK)}$ threshold in magnitude, the gate drive is instantaneously disabled. Any external filtering of the ISNS pin must be performed carefully in order to ensure that the integrity of the current sense signal is maintained for cycle-by-cycle protection.

**Pin FREQ:** This is the user-programmable frequency pin. The switching frequency is programmed by inserting a capacitor between FREQ & COM pins. A pair of current sources inside the IC source/sink current in/out of the capacitor alternately thus generating a constant-slope saw-tooth ramp signal between a pre-determined peak & valley voltage pair (typically between 2V to 4V). This saw-tooth signal is the oscillator signal of the IC. The frequency of operation of the IC can be programmed anywhere between 48kHz and 200kHz by suitably sizing the capacitor.

The FREQ-COM loop represents yet another very important control loop to the IC and hence a dedicated PCB trace loop is recommended in lay-out (star-connection to GND potential) for noise free, stable operation.

**Pin OVP/EN:** The OVP/EN pin is connected to the input of the overvoltage comparator and is used to detect output overvoltage situations. The output voltage information is communicated to the OVP pin using a resistive divider. This pin also serves the second purpose of an ENABLE pin. The OVP/EN pin can be used to activate the IC into “micropower sleep” mode by pulling the voltage on this pin below the $V_{SLEEP}$ threshold.

**Pin VFB:** The converter output voltage is sensed via a resistive divider and fed into this pin. VFB pin is the inverting input of the output voltage error amplifier. The non-inverting input of this amplifier is connected to an internal 5V reference. The impedance of the divider string must be low enough that it does not introduce substantial error due to the input bias currents of the amplifier, yet high enough to minimize power dissipation. Typical value of external divider impedance will be 1MΩ. VFB pin is also the inverting input to the Open Loop comparator. The IC is held in Stand-by Mode whenever VFB pin voltage is below $V_{OLP}$ threshold.

**Pin VCC:** This is the supply voltage pin of the IC and sense node for the under-voltage lock out circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, $V_{CC,UVLO}$ without damage to the IC. This pin is not internally clamped.

**Pin GATE:** This is the gate drive output of the IC. This drive voltage is internally clamped to 13V(Typ) and provides a drive current of ±1.5A peak with matched rise and fall times.

**IR1155 Modes of operation (refer to States & Transitions Diagram)**

**UVLO/Sleep Mode:** The IC is in the UVLO/Sleep mode when either the VCC pin voltage is below $V_{CC,UVLO}$ and/or the OVP/EN pin voltage is below $V_{SLEEP}$. The UVLO/Sleep mode is accessible from any other state of operation. This mode can be actively invoked by pulling the OVP/EN pin below the Sleep threshold $V_{SLEEP}$ even if VCC pin voltage is above $V_{CC,ON}$. In the UVLO/Sleep state, the gate drive circuit is inactive, most of the internal circuitry is unbiased and the IC draws a quiescent current of $I_{SLEEP}$ which is typically 200uA or less. Also, the internal logic of the IC ensures that whenever the UVLO/Sleep mode is actively invoked, the COMP pin is actively discharged below $V_{COMP,START}$ prior to entering the sleep mode, in order to facilitate soft-start upon resumption of operation.

**Stand-by Mode:** The IC is placed in Stand-by mode whenever an Open-loop situation is detected. An open-loop situation is sensed anytime VFB pin voltage is less than $V_{OLP}$. All internal circuitry is biased in the Stand-by Mode, but the gate is inactive and the IC draws a few mA of current. This state is accessible from any other state of operation of the IC. COMP pin is actively discharged to below $V_{COMP,START}$ whenever this state is entered from normal operation in order to facilitate soft-start upon resumption of operation.

**Soft Start Mode:** During system start-up, the soft-start mode is activated once the VCC voltage has exceeded $V_{CC,ON}$, the VFB pin voltage has exceeded $V_{OLP}$ and OVP pin voltage has exceeded $V_{SLEEP(ON)}$. The soft start time is the time required for the VCOMP voltage to charge through its entire dynamic range i.e. through $V_{COMP,EFF}$. As a result, the soft-start time is dependent upon the component values selected for compensation of the voltage loop on the COMP pin. As VCOMP voltage raises gradually, the IC allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current amplitude contributes to reducing system component stress during start-up. It is clarified that, during soft-start, the IC is capable of full duty cycle modulation (from 0% to MAX DUTY), based on the instantaneous ISNS signal from system current sensing. .

For all practical purposes, the Soft-start mode of the IC is the same as the Normal mode (only difference being that the DC bus voltage is approaching the regulation point). All protection functions of the IC are active during soft-start mode.

**Normal Mode:** The IC enters the normal operating mode seamlessly following conclusion of soft-start. At this point the DC bus is well regulated and all protection functions of the IC are active. If, from the normal mode, the IC is pushed into either a Stand-by mode or Sleep mode then COMP pin is actively discharged below $V_{COMP,START}$ and system will go through soft-start upon resumption of operation.

**OVP Mode:** The IC enters OVP fault mode whenever an overvoltage condition is detected. A system overvoltage condition is recognized when OVP/EN pin voltage exceeds $V_{OVP}$ threshold. When this happens the IC immediately disables the gate drive. The gate drive is re-enabled only when OVP/EN pin voltage is less than $V_{OVP(RST)}$ threshold. This state is accessible from both the soft start and normal modes of operation.

**IPK LIMIT Mode:** The IC enters IPK LIMIT fault mode whenever the magnitude of ISNS pin voltage exceeds the $V_{ISNS(PK)}$ threshold triggering cycle-by-cycle peak over current protection. When this happens, the IC immediately disables the gate drive. Gate drive is re-enabled when magnitude of ISNS pin voltage drops below $V_{ISNS(PK)}$ threshold. This state is accessible from both the soft start and normal modes of operation.

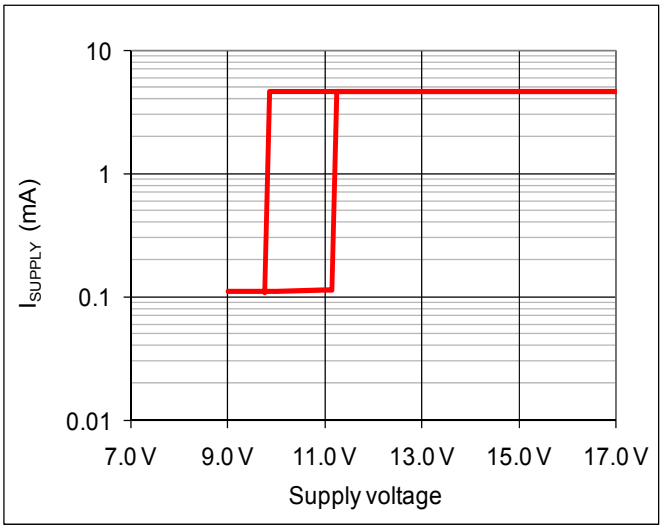



**Figure 1: Supply Current vs. Supply Voltage**

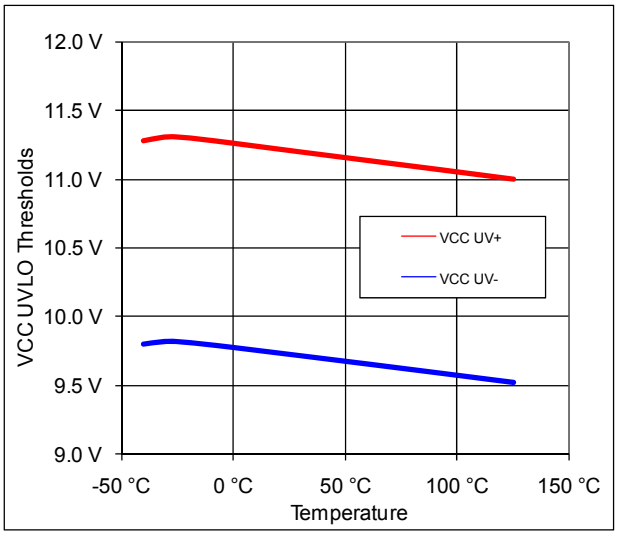



**Figure 2: Undervoltage Lockout vs. Temperature**

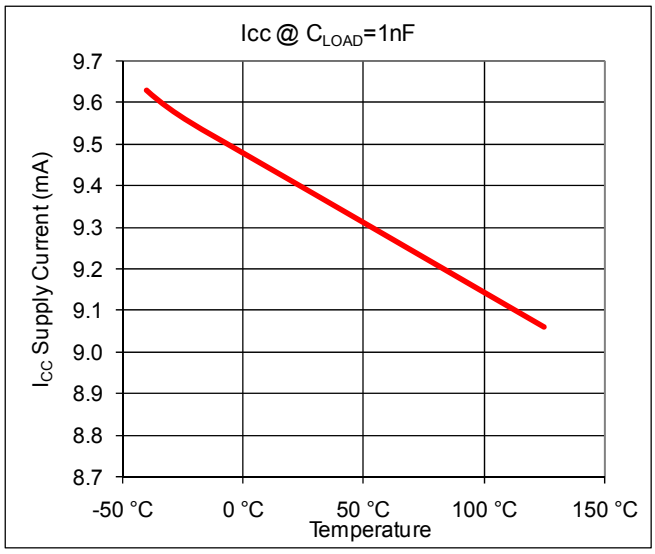



**Figure 3: Icc Current vs. Temperature (@181kHz frequency)**

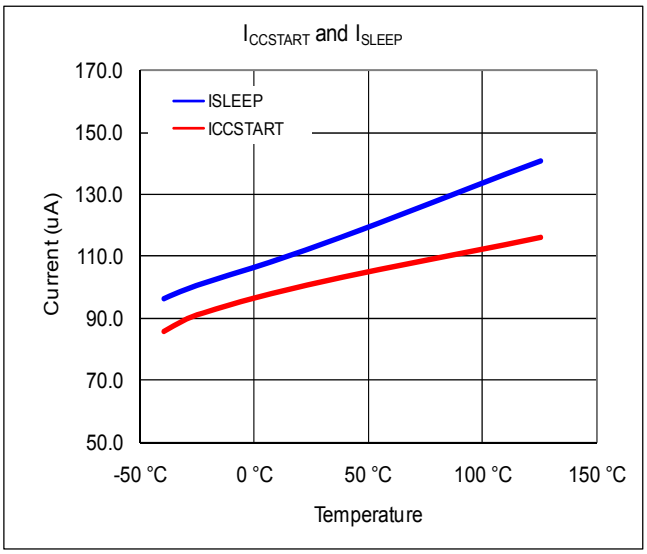



**Figure 4: Startup Current and Sleep Current vs. Temperature**

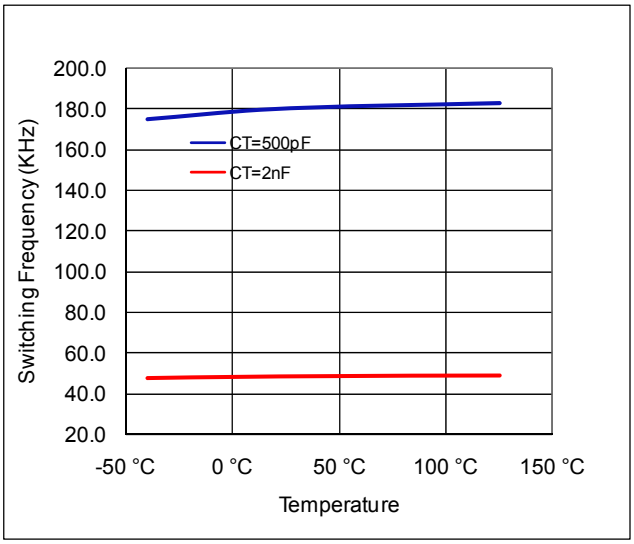



**Figure 5: Switching Frequency vs. Temperature**

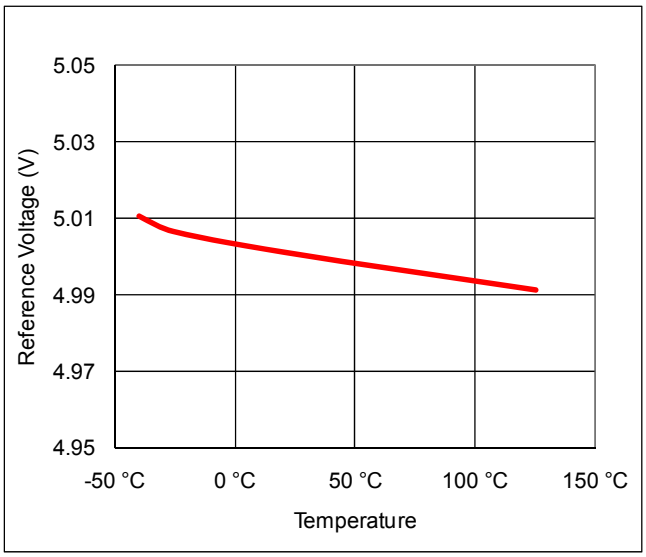



**Figure 6: Reference Voltage vs. Temperature**

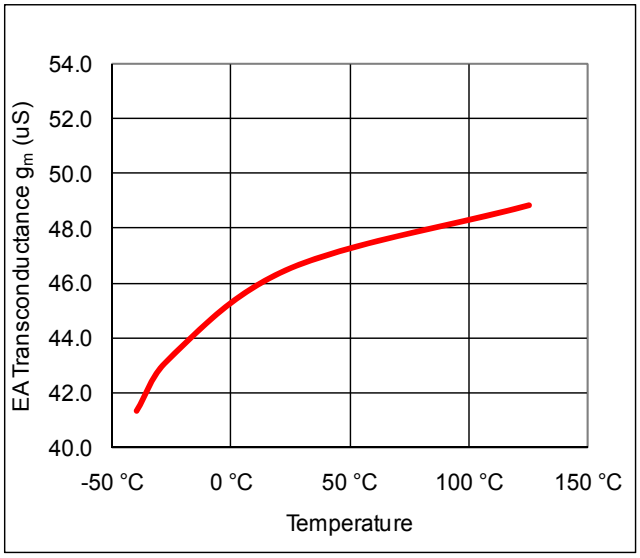



**Figure 7: Voltage Error Amplifier Transconductance vs. Temperature**

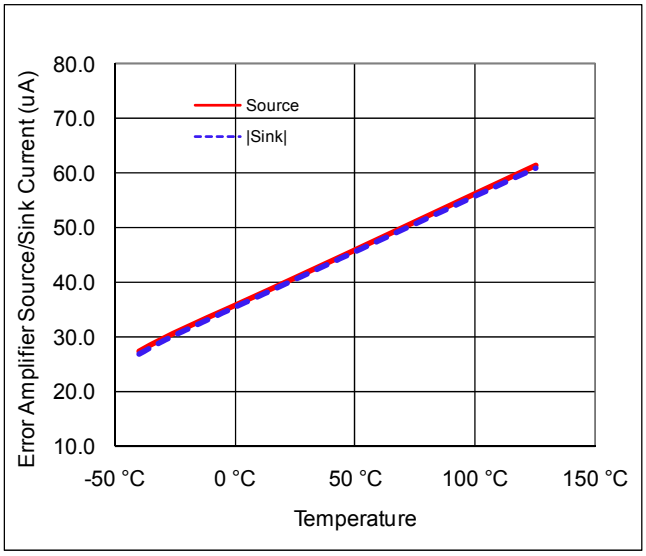



**Figure 8: Voltage Error Amplifier Source & Sink Current vs. Temperature**

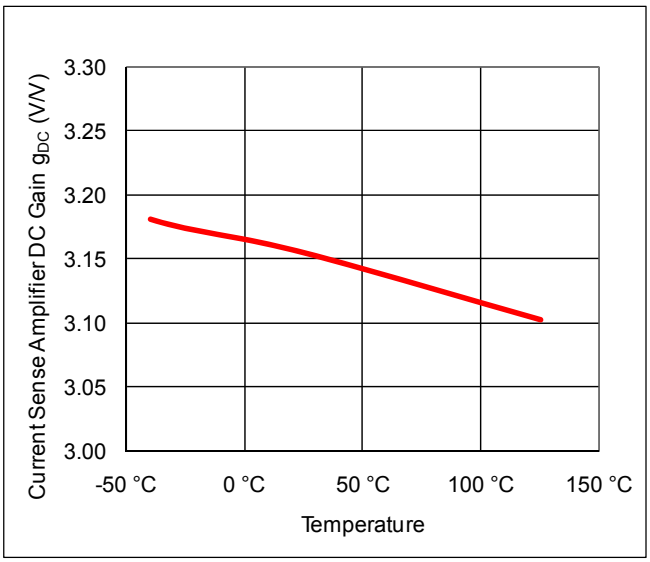



**Figure 9: Current Amplifier DC Gain vs. Temperature**

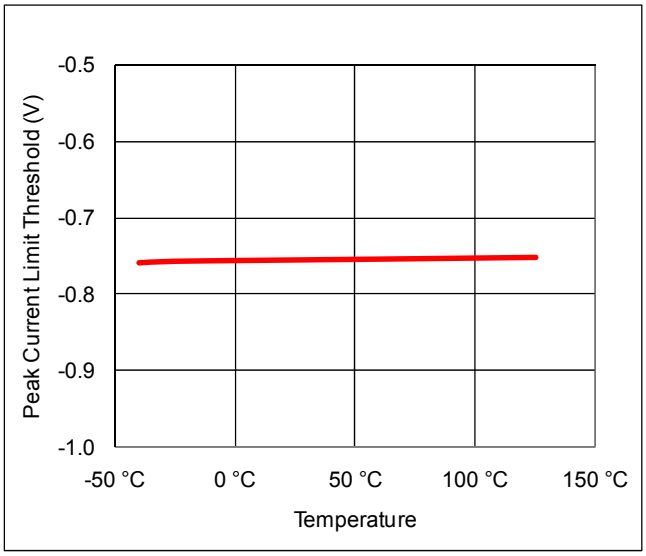



**Figure 10: Peak Current Limit Threshold $V_{ISNS(PK)}$ vs. Temperature**

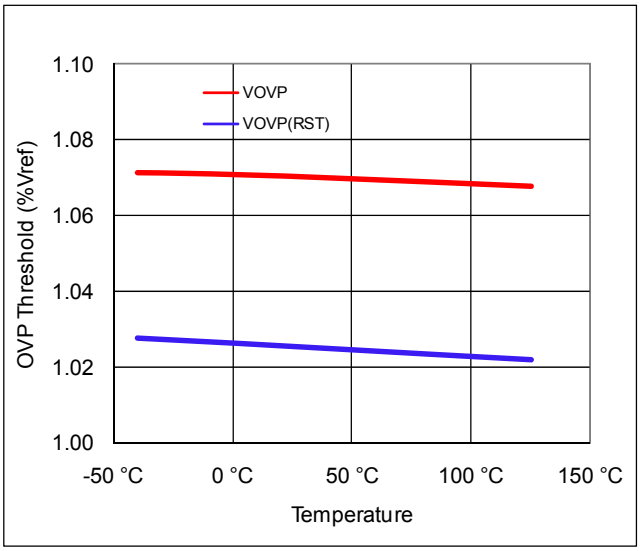



**Figure 11: Over Voltage Protection Thresholds vs. Temperature**

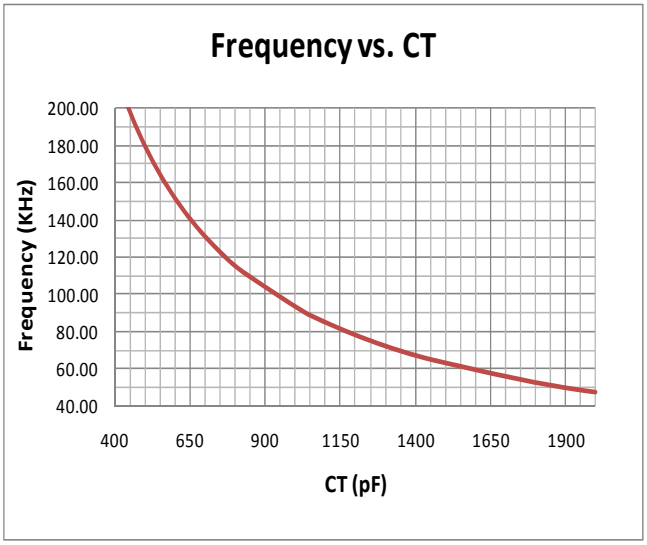
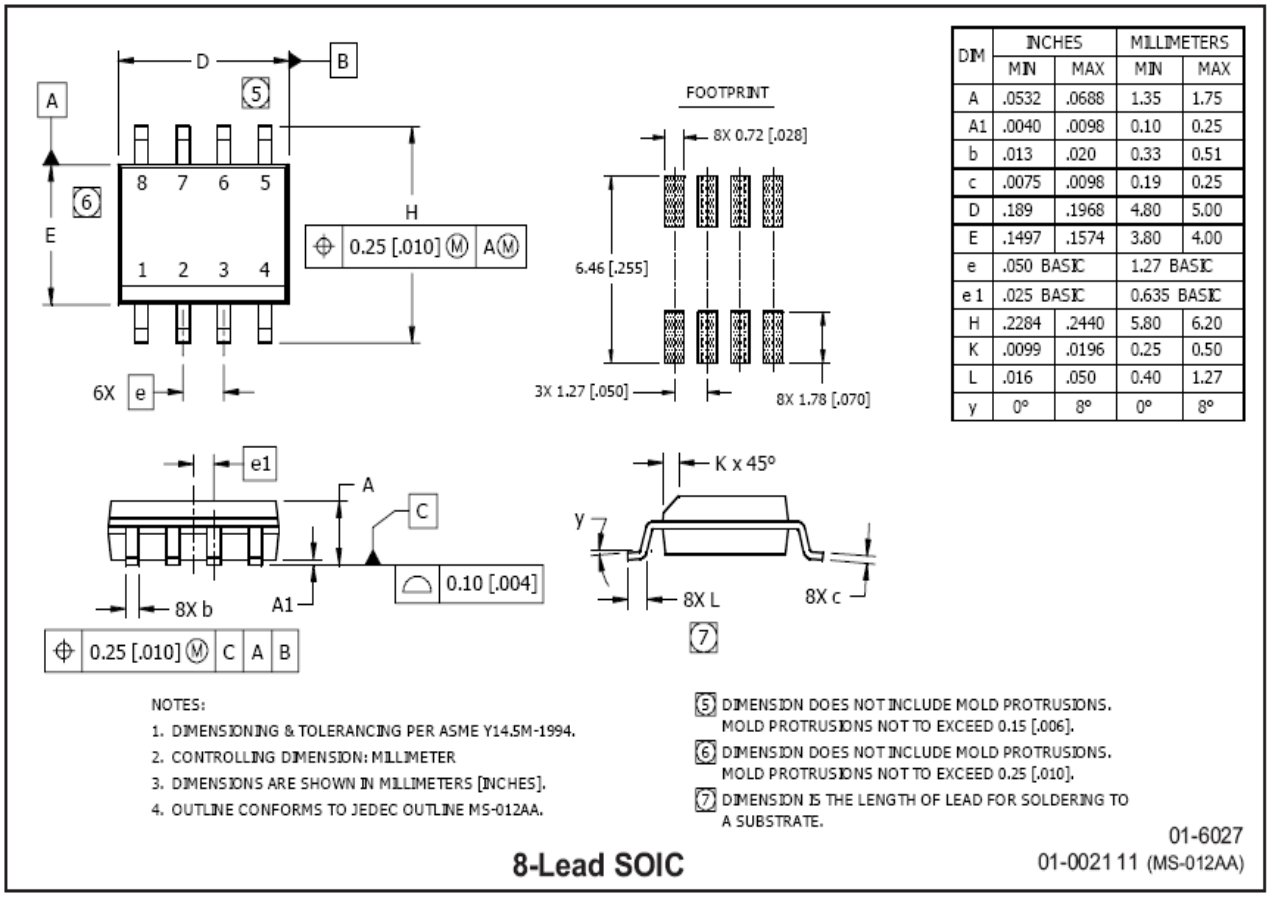



**Figure 12: Oscillator Frequency vs. Programming Capacitor**

## Package Details: SOIC8N




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

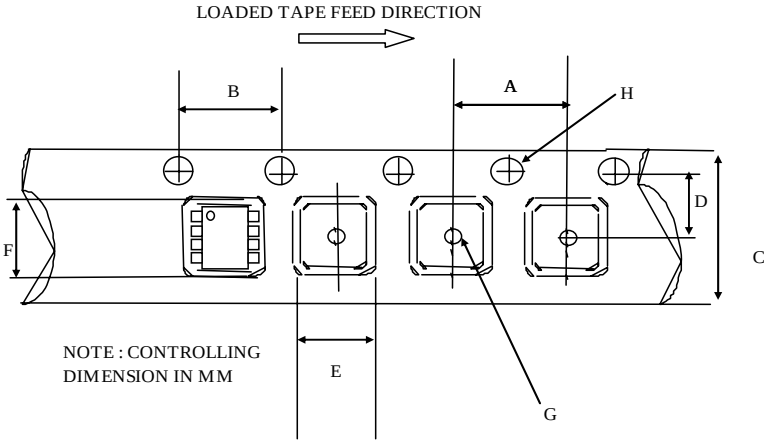
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

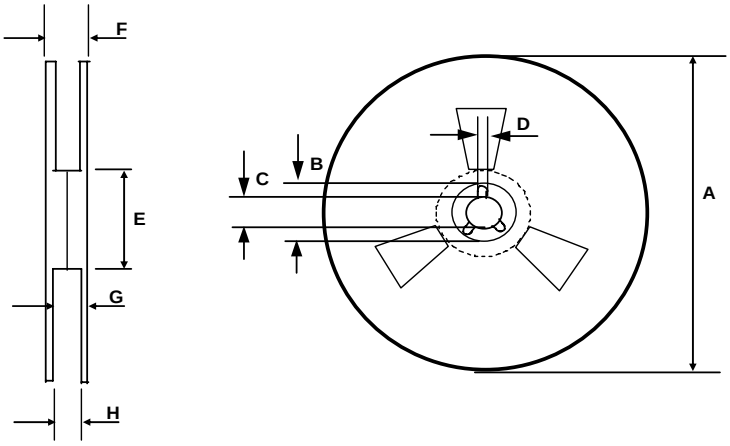
**8-Lead SOIC**

## Tape and Reel Details: SOIC8N




CARRIER TAPE DIMENSION FOR 8SOICN

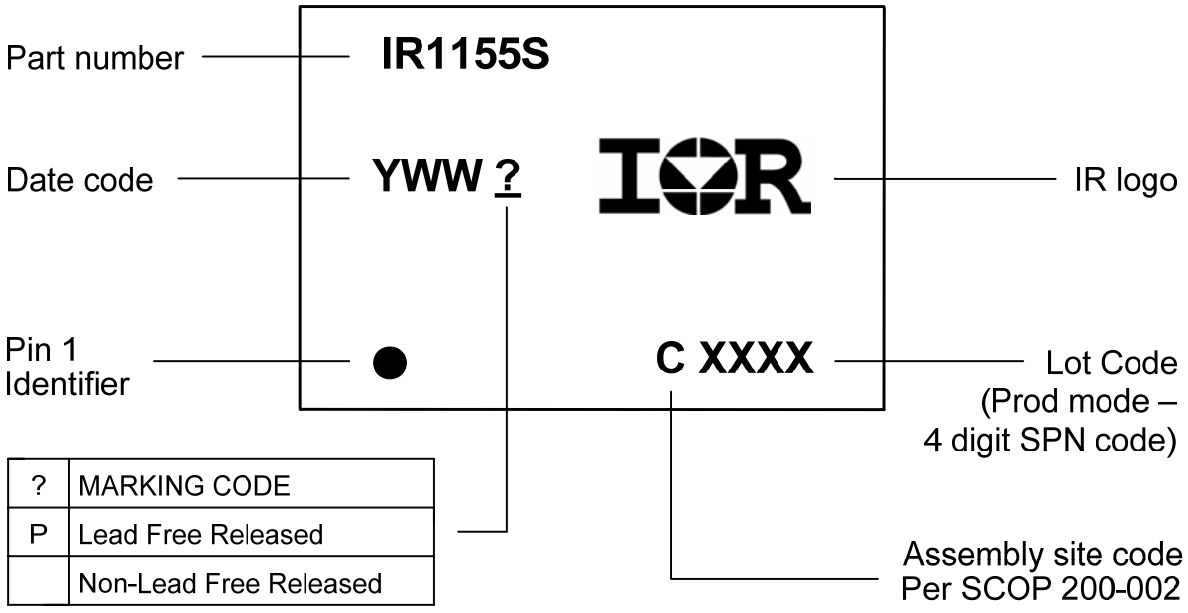
| Code | Metric | | Imperial | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 8SOICN

| Code | Metric | | Imperial | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

## Part Marking Information




| | |
|---|---|
| ? | MARKING CODE |
| P | Lead Free Released |
| | Non-Lead Free Released |

## Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IR1155S | SOIC8N | Tube/Bulk | 95 | IR1155SPBF |
| | | Tape and Reel | 2500 | IR1155STRPBF |



For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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Tel: (310) 252-7105