



Description

The S3165 SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 transceiver is one of the latest additions to AMCC's OC-48 product family. The S3165 device provides fully integrated serialization/de-serialization capabilities for low power SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 applications. The device performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 transmission standards. The standard operating range is from 2.125 Gbps to 3.00 Gbps and the device incorporates multiple dividers to cover the rates for the protocols listed under General Features. Figure 1, *System Block Diagram*, shows a typical network application.

Overview

The S3165 can be used to implement the front end of SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution. The device utilizes on-chip clock synthesis PLL components that allow the use of a slower external clock reference, 155.52 MHz (or equivalent rate), in support of existing system clocking schemes. The low-jitter, 16-bit differential LVPECL/LVDS data path or single-ended LVPECL option interfaces guarantee compliance with the bit-error rate requirements of the Telecordia and ITU-T standards.

S4801 Amazon	STS-48c POS/ATM SONET Mapper
S4802 Missouri	SONET/SDH STS-48/STM-16 Framer/ Pointer Processor
S4804 Rhine	STS-48 SONET/SDH Framer and POS/ATM Mapper
S4805 Danube	SONET/SDH STS-48/STM-16 Framer/ Pointer Processor
S19201 Indus	STS-192 SONET/SDH Inter-leaver/ Disinterleaver

- At a Glance -

General Features

- Operational from 2.125 Gbps to 3.00 Gbps
- Supports:
 - OC-48 with or w/o FEC
 - OC-24 with or w/o FEC
 - OC-12 with or w/o FEC
 - OC-3 with or w/o FEC
 - HDTV (1.485 Gbps)
 - D1 (1.38 Gbps)
 - Fibre Channel (1062 Mbps)
 - 2 x Fibre Channel (2.124 Gbps)
 - Gigabit Ethernet (1.25 Gbps)
 - DTV (143.18 Mbps)
 - ESCON (200 Mbps)
- 650 mW typical power
- Integrated clock data recovery
- On-chip high-frequency PLL for clock generation and clock recovery
- Reference frequency of 155.52 to 166.63 MHz
- RX and TX reference selectable
- Interface to LVCMOS/LVTTL logic
- Internal input termination option built-in
- 16-bit differential LVPECL/LVDS data path or single-ended LVPECL option

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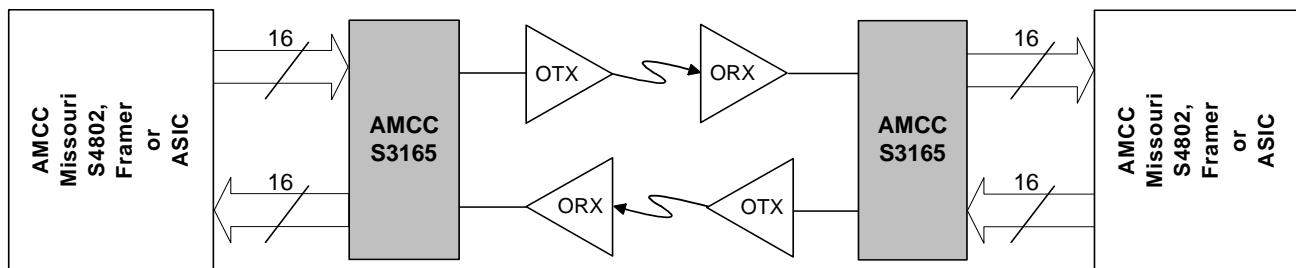


Figure 1. System Block Diagram

The sequence of operations is as follows:

Transmitter Operations

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial data output

Receiver Operations

1. Clock and Data recovery from serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

Internal clocking and control functions are transparent to the user.

Prefix	Device	Package	Temperature Grade
S – Integrated Circuit	3165	PB - 196 PBGA	I - Industrial

X XXXX XX X
Prefix Device Package Temp

Figure 2. S3165 Ordering Information

- 196 PBGA package
- Diagnostic and line loopback mode
- Support serial loop timing mode
- Lock detect
- Signal detect input with polarity select
- Low Jitter LVPECL/LVDS interface
- Internal FIFO to decouple transmit clocks
- Dual 1.2 V and 3.3 V/2.5V supply
- Complies with Telcordia and ITU-T specifications
- Built-in self test

Transmitter Features

- Reference frequency of 155.52 MHz (or equivalent rate)
- 155.52 MHz (or equivalent rate) clock output
- Internal, self-initializing FIFO to decouple transmit clocks

Receiver Features

- Recovers clock from data
- Low-jitter CML differential or single-ended serial interface
- Reference frequency of 155.52 MHz (or equivalent rate)

Applications

- SONET/SDH-based transmission systems
- SONET/SDH modules
- Wavelength Division Multiplexing (WDM)
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber Optic Terminators
- Fiber Optic Test Equipment

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