Description

The S3157 GPON transceiver chip is a fully integrated serialization/ deserialization GPON OC-48/24/12 transceiver interface device. The S3157 receives an OC-48/24/12 Non-Return to Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with GPON transmission standards. The device is suitable for GPON-based applications. The figure below shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Locked Loop (PLL) on the S3157 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 or 166.63 MHz reference clock in support of existing system clocking schemes.

The low jitter LVPECL interface is compliant with the bit-error rate requirements of the ITU-T standards. The S3157 is packaged in a 196 PBGA, offering designers a small package outline.

Overview

The S3157 transceiver implements GPON serialization/deserialization, and transmission functions. This chip can be used to implement the front end of GPON equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The S3157 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

Due to the asynchronous nature of the GPON, the FPGA that connects to the S3157 has to accommodate for the 1/2 upstream data rate.

– At a Glance –

Features

- 650 mW typical power
- Integrated clock data recovery
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports OC-48/24/12 rates
- Reference frequency of 155.52 to 166.63 MHz
- RX and TX reference selectable
- Interface to LVCMOS/LVTTL logic
- Internal input termination option built-in
- 16-bit differential LVPECL/ LVDS data path or single-ended LVPECL option
- 196 PBGA package
- Diagnostic and line loopback mode
- Support serial loop timing mode
- Lock detect
- Signal detect input with polarity select
- Low Jitter LVPECL/LVDS interface
- Internal FIFO to decouple transmit clocks

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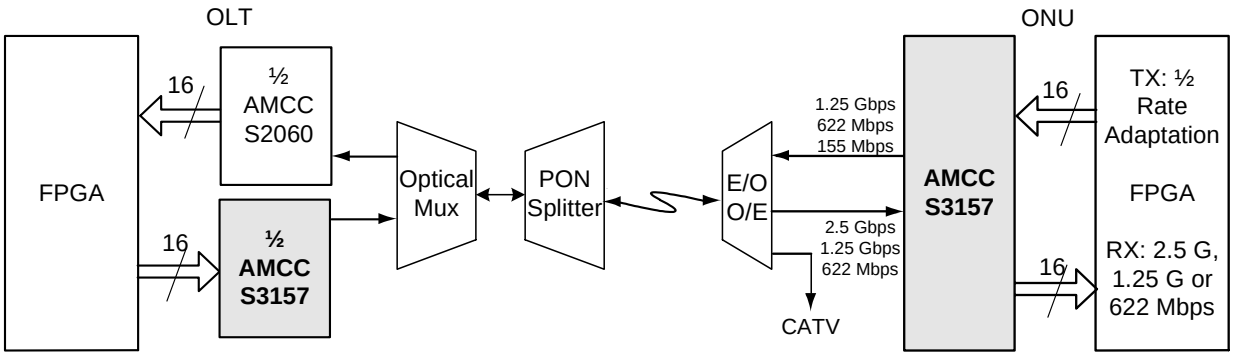

Figure 1. System Block Diagram

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AMCC Suggested Interface Device

AMCC S2060	Gigabit Ethernet Transceiver

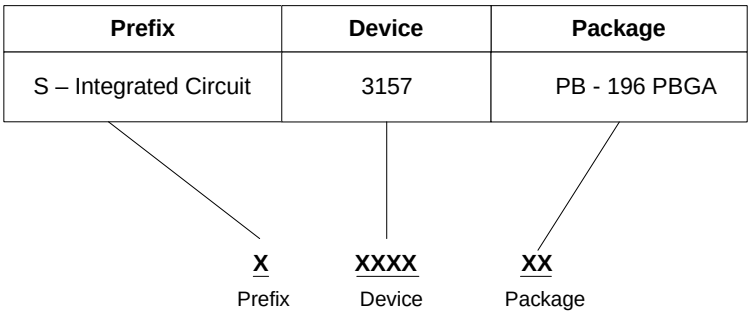

Figure 2. S3157 Ordering Information

- Dual 1.2 V and 3.3 V/2.5V supply
- Complies with ITU-T specifications
- Built-in self test

Applications

- GPOS-based transmission systems
- GPON ONU (Optical Network Unit)
- GPON OLT (Optical Line Termination)
- GPON test equipment

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