

# DATA SHEET

## **74F569**

4-bit bidirectional binary synchronous counter (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

# 4-bit bidirectional binary synchronous counter (3-State)

# 74F569

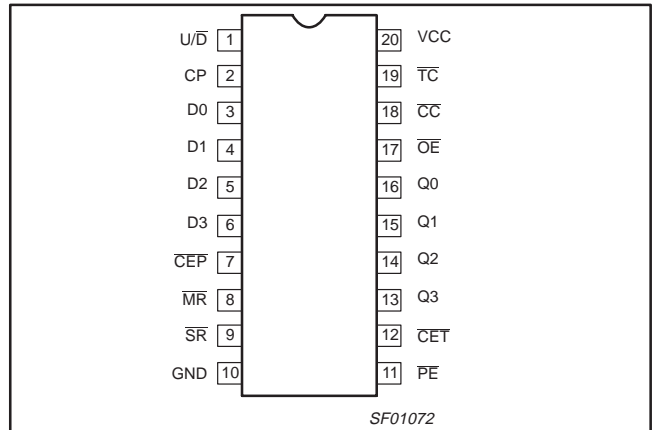
## FEATURES

- 4-bit bidirectional counting – binary counter
- Synchronous counting and loading
- Look ahead carry capability for easy cascading
- Preset capability for programmable operation
- Master Reset ( $\overline{MR}$ ) overrides all other inputs
- Synchronous Reset ( $\overline{SR}$ ) overrides counting and parallel loading
- Clock Carry ( $\overline{CC}$ ) output to be used as a clock for flip-flops, register and counters
- 3-State outputs for bus organized systems

## DESCRIPTION

The 74F569 is a fully synchronous Up/Down binary counter. It features preset capabilities for programmable operation, carry look ahead for programmable operation, carry look ahead for easy cascading, and U/D input to control the direction of counting. For maximum flexibility there are both Synchronous and Master Reset inputs as well as both Clocked Carry ( $\overline{CC}$ ) and Terminal Count ( $\overline{TC}$ ) outputs. All state changes except Master Reset are initiated by rising edge of the clock. A High signal on the Output Enable ( $\overline{OE}$ ) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

## PIN CONFIGURATION

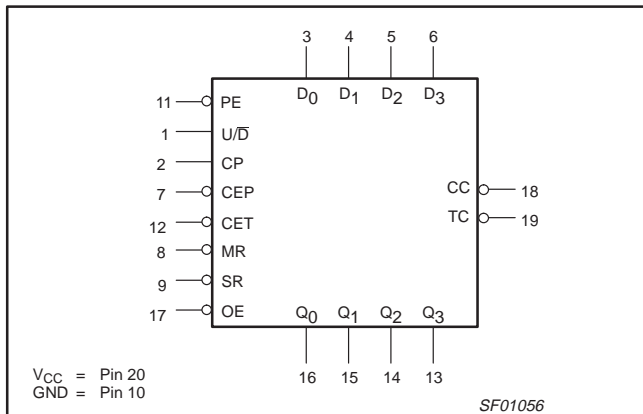


| TYPE   | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|-------------------|--------------------------------|
| 74F569 | 115MHz            | 40mA                           |

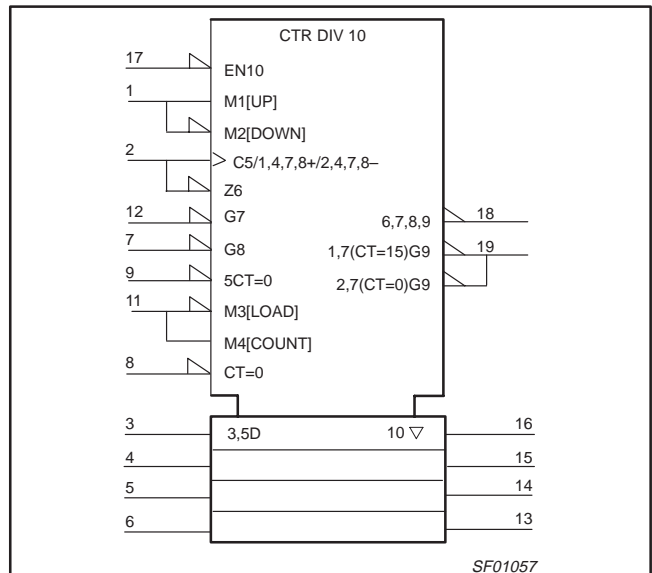
## ORDERING INFORMATION

| DESCRIPTION        | ORDER CODE   | PKG. DWG. # |
|--------------------|--|-------------|
|                    | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ ,<br>$T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ |             |
| 20-pin plastic DIP | N74F569N   | SOT146-1    |
| 20-pin plastic SO  | N74F569D   | SOT163-1    |

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## 4-bit bidirectional binary synchronous counter (3-State)

74F569

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS              | DESCRIPTION                              | 74F(U.L.)<br>HIGH/LOW | LOAD VALUE<br>HIGH/LOW |
|-------------------|--|-----------------------|------------------------|
| D0 - D3           | Parallel data inputs                     | 1.0/1.0               | 20µA/0.6mA             |
| $\overline{CEP}$  | Count Enable parallel input (active Low) | 1.0/1.0               | 20µA/0.6mA             |
| $\overline{CET}$  | Count Enable Trickle input (active Low)  | 1.0/2.0               | 20µA/1.2mA             |
| CP                | Clock input (active rising edge)         | 1.0/1.0               | 20µA/0.6mA             |
| PE                | Parallel Enable input (active Low)       | 1.0/2.0               | 20µA/1.2mA             |
| U/ $\overline{D}$ | Up/Down count control input              | 1.0/1.0               | 20µA/0.6mA             |
| $\overline{OE}$   | Output Enable input                      | 1.0/1.0               | 20µA/0.6mA             |
| $\overline{MR}$   | Master Reset input (active Low)          | 1.0/1.0               | 20µA/0.6mA             |
| $\overline{SR}$   | Synchronous Reset (active Low)           | 1.0/1.0               | 20µA/0.6mA             |
| TC                | Terminal count output (active Low)       | 50/33                 | 1.0mA/20mA             |
| $\overline{CC}$   | Clocked carry output (active Low)        | 50/33                 | 1.0mA/20mA             |
| Q0 - Q3           | Data outputs                             | 150/40                | 3.0mA/24mA             |

**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

## FUNCTIONAL DESCRIPTION

The 74F569 counts in the modulo-16 binary sequence. From state 0 (LLLL) it will increment to 15 in the up mode; in the down mode it will decrement from 15 to 0. The clock inputs of all flip-flops are driven parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse ( $\overline{CP}$ ) input.

The circuit has five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Six control inputs—Master Reset ( $\overline{MR}$ ), Synchronous Reset ( $\overline{SR}$ ), Count Enable Trickle ( $\overline{CET}$ ), Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel ( $\overline{CEP}$ ), and the Up/Down (U/ $\overline{D}$ ) input – determine the mode of operation, as shown in the Function Table.

A Low signal on  $\overline{MR}$  overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on  $\overline{SR}$  overrides counting and parallel loading and allows the Q output to go Low on the next rising edge of CP. A Low signal on  $\overline{PE}$  overrides counting and allows information on the parallel data (Dn) inputs to be loaded into the flip-flops on the next rising edge of CP. With  $\overline{MR}$ ,  $\overline{SR}$ , and  $\overline{PE}$  High,  $\overline{CEP}$  and  $\overline{CET}$  permit counting when both are Low. Conversely, a High signal on either  $\overline{CEP}$  and  $\overline{CET}$  inhibits counting.

The 74F569 uses edge-triggered flip-flops and changing the  $\overline{SR}$ ,  $\overline{PE}$ ,  $\overline{CEP}$ ,  $\overline{CET}$  or U/ $\overline{D}$  inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally High and goes Low provided  $\overline{CET}$  is Low, when the counter reaches zero in the down mode, or reaches maximum 15 in the up mode

TC will then remain Low until a state change occurs by counting or presetting, or until U/ $\overline{D}$  or  $\overline{CET}$  is changed.

To implement synchronous multistage counters, the connections between the TC output and the  $\overline{CEP}$  and  $\overline{CET}$  inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for a simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative  $\overline{CET}$  to TC delays of the intermediate stages, plus the  $\overline{CET}$  to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look ahead connections in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from Max to Min in the up mode, or Min to Max in the down mode, to start its final cycle. Since this takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the  $\overline{CEP}$  to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, register or counters.

For such applications, the Clocked Carry ( $\overline{CC}$ ) output is provided. The  $\overline{CC}$  output is normally High. When  $\overline{CEP}$ ,  $\overline{CET}$ , and TC are Low, the  $\overline{CC}$  output will go Low, when the clock next goes Low and will stay Low until the clock goes High again; as shown in the CC Function Table. When the Output Enable ( $\overline{OE}$ ) is Low, the parallel data outputs Q0–Q3 are active and follow the flip-flop Q outputs. A High signal on  $\overline{OE}$  forces Q0–Q3 to the High impedance state but does not prevent counting, loading or resetting.

## LOGIC EQUATIONS:

Count Enable =  $\overline{CEP} \times \overline{CET} \times \overline{PE}$

Up:  $TC = Q0 \times Q1 \times Q2 \times Q3 \times (Up) \times \overline{CET}$

Down:  $TC = Q0 \times Q1 \times Q2 \times Q3 \times (Down) \times \overline{CET}$

# 4-bit bidirectional binary synchronous counter (3-State)

74F569

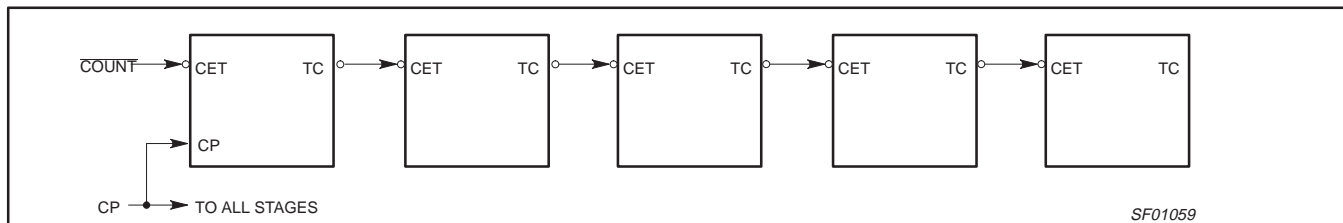


Figure 1. Multistage Counter with Ripple Carry

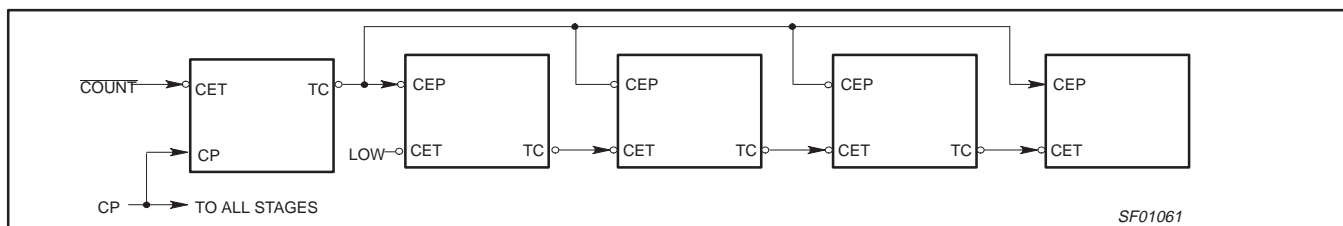
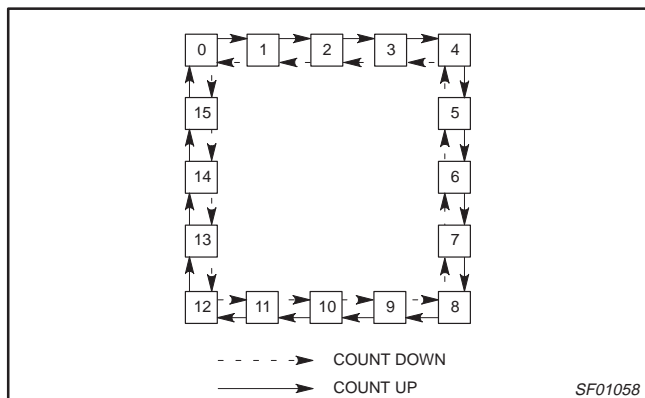


Figure 2. Multistage Counter with Look-Ahead Carry

### STATE DIAGRAM



### CC FUNCTION TABLE

| INPUTS |    |     |     |     |    | OUTPUT |
|--------|----|-----|-----|-----|----|--------|
| SR     | PE | CEP | CET | TC* | CP | CC     |
| L      | X  | X   | X   | X   | X  | H      |
| X      | L  | X   | X   | X   | X  | H      |
| X      | X  | H   | X   | X   | X  | H      |
| X      | X  | X   | H   | X   | X  | H      |
| X      | X  | X   | X   | H   | X  | H      |
| H      | H  | L   | L   | L   |    |        |

\* = TC is generated internally  
 H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 = Low Pulse

### FUNCTION TABLE

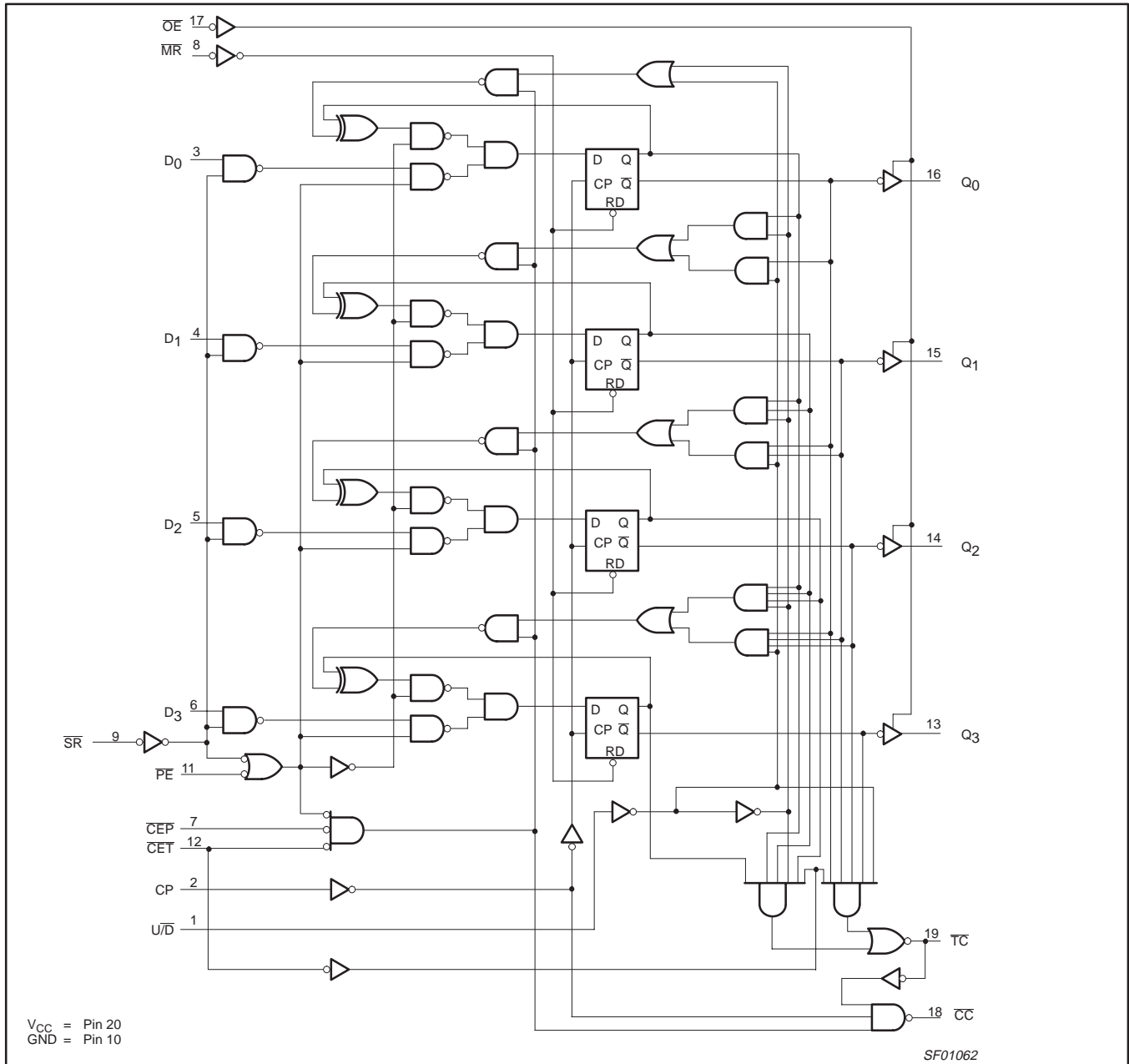
| INPUTS |    |    |     |     |     |    | OPERATING MODE         |
|--------|----|----|-----|-----|-----|----|------------------------|
| MR     | SR | PE | CEP | CET | U/D | CP |                        |
| L      | X  | X  | X   | X   | X   | X  | Asynchronous reset     |
| h      | l  | X  | X   | X   | X   | ↑  | Synchronous reset      |
| h      | h  | l  | X   | X   | X   | ↑  | Parallel load          |
| h      | h  | h  | l   | l   | h   | ↑  | Count Up (increment)   |
| h      | h  | h  | l   | l   | l   | ↑  | Count Down (decrement) |
| h      | H  | H  | H   | X   | X   | X  | Hold (do nothing)      |
| h      | H  | H  | X   | H   | X   | X  |                        |

H = High voltage level  
 h = High voltage level one setup time prior to the Low-to-High clock transition  
 L = Low voltage level  
 l = Low voltage level one setup time prior to the Low-to-High clock transition  
 X = Don't care  
 ↑ = Low-to-High clock transition

# 4-bit bidirectional binary synchronous counter (3-State)

74F569

## LOGIC DIAGRAM



## 4-bit bidirectional binary synchronous counter (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL           | PARAMETER                                      | RATING                         | UNIT |    |
|------------------|--|--------------------------------|------|----|
| V <sub>CC</sub>  | Supply voltage                                 | -0.5 to +7.0                   | V    |    |
| V <sub>IN</sub>  | Input voltage                                  | -0.5 to +7.0                   | V    |    |
| I <sub>IN</sub>  | Input current                                  | -30 to +5                      | mA   |    |
| V <sub>OUT</sub> | Voltage applied to output in High output state | -0.5 to +V <sub>CC</sub>       | V    |    |
| I <sub>OUT</sub> | Current applied to output in Low output state  | $\overline{TC}, \overline{CC}$ | 40   | mA |
|                  |  | Q <sub>n</sub>                 | 48   | mA |
| T <sub>amb</sub> | Operating free-air temperature range           | 0 to +70                       | °C   |    |
| T <sub>stg</sub> | Storage temperature                            | -65 to +150                    | °C   |    |

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL           | PARAMETER                            | LIMITS                         |     |     | UNIT |
|------------------|--------------------------------------|--------------------------------|-----|-----|------|
|                  |                                      | MIN                            | NOM | MAX |      |
| V <sub>CC</sub>  | Supply voltage                       | 4.5                            | 5.0 | 5.5 | V    |
| V <sub>IH</sub>  | High-level input voltage             | 2.0                            |     |     | V    |
| V <sub>IL</sub>  | Low-level input voltage              |                                |     | 0.8 | V    |
| I <sub>IK</sub>  | Input clamp current                  |                                |     | -18 | mA   |
| I <sub>OH</sub>  | High-level output current            | $\overline{TC}, \overline{CC}$ |     | -1  | mA   |
|                  |                                      | Q <sub>n</sub>                 |     | -3  | mA   |
| I <sub>OL</sub>  | Low-level output current             | $\overline{TC}, \overline{CC}$ |     | 20  | mA   |
|                  |                                      | Q <sub>n</sub>                 |     | 24  | mA   |
| T <sub>amb</sub> | Operating free-air temperature range | 0                              |     | 70  | °C   |

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL           | PARAMETER   | TEST CONDITIONS <sup>NO TAG</sup>   | LIMITS                |               |      | UNIT |    |
|------------------|---|---|-----------------------|---------------|------|------|----|
|                  |   |   | MIN                   | TYP<br>NO TAG | MAX  |      |    |
| V <sub>OH</sub>  | High-level output voltage                               | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,<br>V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX | ±10%V <sub>CC</sub>   | 2.4           |      | V    |    |
|                  |   |   | ±5%V <sub>CC</sub>    | 2.7           | 3.3  | V    |    |
| V <sub>OL</sub>  | Low-level output voltage                                | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,<br>V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX | ±10%V <sub>CC</sub>   |               | 0.35 | 0.50 | V  |
|                  |   |   | ±5%V <sub>CC</sub>    |               | 0.35 | 0.50 | V  |
| V <sub>IK</sub>  | Input clamp voltage                                     | V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>                                       |                       | -0.73         | -1.2 | V    |    |
| I <sub>I</sub>   | Input current at maximum input voltage                  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V  |                       |               | 100  | μA   |    |
| I <sub>IH</sub>  | High-level input current                                | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V  |                       |               | 20   | μA   |    |
| I <sub>IL</sub>  | Low-level input current                                 | Others  |                       |               | -0.6 | mA   |    |
|                  |   | $\overline{CET}, \overline{PE}$   |                       |               | -1.2 | mA   |    |
| I <sub>OZH</sub> | Off-state output current,<br>High-level voltage applied | V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V  |                       |               | 50   | μA   |    |
| I <sub>OZL</sub> | Off-state output current,<br>High-level voltage applied | V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V  |                       |               | -50  | μA   |    |
| I <sub>OS</sub>  | Short-circuit output current <sup>NO TAG</sup>          | V <sub>CC</sub> = MAX   | -60                   |               | -150 | mA   |    |
| I <sub>CC</sub>  | Supply current (total)                                  | I <sub>CCH</sub>  |                       | 38            | 60   | mA   |    |
|                  |   | I <sub>CCL</sub>  | V <sub>CC</sub> = MAX |               | 43   | 62   | mA |
|                  |   | I <sub>CCZ</sub>  |                       | 40            | 60   | mA   |    |

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 4-bit bidirectional binary synchronous counter (3-State)

74F569

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL                               | PARAMETER  |                | TEST CONDITIONS            | LIMITS   |             |              |   |              | UNIT     |
|--------------------------------------|--|----------------|----------------------------|--|-------------|--------------|---|--------------|----------|
|                                      |  |                |                            | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |              | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |              |          |
|                                      |  |                |                            | MIN  | TYP         | MAX          | MIN   | MAX          |          |
| f <sub>MAX</sub>                     | Maximum clock frequency  | Q <sub>n</sub> | Waveform 1                 | 100  | 115         |              | 90  |              | MHz      |
|                                      |  | CC, TC         | Waveform 2                 | 50   | 65          |              | 45  |              | MHz      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to Q <sub>n</sub> (PE, High or Low)      |                | Waveform 1                 | 3.0<br>4.0   | 6.0<br>7.5  | 9.5<br>11.0  | 3.0<br>4.0  | 10.0<br>12.0 | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to TC                                    |                | Waveform 2                 | 5.5<br>4.0   | 10.0<br>7.5 | 15.0<br>11.0 | 5.5<br>4.0  | 16.0<br>12.0 | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CET to TC                                   |                | Waveform 3                 | 1.5<br>2.5   | 3.0<br>5.0  | 6.0<br>8.0   | 1.0<br>2.5  | 7.0<br>9.0   | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>U/D to TC                                   |                | Waveform 4                 | 4.0<br>4.0   | 7.5<br>6.5  | 11.0<br>11.0 | 4.0<br>4.0  | 12.0<br>12.0 | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to CC                                    |                | Waveform 2                 | 2.5<br>2.0   | 4.5<br>4.0  | 7.5<br>6.6   | 2.0<br>2.0  | 6.0<br>7.0   | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CEP, CET to CC                              |                | Waveform 2                 | 2.0<br>3.5   | 4.0<br>5.5  | 7.0<br>9.0   | 1.5<br>3.0  | 7.5<br>10.0  | ns<br>ns |
| t <sub>PHL</sub>                     | Propagation delay<br>MR to Q <sub>n</sub>                        |                | Waveform 5                 | 6.0  | 8.0         | 11.0         | 5.5   | 12.0         | ns       |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>U/D to CC                                   |                | Waveform 4                 | 4.5<br>5.0   | 9.0<br>11.0 | 12.0<br>16.0 | 4.0<br>5.0  | 13.5<br>17.0 | ns<br>ns |
| t <sub>PHL</sub>                     | Propagation delay<br>MR to TC, CC                                |                | Waveform 5                 | 8.0  | 11.0        | 15.0         | 7.5   | 16.0         | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>SR to CC                                    |                | Waveform 3                 | 5.5<br>7.5   | 8.0<br>9.5  | 11.0<br>12.0 | 5.0<br>7.0  | 12.0<br>13.0 | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>PE to CC                                    |                | Waveform 3                 | 3.0<br>4.0   | 5.0<br>6.0  | 8.0<br>8.5   | 2.5<br>4.0  | 8.5<br>9.5   | ns<br>ns |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable time to<br>High or Low level OE to Q <sub>n</sub>  |                | Waveform 10<br>Waveform 11 | 2.0<br>4.5   | 4.0<br>6.5  | 7.0<br>9.5   | 2.0<br>4.0  | 7.5<br>10.0  | ns<br>ns |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable time to<br>High or Low level OE to Q <sub>n</sub> |                | Waveform 10<br>Waveform 11 | 1.5<br>1.5   | 3.5<br>3.5  | 6.5<br>6.0   | 1.5<br>1.5  | 7.5<br>6.5   | ns<br>ns |

# 4-bit bidirectional binary synchronous counter (3-State)

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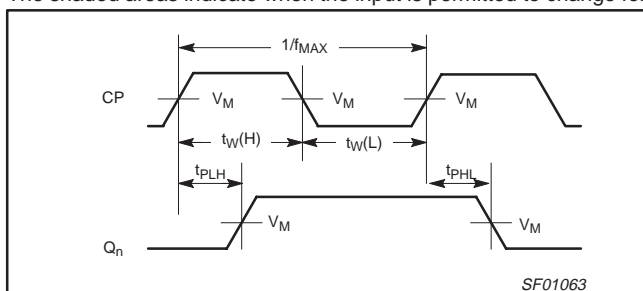
## AC SETUP REQUIREMENTS

| SYMBOL                                   | PARAMETER                                       | TEST CONDITIONS | LIMITS  |     |  |     | UNIT     |
|--|---|-----------------|---|-----|--|-----|----------|
|  |   |                 | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |          |
|  |   |                 | MIN   | TYP | MIN  | MAX |          |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>D <sub>n</sub> to CP | Waveform 6      | 4.0<br>4.0  |     | 4.5<br>4.5   |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>D <sub>n</sub> to CP  | Waveform 6      | 2.0<br>2.0  |     | 2.5<br>2.5   |     | ns<br>ns |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>CEP or CET to CP     | Waveform 7      | 5.0<br>5.0  |     | 6.0<br>6.0   |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>CEP or CET to CP      | Waveform 7      | 0<br>0  |     | 0<br>0   |     | ns<br>ns |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>PE to CP             | Waveform 6      | 8.0<br>8.0  |     | 9.0<br>9.0   |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>PE to CP              | Waveform 6      | 0<br>0  |     | 0<br>0   |     | ns<br>ns |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>U/D to CP            | Waveform 8      | 10.0<br>8.0   |     | 12.5<br>8.0  |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>U/D to CP             | Waveform 8      | 0<br>0  |     | 0<br>0   |     | ns<br>ns |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>SR to CP             | Waveform 9      | 8.0<br>8.0  |     | 9.0<br>9.0   |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>SR to CP              | Waveform 9      | 0<br>0  |     | 0<br>0   |     | ns<br>ns |
| t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | CP Pulse width,<br>High or Low                  | Waveform 1      | 7.0<br>5.0  |     | 8.0<br>6.0   |     | ns<br>ns |
| t <sub>w</sub> (H)                       | MR Pulse width, Low                             | Waveform 5      | 4.5   |     | 5.0  |     | ns       |
| t <sub>REC</sub>                         | Recovery time, MR to CP                         | Waveform 5      | 6.0   |     | 7.0  |     | ns       |

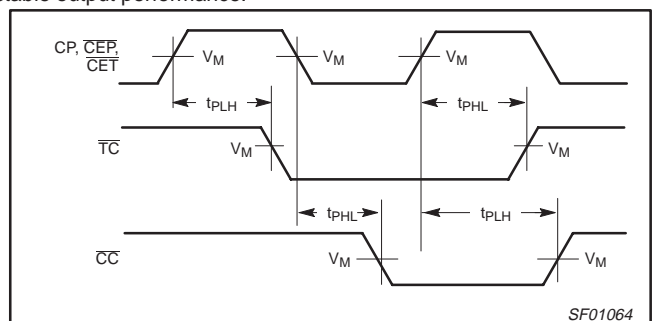
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



**Waveform 2. Propagation Delay, CP, CET, and CEP to CC and CP to TC**



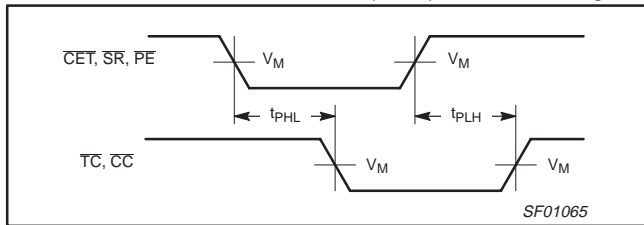
# 4-bit bidirectional binary synchronous counter (3-State)

74F569

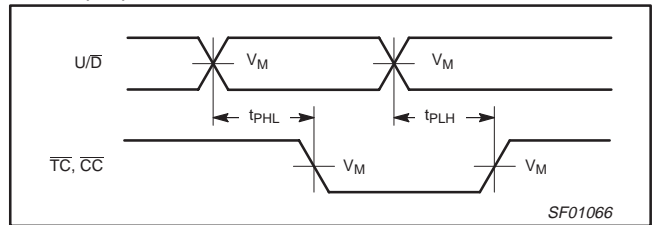
## AC WAVEFORMS (Continued)

For all waveforms,  $V_M = 1.5V$

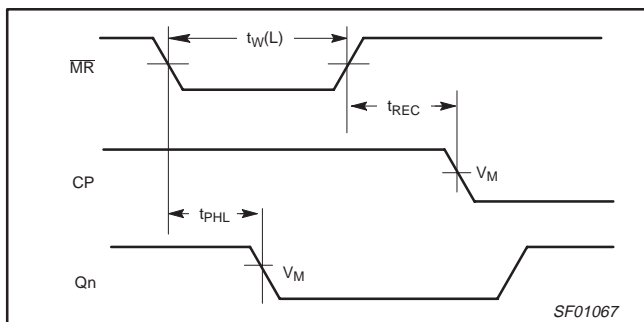
The shaded areas indicate when the input is permitted to change for predictable output performance.



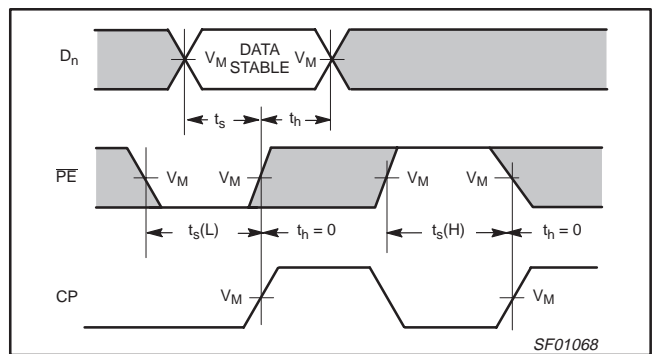
**Waveform 3. Propagation Delays  $\overline{CET}$  to  $\overline{TC}$  and  $\overline{SR}$  or  $\overline{PE}$  to  $\overline{CC}$**



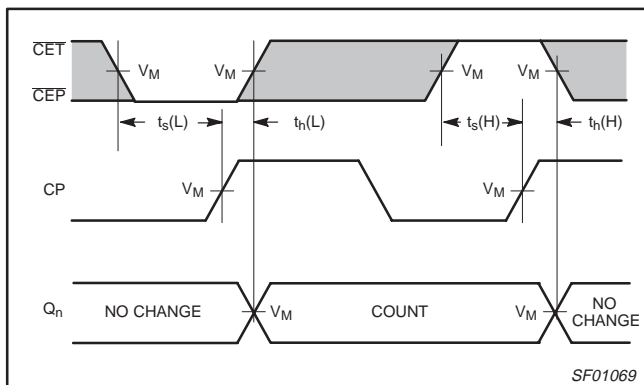
**Waveform 4. Propagation Delays  $U/\overline{D}$  to  $\overline{TC}$  and  $\overline{CC}$**



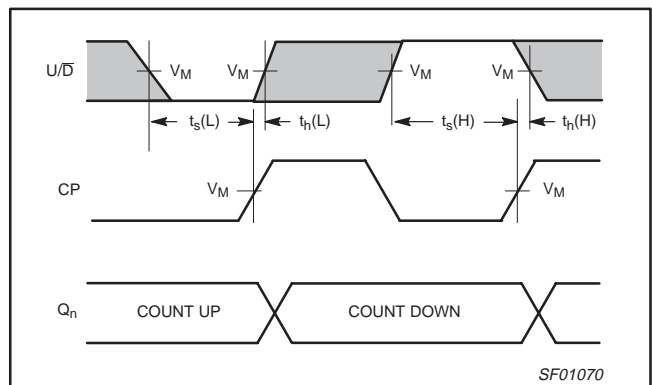
**Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



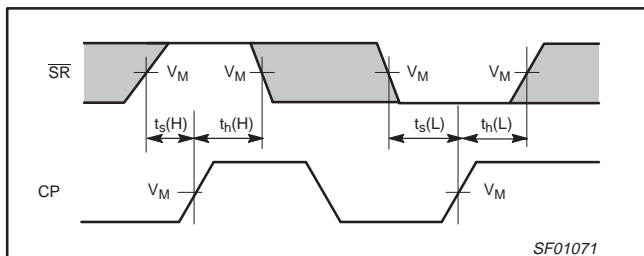
**Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times**



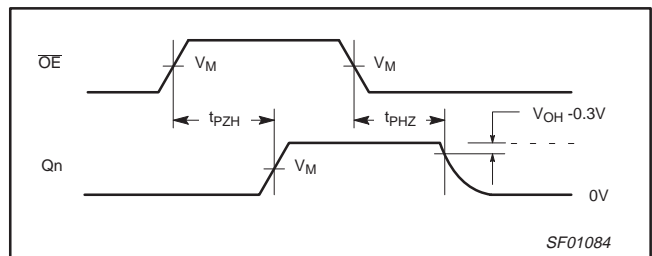
**Waveform 7. Count Enable Data Setup and Hold Times**



**Waveform 8. Up/Down Control Setup and Hold Times**



**Waveform 9. Synchronous Reset Setup and Hold Times**



**Waveform 10. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

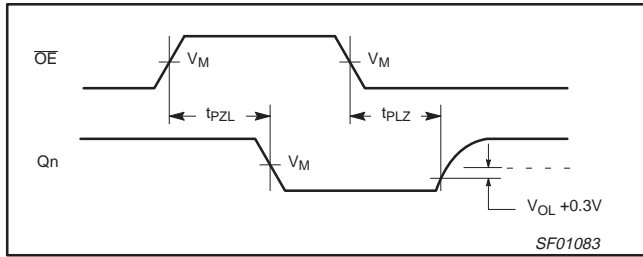
# 4-bit bidirectional binary synchronous counter (3-State)

74F569

## AC WAVEFORMS (Continued)

For all waveforms,  $V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 11. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**

**SWITCH POSITION**

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open   |

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

| family | INPUT PULSE REQUIREMENTS |       |           |       |           |           |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
|        | amplitude                | $V_M$ | rep. rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74F    | 3.0V                     | 1.5V  | 1MHz      | 500ns | 2.5ns     | 2.5ns     |

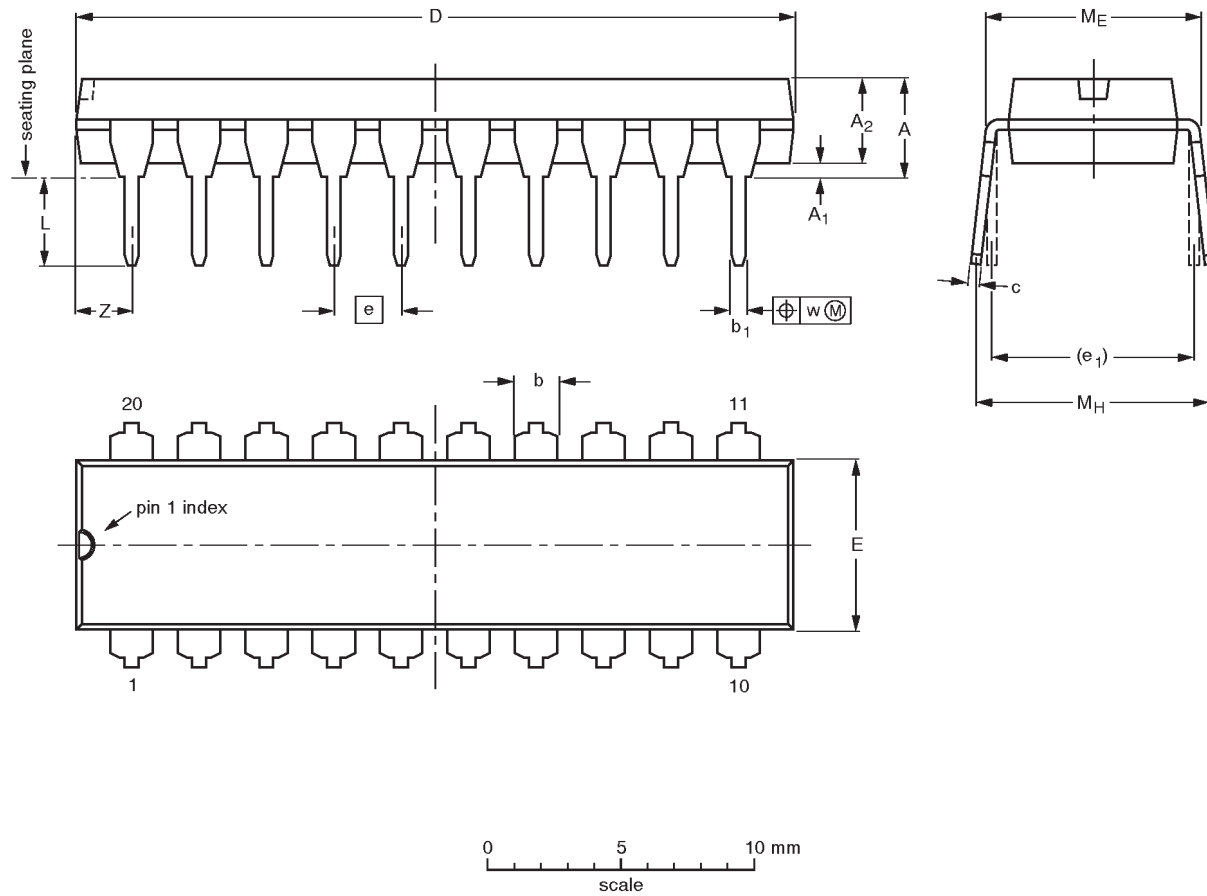
SF00777

# 4-bit bidirectional binary synchronous counter (3-State)

74F569

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.30   | 0.53<br>0.38   | 0.36<br>0.23   | 26.92<br>26.54   | 6.40<br>6.22     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.0                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045   | 0.25<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.078                 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

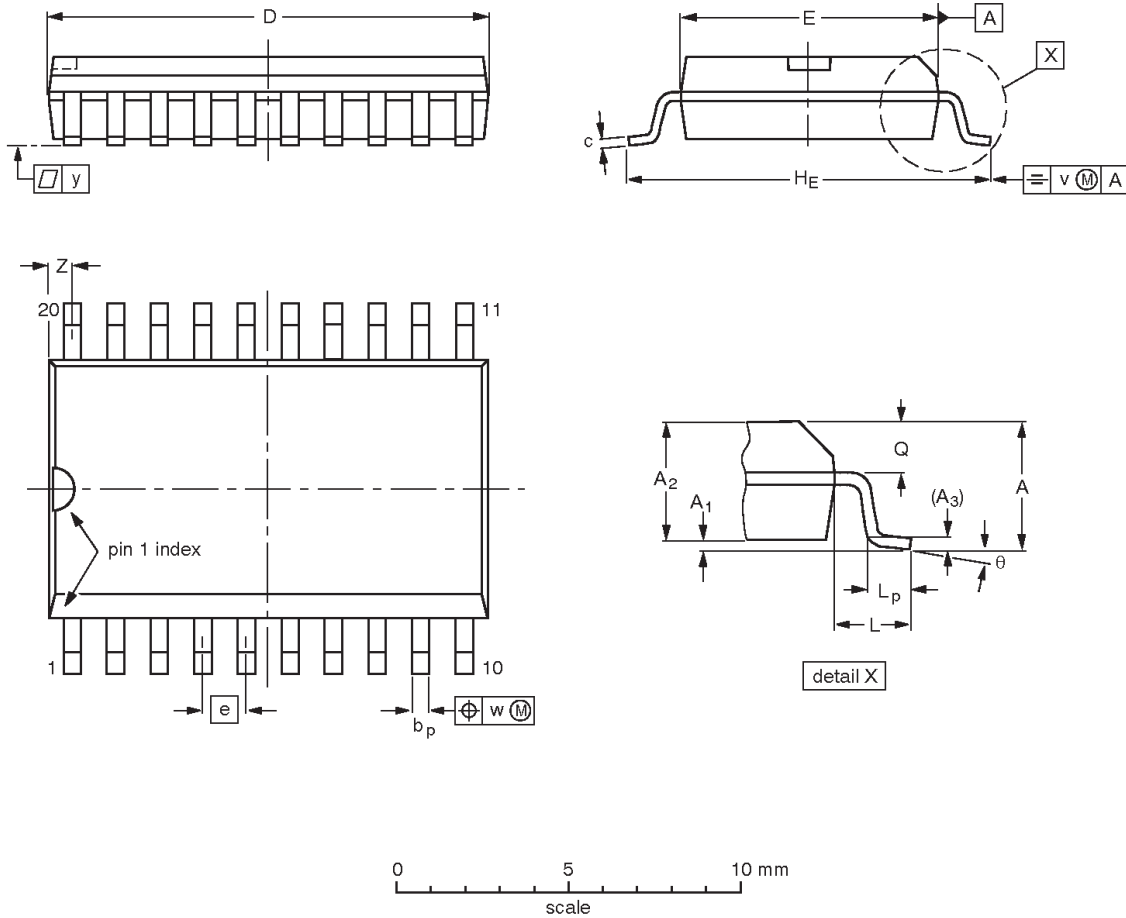
| OUTLINE VERSION | REFERENCES |       |       |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ  |  |                     |                      |
| SOT146-1        |            |       | SC603 |  |                     | 92-11-17<br>95-05-24 |

4-bit bidirectional binary synchronous counter (3-State)

74F569

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | HE             | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 13.0<br>12.6     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49     | 0.30<br>0.29     | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT163-1        | 075E04     | MS-013AC |      |  |                     | 95-01-24<br>97-05-22 |

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4-bit bidirectional binary synchronous counter (3-State)

74F569

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**NOTES**

## 4-bit bidirectional binary synchronous counter (3-State)

74F569

## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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