MACH435-12/15/20, Q-20/25

Lattice Semiconductor

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **84 Pins in PLCC**
- **128 Macrocells**
- **12 ns t_{PD}**
- **83.3 MHz f_{CNT}**
- **70 Inputs with pull-up resistors**
- **64 Outputs**
- **192 Flip-flops**
  - — 128 Macrocell flip-flops
  - — 64 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **Pin compatible with MACH130, MACH131, MACH230, and MACH231**

GENERAL DESCRIPTION

The MACH435 is a member of our high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH435 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH435 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH435 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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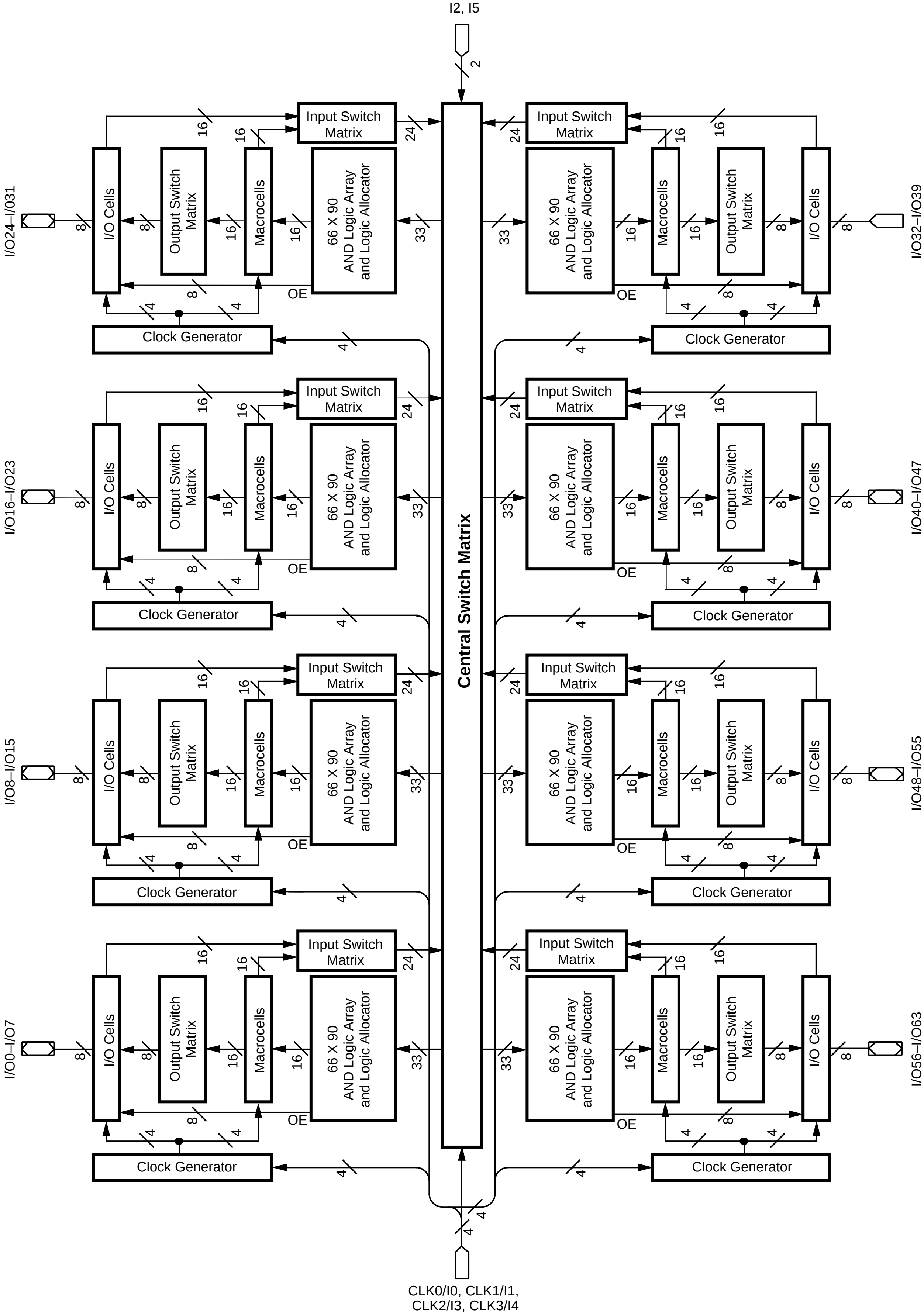
BLOCK DIAGRAM



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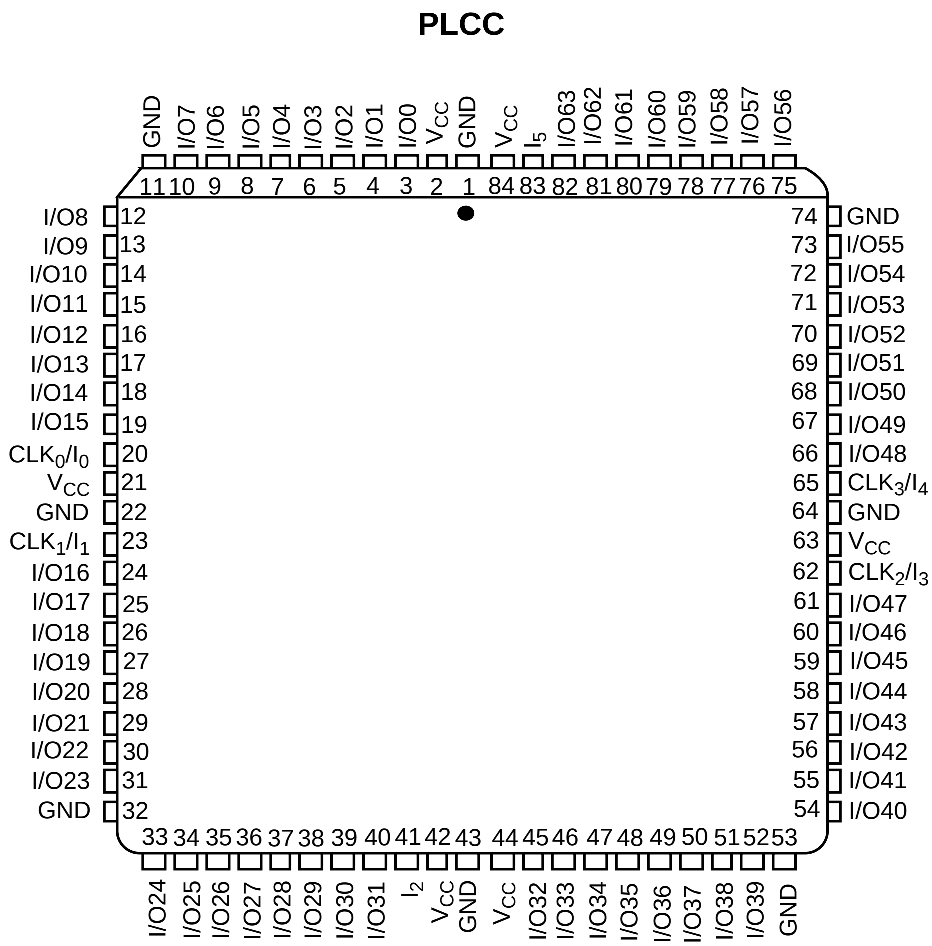
CONNECTION DIAGRAM
Top View



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Note:

Pin-compatible with MACH130, MACH131, MACH230, and MACH231

PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I	=	Input
I/O	=	Input/Output
V_{CC}	=	Supply Voltage

ORDERING INFORMATION
Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 435 -12 J C __

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
435 = 2nd Generation, 128 Macrocells, 84 Pins
435Q = 2nd Generation, 128 Macrocells, 84 Pins, Quarter Power

SPEED
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}
-25 = 25 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +70°C)

PACKAGE TYPE
J = 84-Pin Plastic Leaded Chip Carrier (PL 084)

Valid Combinations	
MACH435-12	JC
MACH435-15	
MACH435-20	
MACH435Q-20	
MACH435Q-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH435 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH435 (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH435 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH435 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH435 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH435 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH435 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

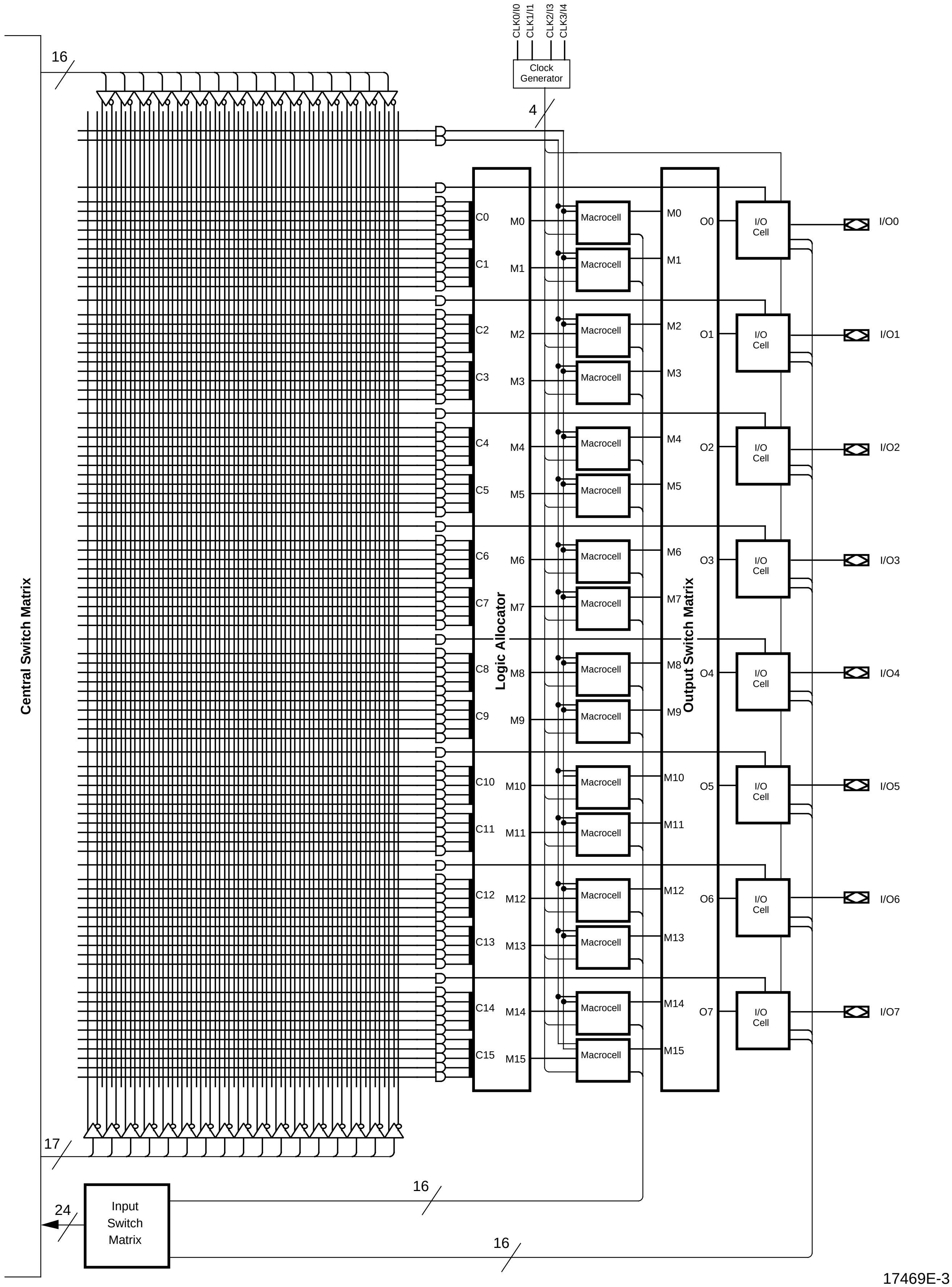


Figure 1. MACH435 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . –0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage . . . . –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current
(T_A = 0°C to +70°C) . . . . 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	12	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	5		ns
			T-type	6		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			5		ns
t_{COA}	Product Term Clock to Output			4	14	ns
t_{WLA}	Product Term, Clock Width		LOW	8		ns
t_{WHA}			HIGH	8		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	52.6		MHz
			T-type	50		MHz
		Internal Feedback (f_{CNTA})	D-type	58.8		MHz
			T-type	55.6		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	7		ns
			T-type	8		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	8	ns
t_{WLS}	Global Clock Width		LOW	6		ns
t_{WHS}			HIGH	6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	66.7		MHz
			T-type	62.5		MHz
		Internal Feedback (f_{CNTA})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (Note 3)		83.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			5		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			5		ns
t_{GOA}	Product Term Gate to Output				16	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			8		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				10	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			3		ns
t_{ICO}	Input Register Clock to Combinatorial Output				18	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	9		ns
		T-type	10		ns
t_{WICL}	Input Register Clock Width	LOW	6		ns
t_{WICH}		HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency		83.3		MHz
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			16	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			18	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		4		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		9		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		ns
t_{WIGL}	Input Latch Gate Width LOW		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16	ns
t_{APW}	Asynchronous Preset Width (Note 1)		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	12	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . –0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage . . . . –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current (T_A = 0°C to +70°C) . . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the “Typical Dynamic I_{CC} Characteristics” Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				4		5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		10		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		12		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage . . . . –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current (T_A = 0°C to +70°C) . . . . 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		115		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	10		ns
			T-type	11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			16		ns
t_{COA}	Product Term Clock to Output			5	22	ns
t_{WLA}	Product Term, Clock Width		LOW	12		ns
t_{WHA}			HIGH	12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	33.3		MHz
			T-type	37.2		MHz
		Internal Feedback (f_{CNTA})	D-type	35.7		MHz
			T-type	34.5		MHz
		No Feedback (Note 3)		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	13		ns
			T-type	14		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	12	ns
t_{WLS}	Global Clock Width		LOW	8		ns
t_{WHS}			HIGH	8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	40.0		MHz
			T-type	38.5		MHz
		Internal Feedback (f_{CNTA})	D-type	47.6		MHz
			T-type	43.5		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			8		ns
t_{GOA}	Product Term Gate to Output				22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				22	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			4		ns
t_{ICO}	Input Register Clock to Combinatorial Output				22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		ns
		T-type	17		ns
t_{WICL}	Input Register Clock Width	LOW	8		ns
t_{WICH}		HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			24	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		10		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		15		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		15		ns
t_{WIGL}	Input Latch Gate Width LOW or HIGH		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			25	ns
t_{APW}	Asynchronous Preset Width (Note 1)		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . –0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage . . . . –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current
(T_A = 0°C to +70°C) . . . . 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f=25 MHz, T_A = 25°C, (Note 5)		115		mA

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, erased, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of the this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-25 Min	-25 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	25	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	18		ns
				T-type	19		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				18		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	28	ns
t_{WLA}	Product Term, Clock Width			LOW	19		ns
t_{WHA}				HIGH	19		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	21.7		MHz
				T-type	21.3		MHz
		Internal Feedback (f_{CNTA})		D-type	24.4		MHz
				T-type	23.8		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		26.3		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	20		ns
				T-type	21		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		ns
t_{COS}	Global Clock to Output (Note 2)				2	12	ns
t_{WLS}	Global Clock Width			LOW	8		ns
t_{WHS}				HIGH	8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	31.3		MHz
				T-type	30.3		MHz
		Internal Feedback (f_{CNTS})		D-type	37		MHz
				T-type	35.7		MHz
		No Feedback (Note 4)	$1/(t_{SS} + t_{HS})$		50		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				18		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				18		ns
t_{GOA}	Product Term Gate to Output (Note 2)					29	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				19		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				20		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		ns
t_{GOS}	Gate to Output (Note 2)					21	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					27	ns
t_{SIR}	Input Register Setup Time				5		ns
t_{HIR}	Input Register Hold Time				5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					30	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

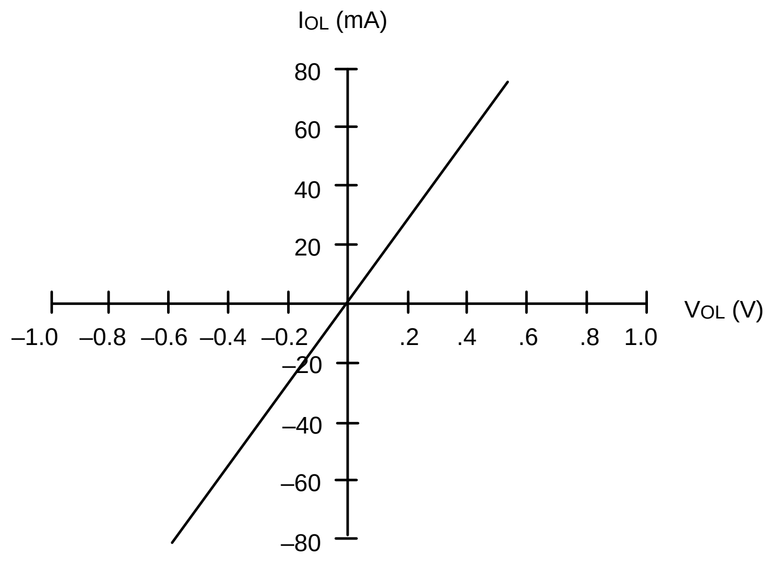
Parameter Symbol	Parameter Description		-25 Min	-25 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	25		ns
		T-type	26		ns
t_{WICL}	Input Register Clock Width	LOW	8		ns
t_{WICH}		HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	62.5		MHz
t_{SIL}	Input Latch Setup Time		5		ns
t_{HIL}	Input Latch Hold Time		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			32	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		20		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		24		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		22		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		26		ns
t_{WIGL}	Input Latch Gate Width LOW or HIGH		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			30	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		25		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		25		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			30	ns
t_{APW}	Asynchronous Preset Width (Note 3)		25		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		25		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	25	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	25	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

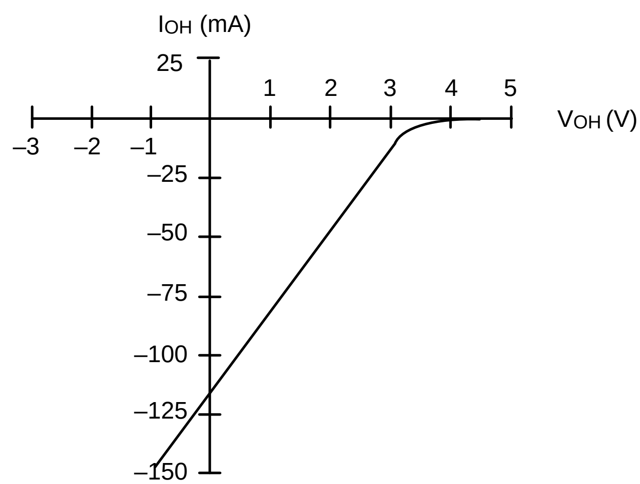
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



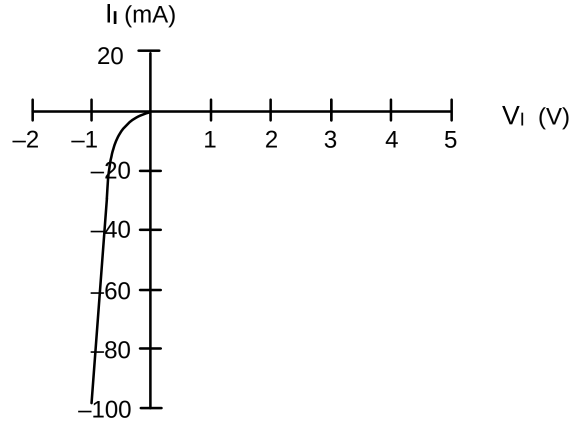
17469E-4

Output, LOW



17469E-5

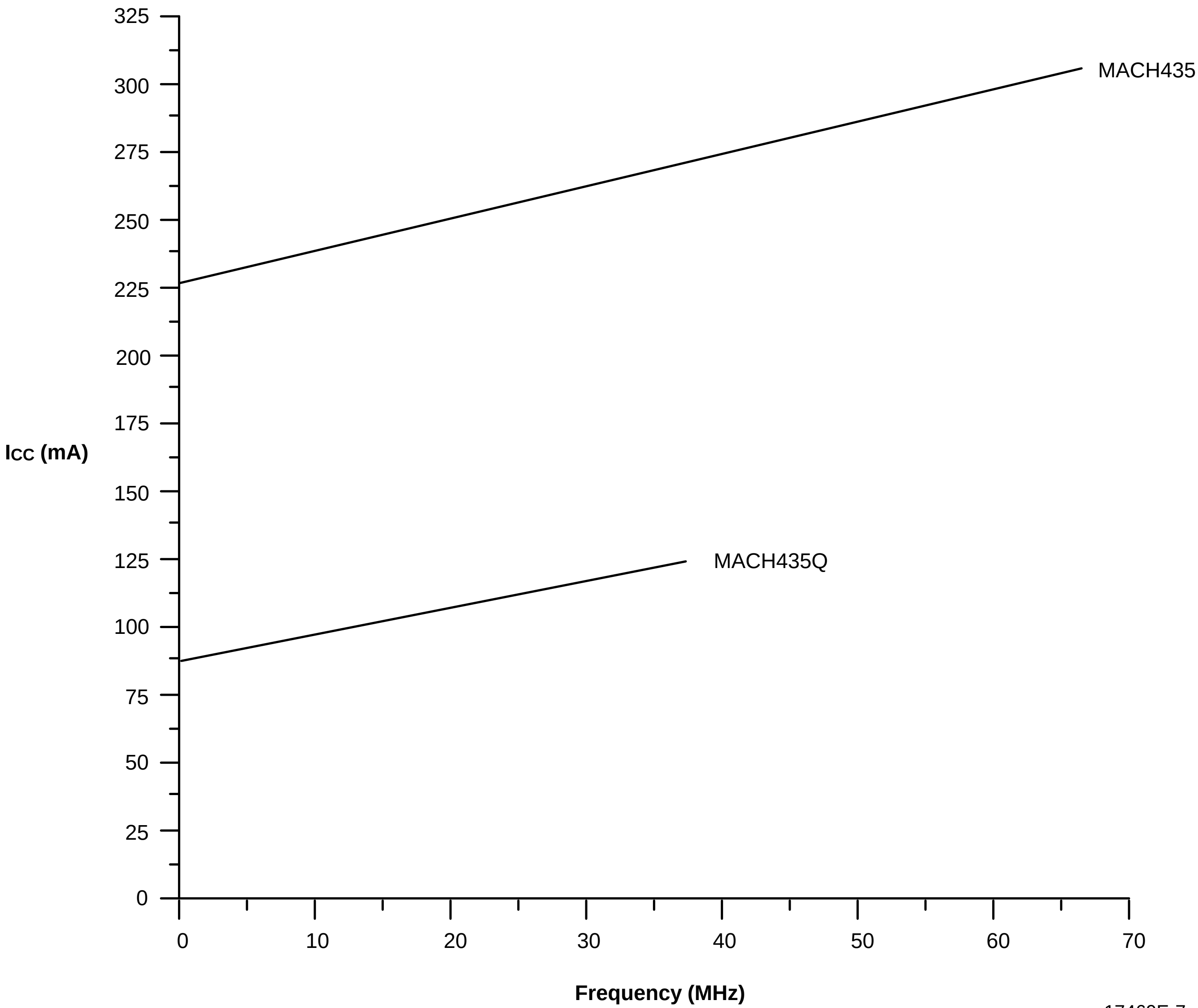
Output, HIGH



17469E-6

Input

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



17469E-7

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

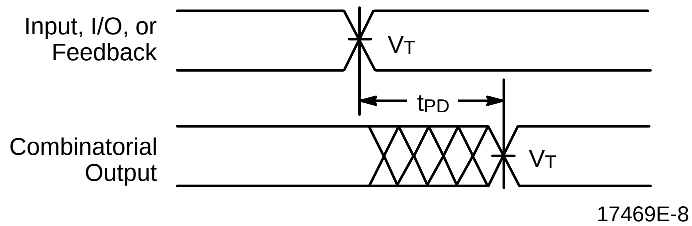
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

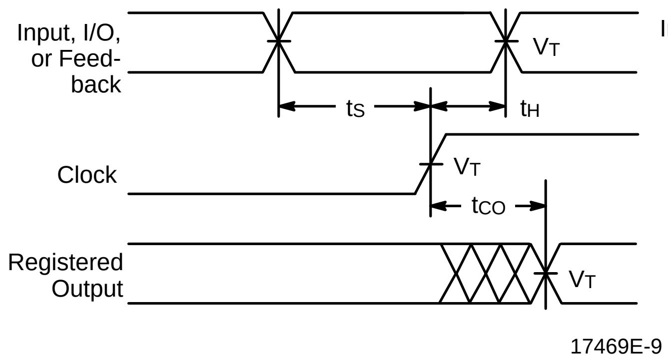
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

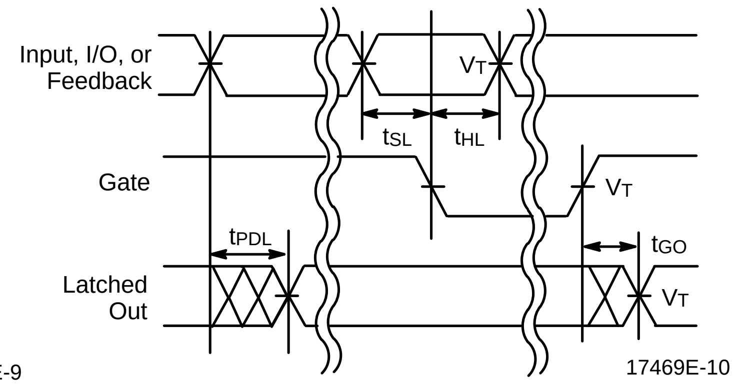
SWITCHING WAVEFORMS



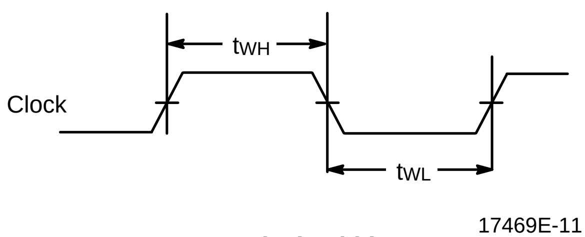
Combinatorial Output



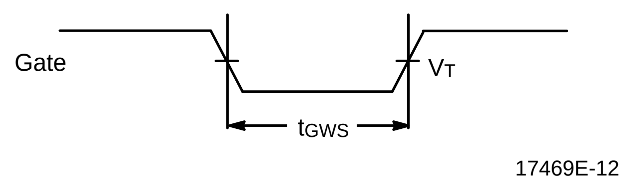
Registered Output



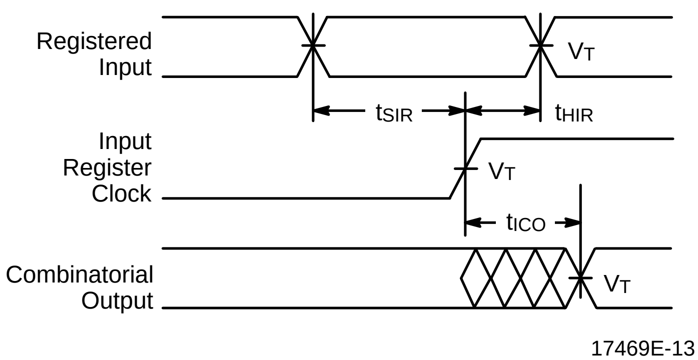
Latched Output (MACH 2, 3, and 4)



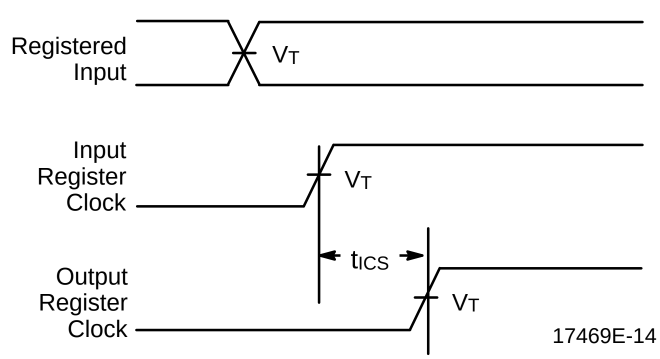
Clock Width



Gate Width (MACH 2, 3, and 4)



Registered Input (MACH 2 and 4)

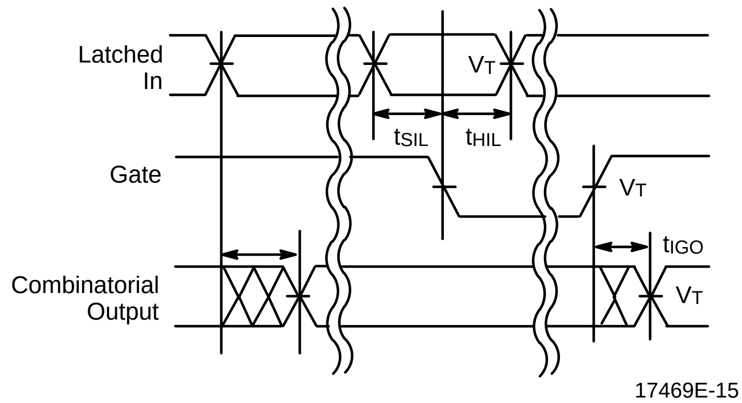


Input Register to Output Register Setup (MACH 2 and 4)

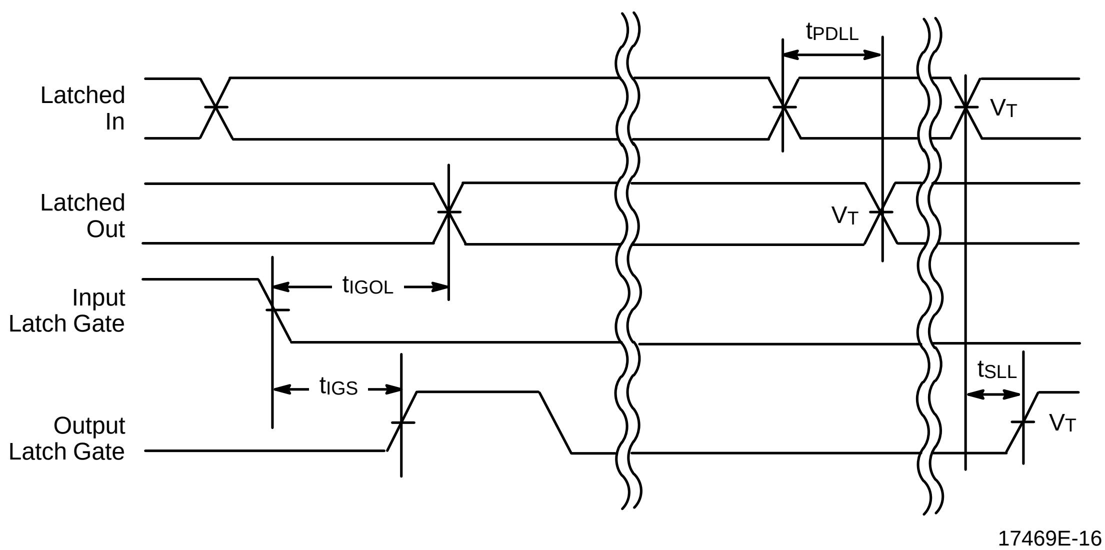
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



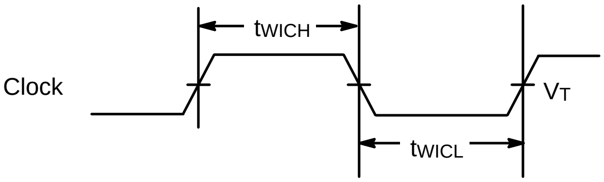
Latched Input (MACH 2 and 4)



Latched Input and Output (MACH 2, 3, and 4)

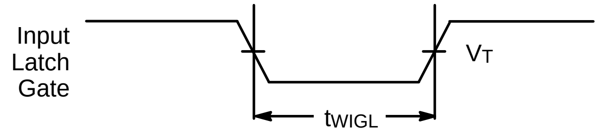
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*



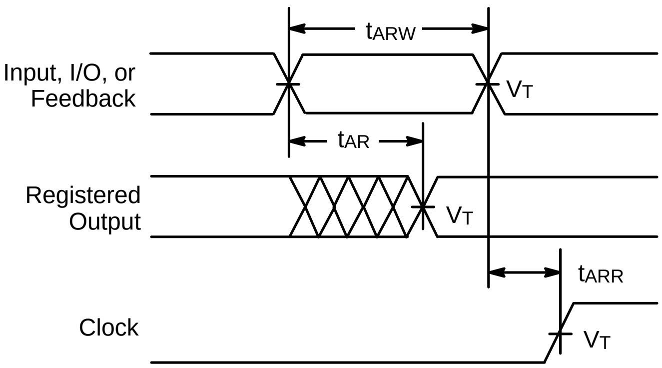
17469E-17

Input Register Clock Width (MACH 2 and 4)



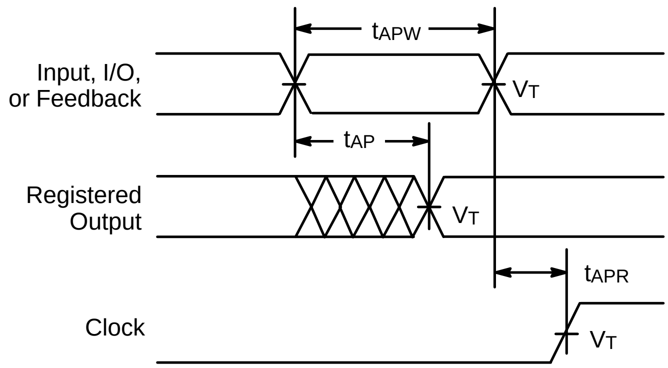
17469E-18

Input Latch Gate Width (MACH 2 and 4)



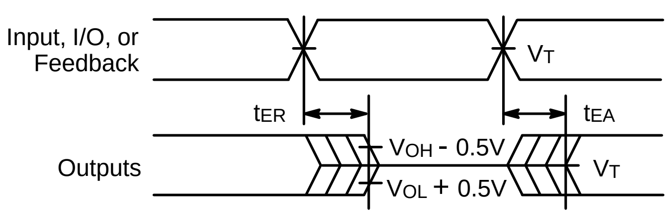
17469E-19

Asynchronous Reset



17469E-20

Asynchronous Preset



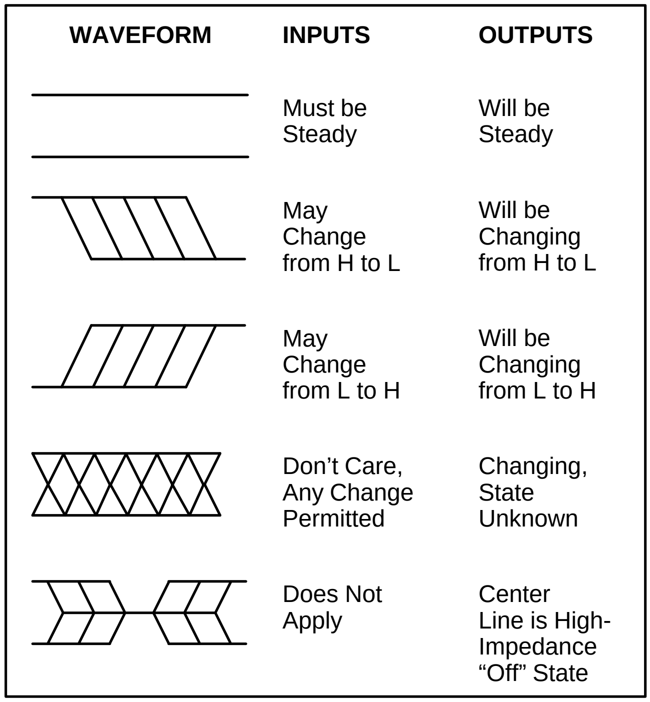
17469E-21

Output Disable/Enable

Notes:

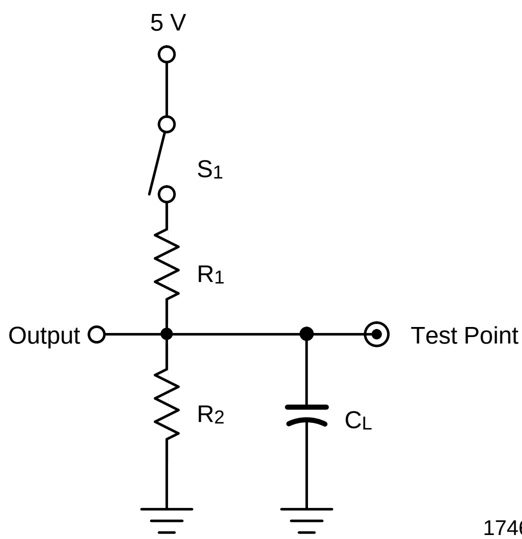
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



17469E-22

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

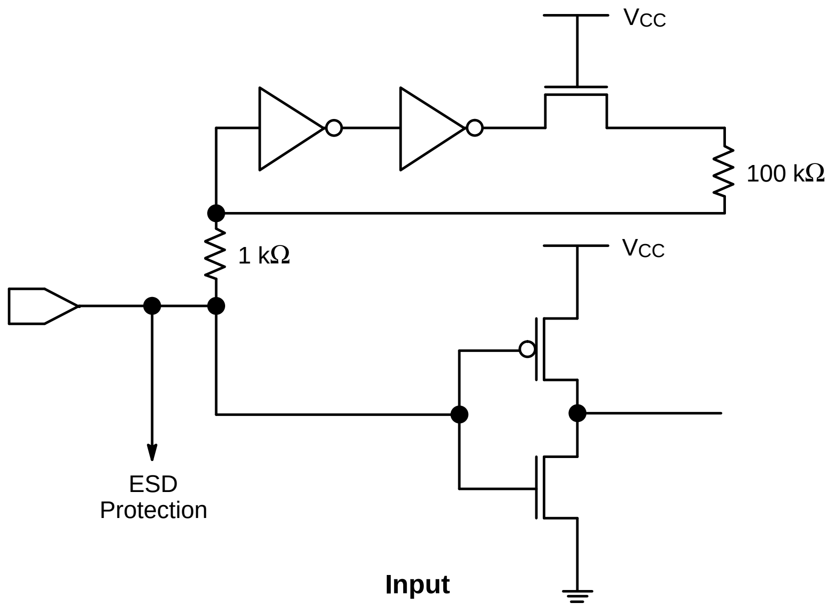
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

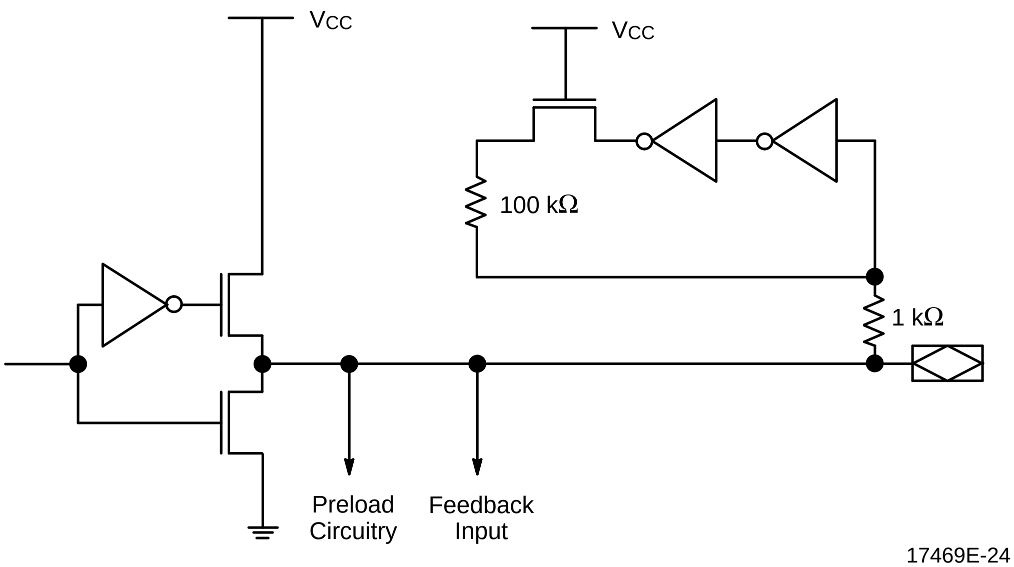
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



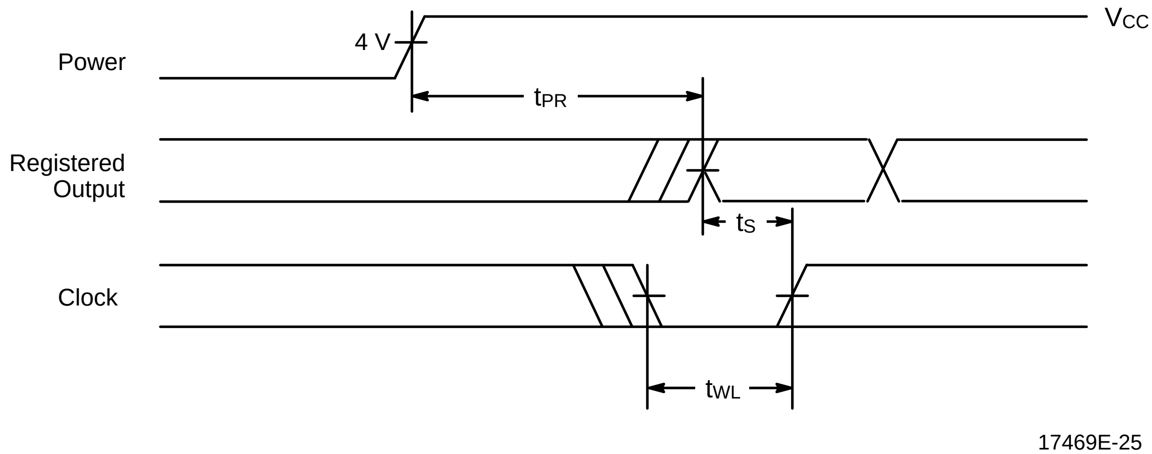
I/O

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

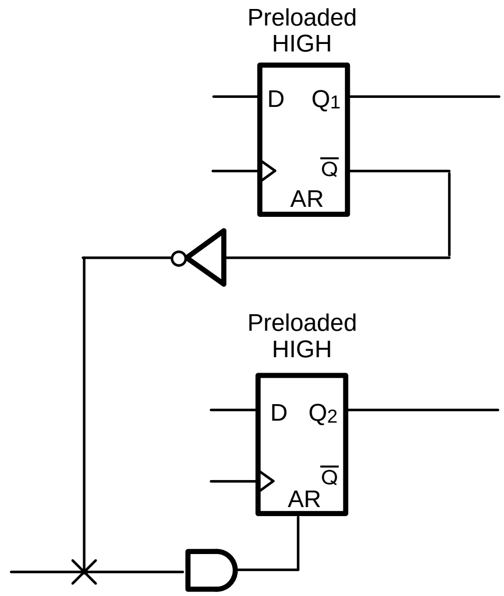
While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 2. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 3. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.



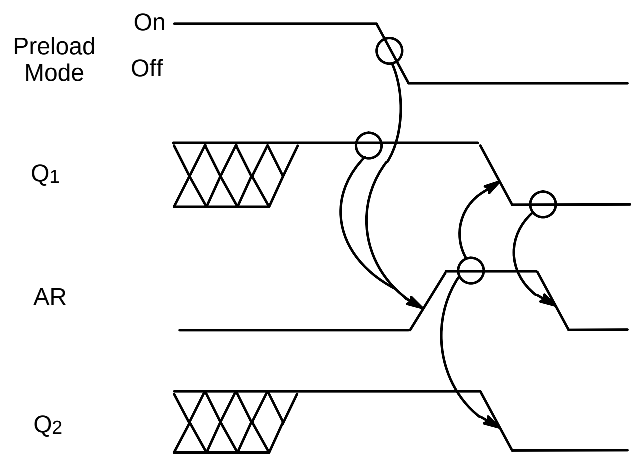


Figure 2. Preload/Reset Conflict

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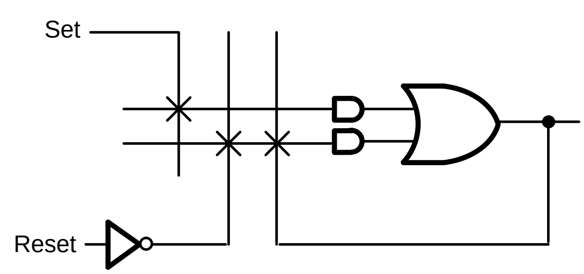

Figure 3. Combinatorial Latch

17469E-27