To:_____

SPECIFICATION

Rev. 4.0

Application:

VACUUM FLUORESCENT DISPLAY MODULE

Model No.: 16T202DA1J

Rev. No.	Issued Date	Revision Descriptions	Remark
Tentative	Oct. 16, 1998	First Edition	All Pages
Rev. 1.0	Jan. 07, 2000	* Change of AC Characteristics (i80 bus interface) - t_{CYC} (/WR) =166ns → 200ns - t_{CYC} (/RD) =166ns → 200ns - t_{WH} (/RD) =70ns → 100ns	Page - 5
Rev. 2.0	Oct. 11, 2002	* Change of Operating and Storage Temperature - Topr:(-20 ~ +75) → (-40 ~ +85) - Tstg:(-40 ~ +85) → (-50 ~ +85) * Change of Outer Dimensions	Page - 4 Page - 8
Rev. 3.0	Oct. 16, 2002	* Change of Power On Reset Timing - t_{OFF}:100ms(Min.) → 1ms(Min.) - tr:1ms(Max.) → 1us(Min.) * Change of System Block Diagram * Change of Outer Dimensions	Page - 5 Page - 7 Page - 8
Rev. 4.0	Apr. 15, 2005	* Addition of Index Page etc * Change of Production Plant (SDI → SSVD) in Section-1 (SCOPE) * Addition of Initialize and Data Set Example * Change of Document Formation	Page - 2 Page - 3 Page - 17 All Pages

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Checked by	
Approved by	

Customer's Approval

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1. SCOPE

* This specification applies to VFD module (Model No.:16T202DA1J) manufactured by Samsung SDI or SSVD.

2. FEATURES

* LCD Compatible: Drop-in-replacement (Same Interface and Mechanical Dimension as LCD Module).

* High Quality, Attractive and Readable Display: 5*7 Dot Matrix Type Vacuum Fluorescent Display.

* Compact and Lightweight: Flat Panel (VFD) and Surface Mount Technology.

* +5V single power supply.

* Brightness Level: Adjustable into 4 Levels (25%, 50%, 75% and 100%) by Software Command.

* Support CG-RAM Fonts and CG-ROM: 8 User-definable Characters (Volatile) and 240 Masked CG-ROM Fonts.

3. PRECAUTIONS

* Avoid applying excessive shock or vibration beyond the specification for the VFD module.

* Since VFDs are made of glass material, careful handling is required. i.e. Direct impact with hard material to the glass surface (especially exhaust tip) may crack the glass.

* When mounting the VFD module to your system, leave a slight gap between the VFD glass and your front panel. The module should be mounted without stress to avoid flexing of the PCB.

* Avoid plugging or unplugging the interface connection with the power on, otherwise it may cause the severe damage to input circuitry.

* Slow starting power supply may cause non-operation because one chip MCU won't be reset.

* Exceeding any of maximum ratings may cause the permanent damage.

* Since the VFD modules contain high voltage source, careful handling is required during powered on.

* When the power is turned off, the capacitor does not discharge immediately. The high voltage applied to the VFD must not contact to the ICs. And the short-circuit of mounted components on PCB within 30 seconds after power-off may cause damage to those.

* The power supply must be capable of providing at least 5 times the rated current, because the surge current can be more than 5 times the specified current consumption when the power is turned on.

* Avoid using the module where excessive noise interference is expected. Noise may affects the interface signal and causes improper operation. And it is important to keep the length of the interface cable less than 50cm.

* Since all VFD modules contain C-MOS ICs, anti-static handling procedures are always required.

4. PRODUCT SPECIFICATIONS

4.1 Type

Type (Module Name)	16T202DA1J
Character Format	5 * 7 Dot Matrix with Cursor
Number of Digits	32 (16 Digits * 2 Lines)

4.2 Outer Dimensions, Weight (See Fig.-8 on Page 8 for details)

Parameter	Symbol	Specification	Unit
Outer Dimensions	W * H * t	85.0 * 36.0 * 19.5	mm
Panel Size	W * H	76.0 * 23.0	mm
Display Size	W * H	51.76 * 11.09	mm
Character Size	W * H	2.26 * 4.343	mm
Character Pitch	W * H	3.30 * 6.15	mm
Dot Size	W * H	0.372 * 0.534	mm
Display Color	-	x= 0.250, y = 0.439 (Green)	-
Weight	-	Approx 35	g

4.3 Environment Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	Topr	-40	+85	°C
Storage Temperature	Tstg	-50	+85	°C
Humidity (Operating)	Hopr	0	85	%
Humidity (Non-operating)	Hstg	0	95	%
Vibration (10 ~ 55 Hz)	-	-	4	G
Shock	-	-	40	G

4.4 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	-0.5	6.0	V_{DC}
Input Signal Voltage	V_{IS}	-0.5	V_{CC}+0.5	V_{DC}

4.5 Recommend Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V_{DC}
Input Signal Voltage	V_{IS}	0	-	V_{CC}	V_{DC}

4.6 DC Characteristics (Ta = +25 °C, V_{CC} = 5.0V_{DC})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Current *1)	I_{CC}	-	130	200	mA
"H" Level Logic Input Voltage	V_{IH}	0.7V_{CC}	-	-	V_{DC}
"L" Level Logic Input Voltage	V_{IL}	-	-	0.3V_{CC}	V_{DC}
"H" level Input Current (V_{IN} = V_{CC}) *2)	I_{IH}	20	-	500	uA
"L" level Input Current (V_{IN} = 0V_{DC})	I_{IL}	-	-	-1.0	mA
Luminance	L	102 (350)	204 (700)	-	ft-L (cd/m^2)

**1) The in-rush current can be approx. 5 times the specified supply current at power on.*
**2) A 10k Ohm resistance is pulled-up on each input signals for TTL compatibility.*

4.7 Timing Chart and AC Characteristics

4.7.1 Power-on Reset Timing

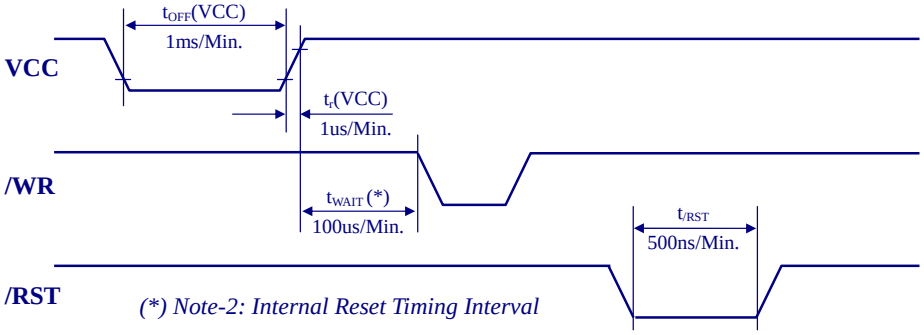


Fig.-1. Power-on Reset and /RST Signal Timing

4.7.2 M68 type CPU Bus Interface Timing

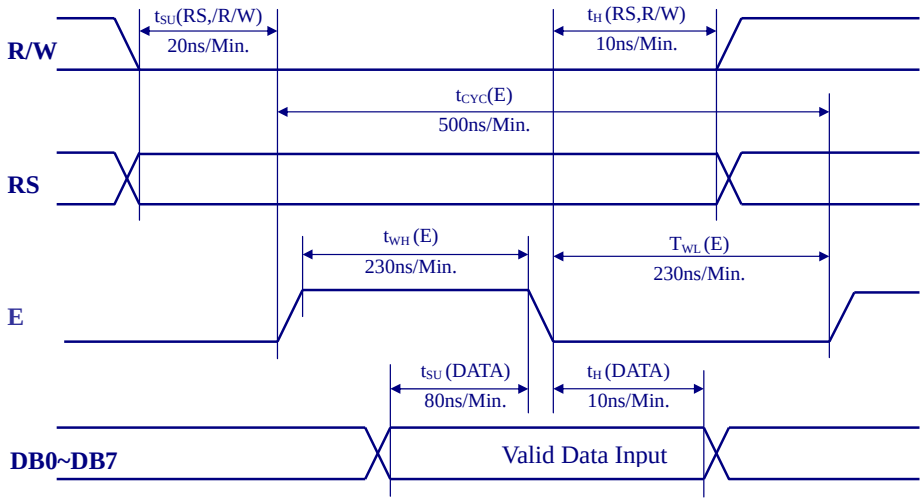


Fig.-2. Data Write-in Timing for M68 Interface Mode

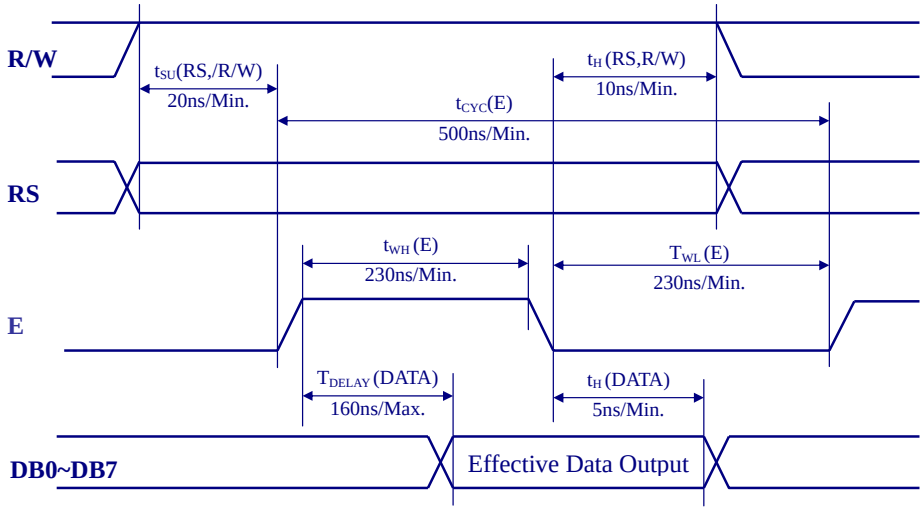


Fig.-3. Data Read-out Timing for M68 Interface Mode

4.7.3 i80 type CPU Bus Interface Timing

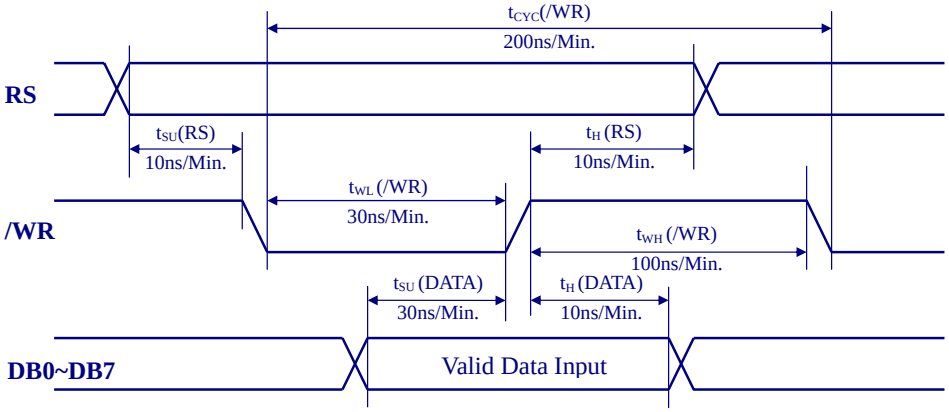


Fig.-4. Data Write-in Timing for i80 Interface Mode

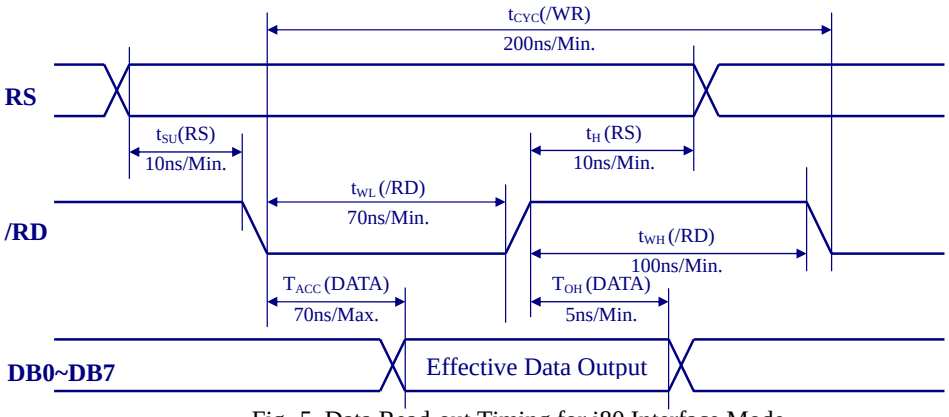


Fig.-5. Data Read-out Timing for i80 Interface Mode

4.8 Connector Pin Assignment

14 through holes are prepared for power supply and signal interface. A connector may be able to solder to the holes. Location and dimensions are shown at Fig.-7 on Page-7.

Pin No.	Symbol	I/O	Descriptions
1	GND	-	Ground Terminal
2	VCC	-	Supply Power Terminal
3	/RST (*)	Input	Reset Signal (Active Low) If a user would like to use external reset by using this terminal then he must short-circuit the jumper switch, JP1. i.e. /RST is signal can be used when JP1 is closed.
4	RS	Input	Register Select ("0"; Instruction Register, "1"; Data Register)
5	R/W (/WR)	Input	When M68 interface mode is selected (JP0; Open), this pin is to be data IN/OUT select pin. ("0"; Data Write-in, "1"; Data Read-out) When i80 interface mode is selected (JP0; Short), this pin is to be WRITE enable pin. (Writes data at rising edge of this signal.)
6	E (/RD)	Input	When M68 mode is selected (JP0; Open), this pin is to be Read/Write enable. (Writes data at the falling edge and Reads data at the rising edge.) When i80 mode is selected (JP0: Short), this signal is to be READ enable pin. (When this pin is low level, logic "0", the effective data is output to data bus.)
7 8 9 10 11 12 13 14	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	I/O	These pins are used for data IN/OUT pin. When select 4 bits transfer mode, just DB4 (pin #11) to DB7 (pin #14) are used. Data are stored sequentially, with data transmitted first stored in upper bits (MSB). The DB7 (pin#14) signal can be used for BUSY flag out when RS="0" and R/W="1" for M68 read-out mode.

4.9 System Block Diagram

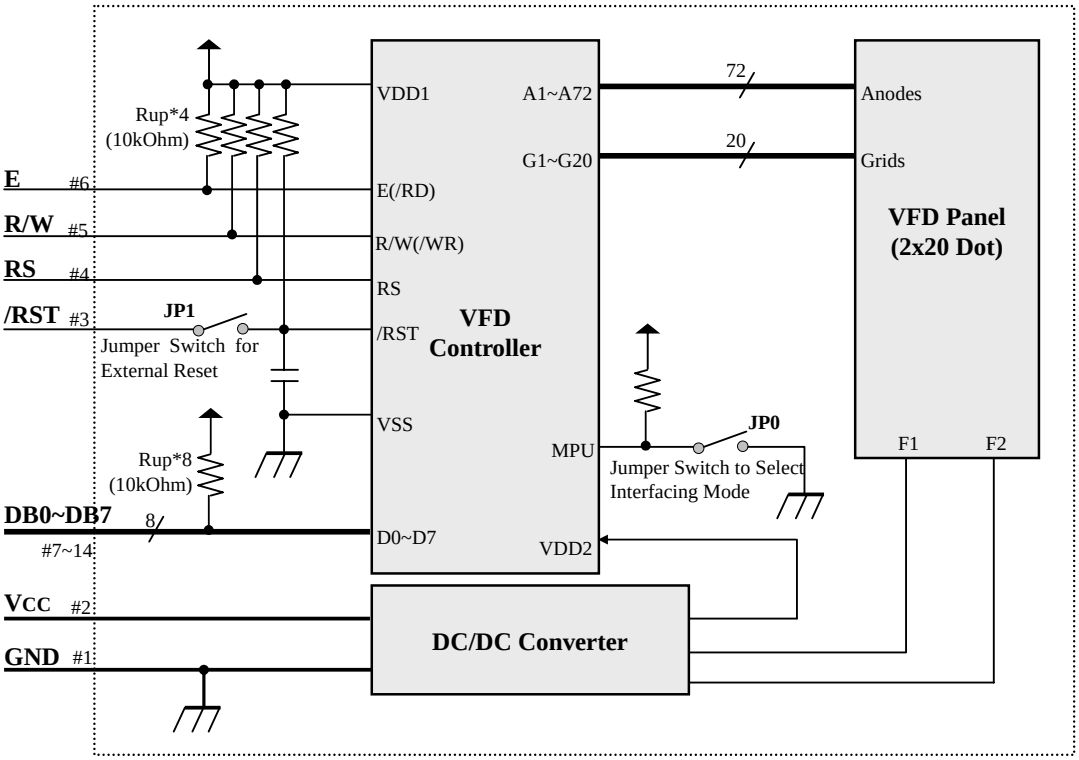


Fig.-6 System Block Diagram

4.10 Connector through Hole Location

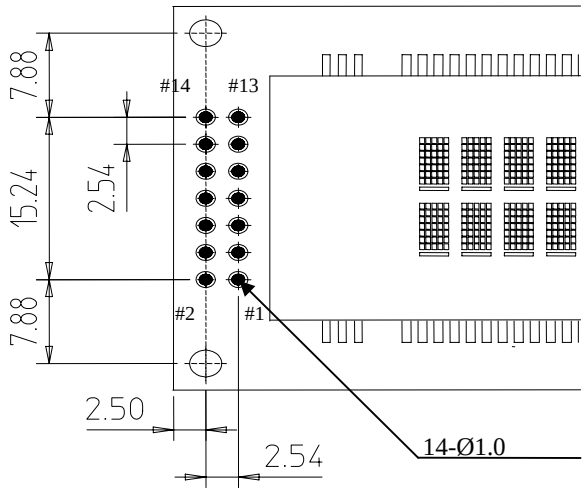
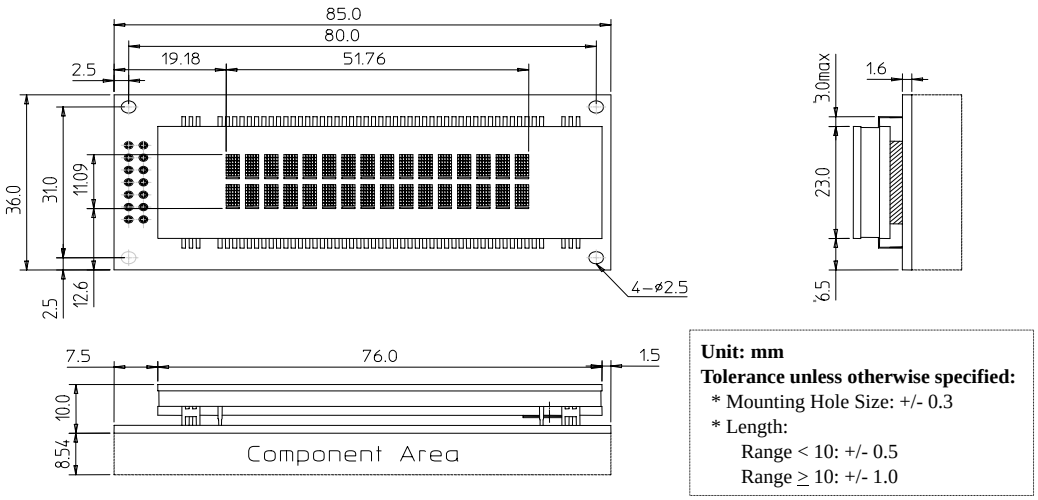


Fig.-7 Connector through Hole Location

4.11 Outer Dimensions



Unit: mm
Tolerance unless otherwise specified:
* Mounting Hole Size: +/- 0.3
* Length:
  Range < 10: +/- 0.5
  Range ≥ 10: +/- 1.0

Fig.-8 Outer Dimensions

4.12 Pattern Details

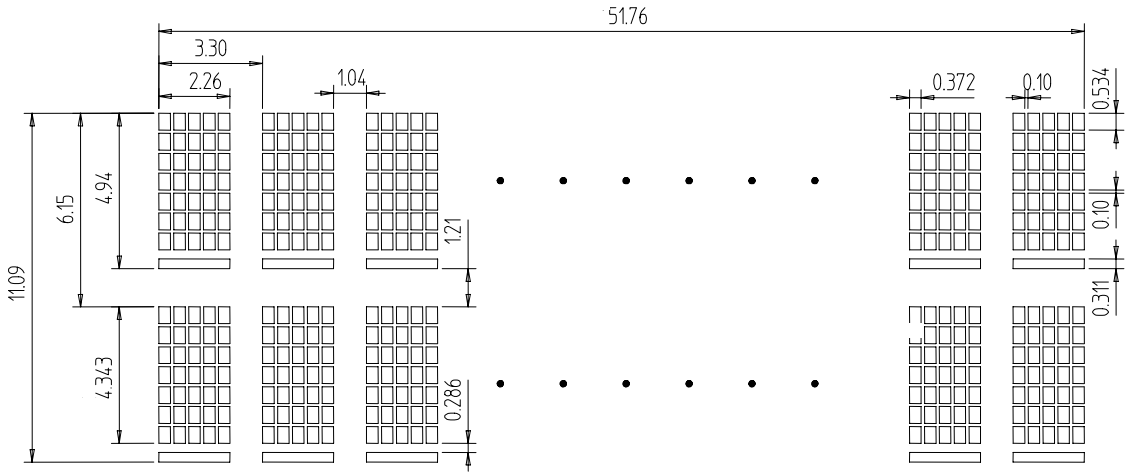


Fig.-9 Pattern Details

5. FUNCTION DESCRIPTIONS

5.1 Registers in VFD Controller

The VFD controller has two 8-bit registers, an instruction register (IR) and a data register (DR). IR stores instruction codes, such as display clear and cursor shift, and address information for DD-RAM and CG-RAM. The IR can only be written from the host MPU. DR temporarily stores data to be written into DD-RAM or CG-RAM and temporarily stores data to be read from DD-RAM or CG-RAM. Data written into the DR from the MPU is automatically written into DD-RAM or CG-RAM by an internal operation. The DR is also used for data storage when reading data from DD-RAM or CG-RAM. When address information is written into the IR, data is read and then stored into the DR from DD-RAM or CG-RAM by internal operation. Data transfer between MPU is then completed when the MPU reads the DR. After the read, data in DD-RAM or CG-RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected.

* **Truth Table for Register Selection**

RS	M68	i80		Operation
	R/W	/RD	/WR	
0	0	1	0	IR write as an internal operation (display clear, etc.)
0	1	0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	1	0	DR write as an internal operation (DR to DD-RAM or CG-RAM)
1	1	0	1	DR read as an internal operation (DD-RAM or CG-RAM to DR)

5.1.1 Busy Flag (BF)

When the busy flag is 1, the controller is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

5.1.2 Address Counter (ACC)

The address counter (ACC) assigns addresses for both DD-RAM and CG-RAM. When an instruction of address is written into the IR, the address information is sent from the IR to the ACC. Selection of either DD-RAM or CG-RAM is also determined concurrently by the instruction. After writing into (reading from) DD-RAM or CG-RAM, the ACC automatically increased by 1 (decreased by 1).
The ACC contents are then output to DB0 to DB6 when RS = 0 and R/W = 1.

5.1.3 Display Data RAM (DD-RAM)

Display data RAM (DD-RAM) stores display data represented in 8-bit character codes. The area in DD-RAM that is not used for display can be used as general data RAM. See below Table for the relationships between DD-RAM addresses and positions on the VFD.

* **The Relationships between DD-RAM Addresses and Positions on the VFD**

	1st Column	2nd Column	3rd Column	.....	15th Column	16th Column
1st ROW	00 Hex	01 Hex	02 Hex	.....	0E Hex	0F Hex
2nd ROW	40 Hex	41Hex	42 Hex	.....	4E Hex	4F Hex

5.1.4 Character Generator ROM (CG-ROM)

The character generator ROM (CG-ROM) generates character patterns of 5*7 dots from 8-bit character codes. It can generate 240 kinds of 5*7 dot character patterns. The character fonts are shown in Appendix-1. The character codes 00H to 0FH are allocated to the CG-RAM.

5.1.5 Character Generator RAM (CG-RAM)

The CG-RAM stores the pixel information (1 = pixel on, 0 = pixel off) for the eight user-definable 5*7 characters including cursor. Valid CG-RAM addresses are 00H to 3FH. CG-RAM not being used to define characters can be used as general purpose RAM (lower 5

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36				

Fig.-10 Dot Assignment

bits only). Character codes 00H to 07H (or 08H to 0FH) are assigned to the user-definable characters (see Fig.-11 Character Font Tables). The table on Page - 11 shows the relationship between the character codes, CG-RAM addresses, and CG-RAM data for each user-definable character.

*** Relationship between CG-RAM Addresses, DD-RAM and 5*7 Dot Patterns (CG-RAM data).**

Character Codes (DD-RAM)								CG-RAM Address						CG-RAM Data								Pattern Example	
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Hex.	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	0	1	1	1	0	0EH	CG-RAM #1 (Example of "A")
											0	0	1	*	*	*	1	0	0	0	1	11H	
											0	1	0	*	*	*	1	0	0	0	1	11H	
											0	1	1	*	*	*	1	1	1	1	1	1FH	
											1	0	0	*	*	*	1	0	0	0	1	11H	
											1	0	1	*	*	*	1	0	0	0	1	11H	
											1	1	0	*	*	*	1	0	0	0	1	11H	
											1	1	1	*	*	*	0	*	*	*	*	00H	Cursor Position
0	0	0	0	*	0	0	1	0	0	1	0	0	0	*	*	*	1	1	1	1	0	1EH	CG-RAM #2 (Example of "B")
											0	0	1	*	*	*	1	0	0	0	1	11H	
											0	1	0	*	*	*	1	0	0	0	1	11H	
											0	1	1	*	*	*	1	1	1	1	0	1EH	
											1	0	0	*	*	*	1	0	0	0	1	11H	
											1	0	1	*	*	*	1	0	0	0	1	11H	
											1	1	0	*	*	*	1	1	1	1	0	1EH	
											1	1	1	*	*	*	0	*	*	*	*	00H	Cursor Position
0	0	0	0	*	0	1	0	0	1	0	0	0	0	*	*	*	0	0	1	1	0	06H	CG-RAM #3 (Example of Euro Currency Symbol)
											0	0	1	*	*	*	0	1	0	0	0	08H	
											0	1	0	*	*	*	1	1	1	0	0	1CH	
											0	1	1	*	*	*	0	1	0	0	0	08H	
											1	0	0	*	*	*	1	1	1	0	0	1CH	
											1	0	1	*	*	*	0	1	0	0	1	09H	
											1	1	0	*	*	*	0	0	1	1	0	06H	
											1	1	1	*	*	*	0	*	*	*	*	00H	Cursor Position

*1) ***:** Indicates no effect (Don't care).*

2) Character code bits 0 to 2 correspond to CG-RAM address bits 3 to 5 (3 bits: 8 types).

3) CG-RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If bit 4 of the 8th line data is 1, 1 bit will light up the cursor regardless of the cursor presence.

4) Character pattern row positions correspond to CG-RAM data bits 0 to 4 (bit 4 being at the left).

*5) CG-RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the "**A**" display example above can be selected by either character code 00H or 08H.*

6) "1" for CG-RAM data corresponds to display selection and 0 to non-selection.

Fig.-11 CG-RAM Font Design Example

5.2 Interfacing to the MPU

This VFD module can interface in either two 4-bit operations or one 8-bit operation, allowing interfacing with 4or 8 bit MPUs.

For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. When to use 4-bit parallel data transfer, DB0 to DB3 keep "H" or "L". The data transfer between the VFD module and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).

The busy flag (BF) are performed before transferring the higher 4 bits. BF checks are not required before transferring the lower 4 bits.

For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

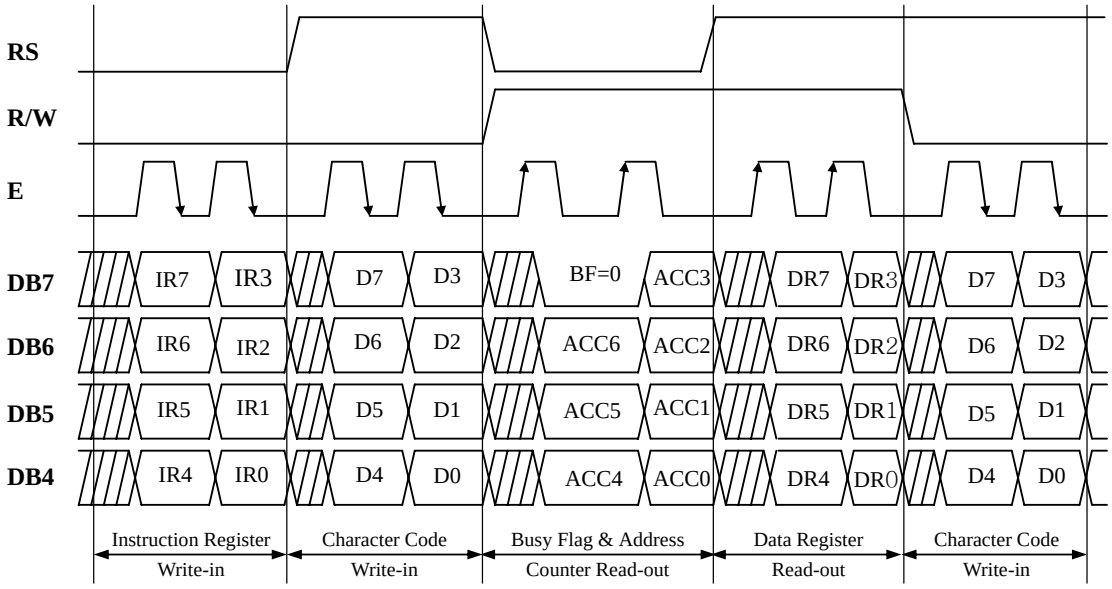


Fig.-12 4-bit Transfer Example (M68)

5.3 MPU Type Select Function

The soldering land is prepared on the rear side of PCB, to set the MPU type of the display module. A soldering iron is required to short soldering lands.

* JP0 = Open .....M68 Interface Mode (Default)
* JP0 = Short .....i80 Interface Mode

5.4 Reset Function

5.4.1 Power-on Reset Function

An internal reset circuit automatically initializes the module when the power is turned on. The following instructions are executed during the initialization.

(1) Display clear
* Fill the DD-RAM with 20H (Space Code)

(2) Set the address counter to 00H
* Set the address counter (ACC) to point DD-RAM.

(3) Display on/off control:
* D = 0.....Display off
* C = 0.....Cursor off
* B = 0.....Blinking off

(4) Entry mode set:
* I/D = 1..... Increment by 1
* S = 0.....No shift

(5) Function set
* IF = 1.....8-bit interface data
* N = 1.....2-line display
* BR0 =0, BR1 =0.....Brightness = 100%

(6) CPU interface type
* JP0 = Open..... M68 type (Factory Setting)
* JP0 = Short..... i80 type

5.4.2 External Reset

When the "JP1" is opened, this function is not effective. Therefore, if a user want to use external H/W reset function (pin #3, /RST), then you must close the soldering switch "JP1". The required pulse width of /RST signal must be longer than 500ns.

6. INSTRUCTIONS

6.1 Outline

Only the instruction register (IR) and the data register (DR) of the VFD controller can be controlled by the user's MPU. Before starting the internal operation of the controller, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the controller is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read or write signal (R/W), and the data bus (DB0 to DB7), make up the controller instructions.

There are four categories of instructions which are:

* Designate controller functions, such as display format, data length, etc.
* Set internal RAM addresses.
* Perform data transfer with internal RAM.
* Perform miscellaneous functions.

Normally, instructions that perform data transfer with internal RAM are used the most.

However, auto-incrementation by 1 (or auto-decrementation by 1) of internal RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag /address read instruction can be executed. Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

*** Instruction List**

Instructions	Control		Instruction Code								Descriptions
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clears all display and sets DD-RAM address 0 in address counter.
Cursor Home	0	0	0	0	0	0	0	0	1	*	Sets DD-RAM address 0 in ACC. Also returns the display being shifted to the original position. DD-RAM contents remain unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF (D), cursor ON/OFF (C), cursor blink of character position (B).
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts display or cursor, keeping DD-RAM contents.
Function Set	0	0	0	0	1	IF	N	*	BR1	BR0	Sets data length (IF), number of display lines(N), Set brightness level(BR1,BR0)
CG-RAM Address Set	0	0	0	1	ACG (CG-RAM Address)						Sets the CG-RAM address.
DD-RAM Address Set	0	0	1	ADD (DD-RAM Address)							Sets the DD-RAM address.
Busy Flag and Address Counter Reading	0	1	BF	ACC (Address Counter)							Reads busy flag (BF) and address counter (ACC).
Data Writing to CG- or DD-RAM	1	0	Character Code								Writes data into CG-RAM or DD-RAM.
Data Reading from CG- or DD-RAM	1	1	Character Code								Reads data from CG-RAM or DD-RAM.
REMARKS: * DD-RAM: Display Data RAM * CG-RAM: Character Generator RAM * ACG: CG-RAM Address * ADD: DD-RAM Address * ACC: Address Counter	* I/D = 1: Increment * I/D = 0: Decrement * S = 1: Display Shift Enabled * S = 0: Cursor Shift Enabled * S/C = 1: Display Shift * S/C = 0: Cursor Move * R/L = 1: Shift to the Right * R/L = 0: Shift to the Left										* IF = 1: 8-bit Operation * IF = 0: 4-bit Operation * N = 1: 2 Lines Display * N = 0: 1 Line Display * BR1, BR0 = 00: 100%, 01: 75%, 10: 50%, 11: 25% * BF = 1: Busy (Internally operating) * BF = 0: Not busy (Instruction acceptable)

6.2 Instruction Descriptions

6.2.1 Display Clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	0	0	0	0	0	1	01H
RS = 0, R/W = 0								

This instruction
(1) Fills all locations in the display data RAM (DD-RAM) with 20H (Blank-character).
(2) Clears the contents of the address counter (ACC) to 00H.
(3) Sets the display for zero character shifts (returns original position).
(4) Sets the address counter (ACC) to point to the DD-RAM.
(5) If the cursor is displayed, moves the cursor to the left most character in the top line (upper line).
(6) Sets the address counter (ACC) to increment on the each access of DD-RAM or CG-RAM.

6.2.2 Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	0	0	0	0	1	*	02H or 03H
RS = 0, R/W = 0								

This instruction
(1) Clears the contents of the address counter (ACC) to 00H.
(2) Sets the address counter (ACC) to point to the DD-RAM.
(3) Sets the display for zero character shift (returns original position).
(4) If the cursor is displayed, moves the left most character in the top line (upper line).

6.2.3 Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	0	0	0	1	I/D	S	04H ~ 07H
RS = 0, R/W = 0								

The I/D bit selects the way in which the contents of the address counter (ACC) are modified after every access to DD-RAM or CG-RAM.

* I/D = 1: The address counter (ACC) is increased.
* I/D = 0: The address counter (ACC) is decreased.

The S bit enables display shift, instead of cursor shift, after each write or read to the DD-RAM.

* S = 1: Display shift enabled.
* S = 0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor.
For example, if S=0 and I/D=1, the cursor would shift one character to the right after a MPU writes to DD-RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on the panel. The cursor will already be shifted in the direction selected by I/D during reads of the DD-RAM, irrespective of the value of S. Similarly reading and writing the CG-RAM always shift the cursor. Also both lines are shifted simultaneously.

*** Cursor Move and Display Shift by the "Entry Mode Set"**

I/D	S	After writing the DD-RAM data	After reading the DD-RAM data
0	0	Cursor moves one character to the left	Cursor moves one character to the left
1	0	Cursor moves one character to the right	Cursor moves one character to the right
0	1	Display shifts one character to the right without cursor	Cursor moves one character to the left
1	1	Display shifts one character to the left without cursor	Cursor moves one character to the right

6.2.4 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	0	0	1	D	C	B	08H ~ 0FH
RS = 0, R/W = 0								

This instruction controls various features of the display.

* D = 1: Display ON, D = 0: Display OFF.
* C = 1: Cursor ON, C = 0: Cursor OFF.
* B = 1: Blinking ON, B = 0: Blinking OFF.

(Blinking is achieved by alternating between a normal and all on display of a character. The cursor blinks with frequency of about 1.0 Hz and DUTY 50%.)

6.2.5 Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	0	1	S/C	R/L	*	*	10H ~ 1FH
RS = 0, R/W = 0								

This instruction shifts the display and/or moves the cursor, one character to the left or right, without reading or writing DD-RAM.

The S/C bit selects movement of the cursor or movement of both the cursor and the display.

* S/C = 1: Shift both cursor and display
* S/C = 0: Shift cursor only

The R/L bit selects left ward or right ward movement of the display and/or cursor.

* R/L = 1: Shift one character right
* R/L = 0: Shift one character left

***Cursor or Display Shift**

S/C	R/L	Cursor Shift	Display Shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to the left	Shift one character to the left
1	1	Shift one character to the right	Shift one character to the right

6.2.6 Function Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	0	1	IF	N	*	BR1	BR0	20H ~ 3FH
RS = 0, R/W = 0								

This instruction sets the width of data bus line (when using parallel interface: IM=1), the number of display line， and brightness control.

This instruction initializes the system, and must be the first instruction executed after power-on.

The IF bit selects a 8-bit or 4-bit bus width interface.

* IF = 1: 8-bit CPU interface using DB7 to DB0
* IF = 0: 4-bit CPU interface using DB7 to DB4

The N bit selects between 1-line or 2-line display.

* N = 1: Select 2 line display (Using anode output A1 to A80)
* N = 0: Select 1 line display (Using anode output A1 to A40. A41 to A80 fixed Low level.)

BR1, BR0 flag controls the brightness of VFD by modulating pulse width of Anode output as follows.

* BR0, BR1 = (0, 0): Brightness = 100%
  (0, 1): Brightness = 75%
  (1, 0): Brightness = 50%
  (1, 1): Brightness = 25%

6.2.7 Set CG-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
0	1	ACG						40H ~ 7FH
RS = 0, R/W = 0								

This instruction:
(1) Load a new 6-bit address into the address counter (ACC).
(2) Sets the address counter (ACC) to address CG-RAM.
Once "Set CG-RAM Address" has been executed, the contents of the address counter (ACC) will be automatically modified after every access of CG-RAM, as determined by the "Entry Mode Set" instruction.
The active width of the address counter (ACC), when it is addressing CG-RAM, is 6 bits, so the counter will wrap around to 3FH from 00H if more than 64 bytes of data are written into CG-RAM.

6.2.8 Set DD-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
1	ADD							80H ~ A7H for 1st Line C0H ~ E7H for 2nd Line
RS = 0, R/W = 0								

This instruction:
(1) Loads a new 7-bit address into the address counter (ACC).
(2) Sets the address counter (ACC) to point to the DD-RAM.
Once the "Set DD-RAM Address" instruction has been executed, the contents of the address counter (ACC) will be automatically modified after each access of DD-RAM, as selected by the "Entry Mode Set" instruction.

***Valid DD-RAM Address Ranges**

	Number of Character	Address Range
1st line	40	00H to 27H
2nd line	40	40H to 67H

6.2.9 Read Busy Flag and Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						
RS = 0, R/W = 1							

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress.

* BF = 1: busy state
* BF = 0: ready for next instruction, command receivable.

The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter (ACC) in binary AAAAAAA is read out. This address counter (ACC) is used by both CG-RAM and DD-RAM addresses, and its value is determined by the previous instruction. The address contents are the same as the instructions setting the CG-RAM address and DD-RAM address.

6.2.10 Write Data to CG or DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
Character Code (Write-in)								00H ~ 0FH for CG-RAM Code 10H ~ FFH for CG-ROM Code
RS = 1, R/W = 0								

This instruction writes 8-bit binary data (DB7 to DB0) into CG-RAM or DD-RAM. To write into CG-RAM or DD-RAM is determined by the previous specification of the CG-RAM or DD-RAM address setting. After a write, the address is automatically increased or decreased by 1 according to the entry mode. The entry mode also determines the display shift. When data is written to the CG-RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

6.2.11 Read Data from CG or DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex. Range
Character Code (Read-out)								00H ~ 0FH for CG-RAM Code 10H ~ FFH for CG-ROM Code
RS = 1, R/W = 1								

This instruction reads 8-bit binary data (DB7 to DB0) from CG-RAM or DD-RAM.
The previous designation determines whether CG-RAM or DD-RAM is to be read. Before entering this read instruction, either CG-RAM or DD-RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions don't need to be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD-RAM).
The operation of the cursor shift instruction is the same as the set DD-RAM address instruction.
After a read, the entry mode automatically increases or decreases the address by 1.

**Note): The address counter (ACC) is automatically increased or decreased by 1 after a writing instruction to CG-RAM or DD-RAM is executed. The RAM data selected by the ACC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD-RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.*

6.3 Example of Initialization After Power ON (8-bits data, date increment etc.)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
										Wait for 100 us after Power ON
0	0	0	0	1	1	1	*	0	0	Function set: - Data length: 8 bits - Display line No.: 2 lines - Brightness: 100%
0	0	0	1	0	0	0	0	0	0	CG-RAM address set to 00H
1	0	*	*	*	D4	D3	D2	D1	D0	Writes data into CG-RAM (the user-definable characters) 64 bytes in total (8 characters)
		*	*	*	D4	D3	D2	D1	D0	
		.....					.....			
		*	*	*	D4	D3	D2	D1	D0	
0	0	1	0	0	0	0	0	0	0	DD-RAM address set to 00H (the first column of upper line)
1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data into DD-RAM (choose the character codes to display in upper line) Totally 16 bytes in the upper line (16 characters)
		D7	D6	D5	D4	D3	D2	D1	D0	
		.....					.....			
		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	1	0	0	0	0	0	0	DD-RAM address set to 40H (the first column of lower line)
1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data into DD-RAM (choose the character codes to display in lower line) Totally 16 bytes in the lower line (16 characters)
		D7	D6	D5	D4	D3	D2	D1	D0	
		.....					.....			
		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	1	0	0	Display ON, Cursor OFF, Cursor blink OFF

* Note) "Dn" is the binary data to be written-in.

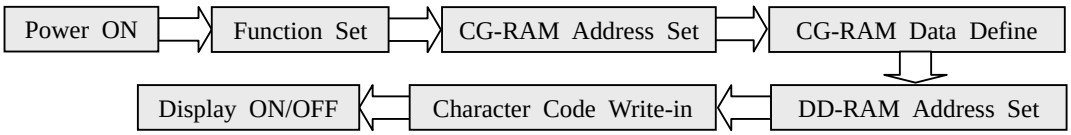
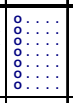
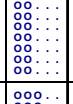
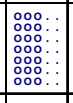
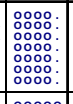
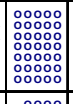
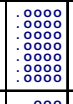
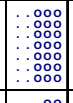
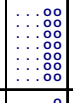
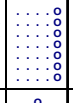
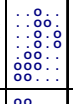
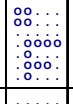
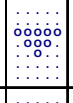
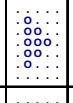
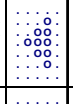


Fig.-13 Example of Initialization after Power ON

Appendix-1. Character Font Table (CG-ROM and CG-RAM Address Codes)

Upper / Lower Nibble		D7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D3 D2 D1 D0			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	CG-RAM (#1)																
0 0 0 1	1	CG-RAM (#2)																
0 0 1 0	2	CG-RAM (#3)																
0 0 1 1	3	CG-RAM (#4)																
0 1 0 0	4	CG-RAM (#5)																
0 1 0 1	5	CG-RAM (#6)																
0 1 1 0	6	CG-RAM (#7)																
0 1 1 1	7	CG-RAM (#8)																
1 0 0 0	8	CG-RAM (#1)																
1 0 0 1	9	CG-RAM (#2)																
1 0 1 0	A	CG-RAM (#3)																
1 0 1 1	B	CG-RAM (#4)																
1 1 0 0	C	CG-RAM (#5)																
1 1 0 1	D	CG-RAM (#6)																
1 1 1 0	E	CG-RAM (#7)																
1 1 1 1	F	CG-RAM (#8)