

# MOS FIELD EFFECT POWER TRANSISTORS

## 2SJ326, 2SJ326-Z

### SWITCHING

### P-CHANNEL POWER MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

The 2SJ326 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

- Low On-state Resistance  
 $R_{DS(on)} = 0.28 \Omega$  TYP. ( $V_{GS} = -10$  V,  $I_D = -1$  A)  
 $R_{DS(on)} = 0.50 \Omega$  TYP. ( $V_{GS} = -4$  V,  $I_D = -0.8$  A)
- Low  $C_{iss}$   $C_{iss} = 320$  pF TYP.
- Built-in G-S Gate Protection Diode

#### QUALITY GRADE

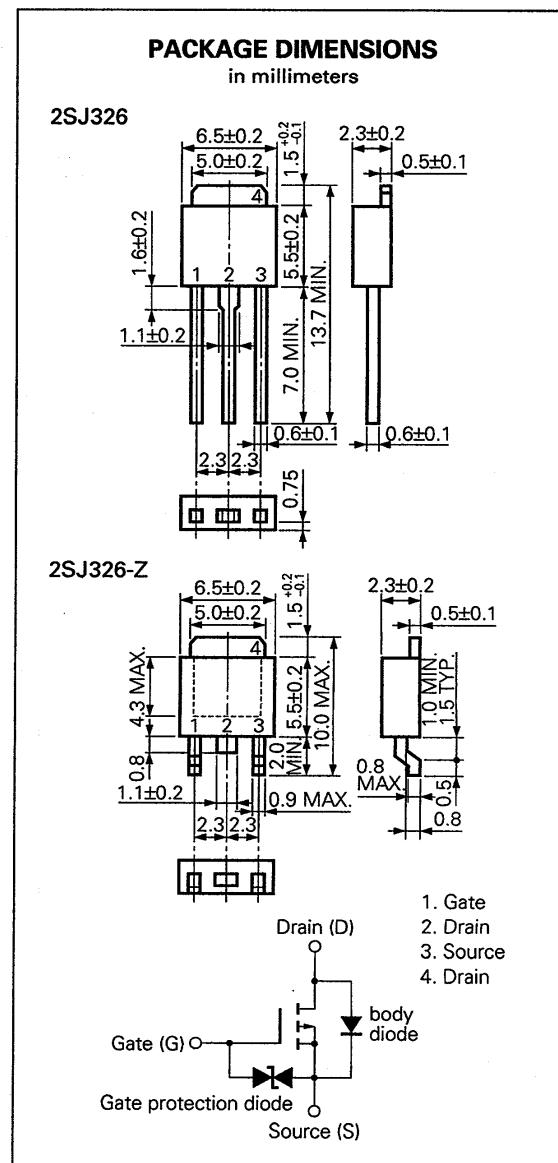
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25$ °C)

Drain to Source Voltage	$V_{DSS}$	-60	V
Gate to Source Voltage (AC)	$V_{GSS}$	$\mp 20$	V
Gate to Source Voltage (DC)	$V_{GSS}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 2.0$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\mp 8.0$	A
Total Power Dissipation ( $T_c = 25$ °C)	$PT_1$	20	W
Total Power Dissipation ( $T_a = 25$ °C)	$PT_2$	1.0	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

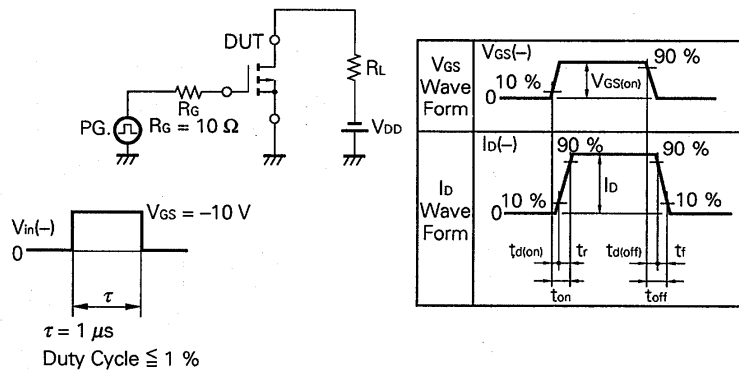
\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$



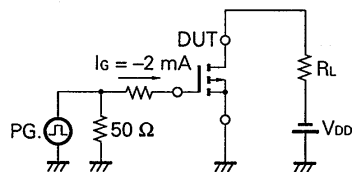
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.28	0.37	Ω	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.50	0.68	Ω	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -0.8 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	-1.0	-1.5	-2.0	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA
Forward Transfer Admittance	y <sub>fs</sub>	1.0	1.8		S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 A
Drain Leakage Current	I <sub>DSS</sub>			-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		320		pF	V <sub>DS</sub> = -10 V
Output Capacitance	C <sub>oss</sub>		220		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		75		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		5		ns	V <sub>GS(on)</sub> = -10 V
Rise Time	t <sub>r</sub>		15		ns	V <sub>DD</sub> = -30 V
Turn-Off Delay Time	t <sub>d(off)</sub>		40		ns	I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		25		ns	R <sub>L</sub> = 30 Ω
Total Gate Charge	Q <sub>G</sub>		12		nC	V <sub>GS</sub> = -10 V
Gate to Source Charge	Q <sub>GS</sub>		1		nC	I <sub>D</sub> = -2.0 A
Gate to Drain Charge	Q <sub>GD</sub>		5		nC	V <sub>DD</sub> = -48 V
Body Diode Forward Voltage	V <sub>F</sub>		0.9		V	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0
ESD	V <sub>ESD</sub>		±130		V	C = 200 pF, R = 0, Single Pulse
Reverse Recovery Time	t <sub>rr</sub>		72		ns	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		30		nC	di/dt = 50 A/μs

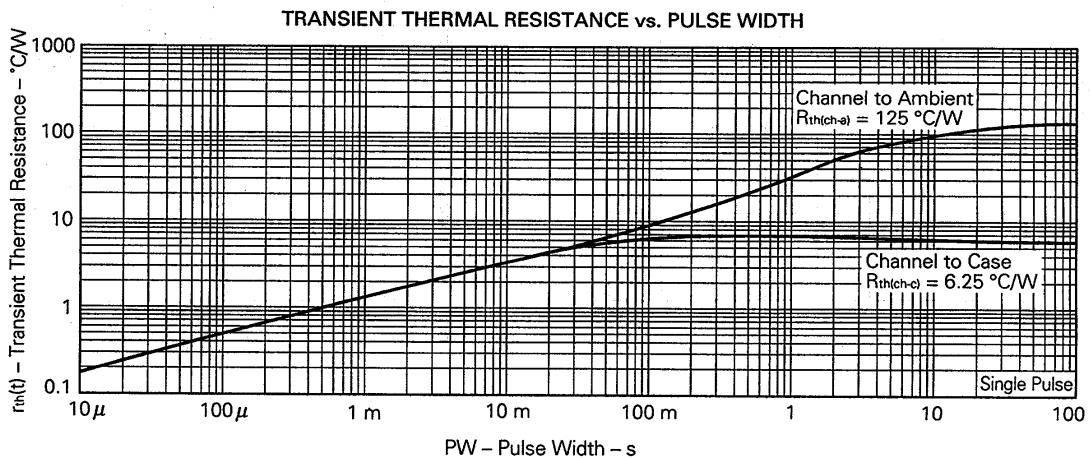
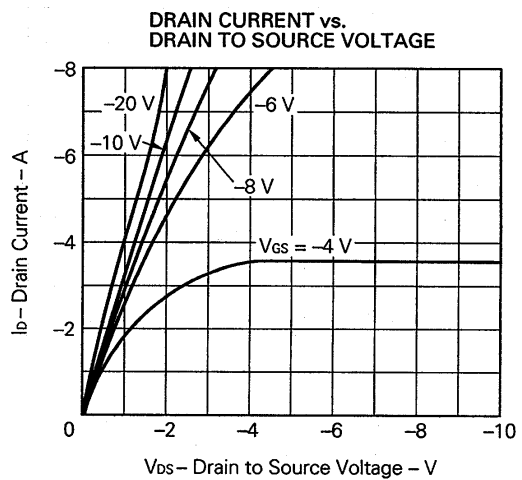
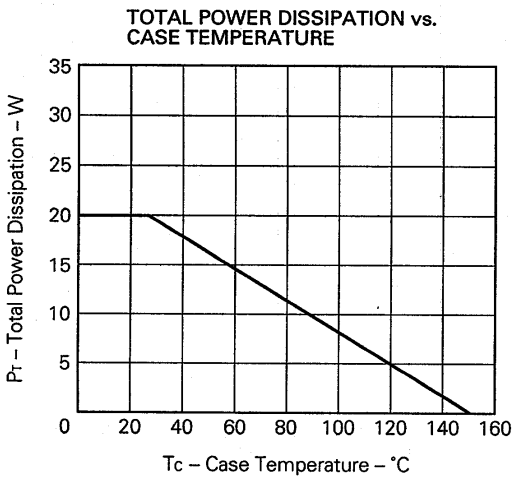
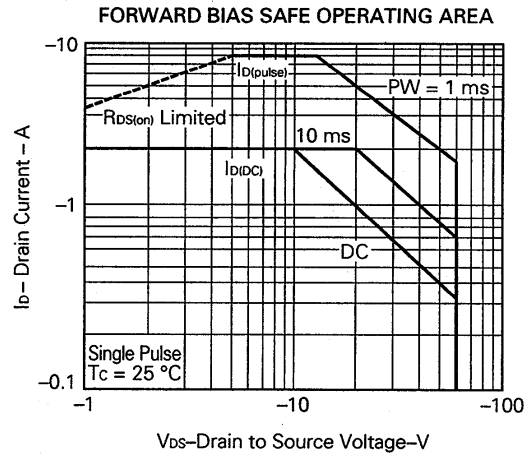
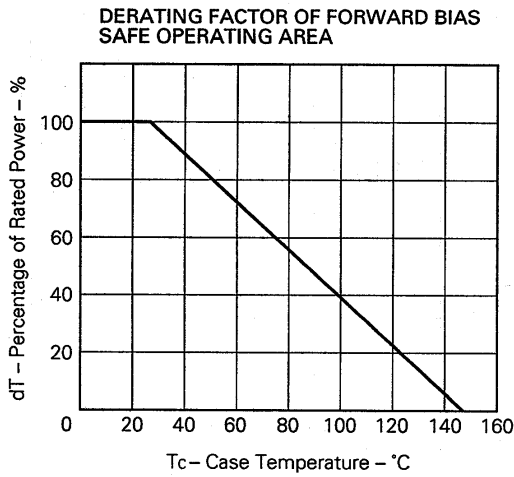
**Test Circuit 1: Switching Time**

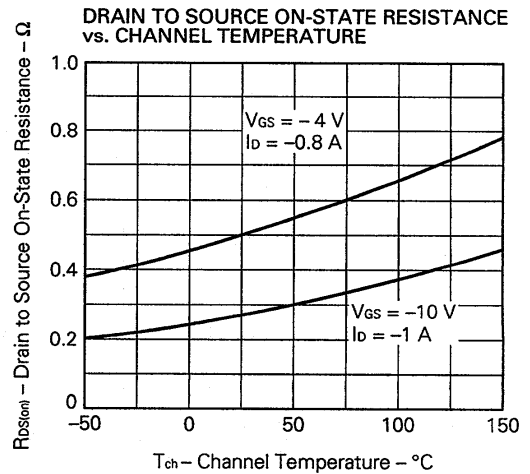
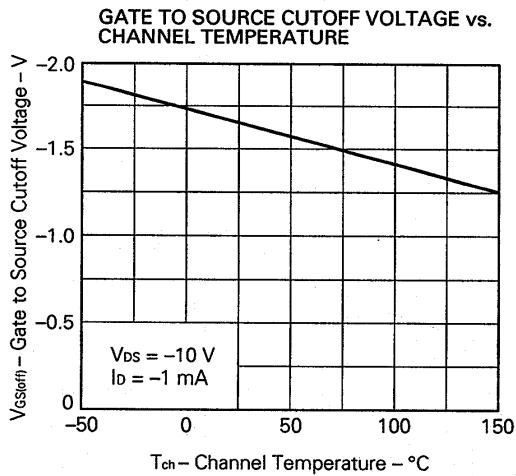
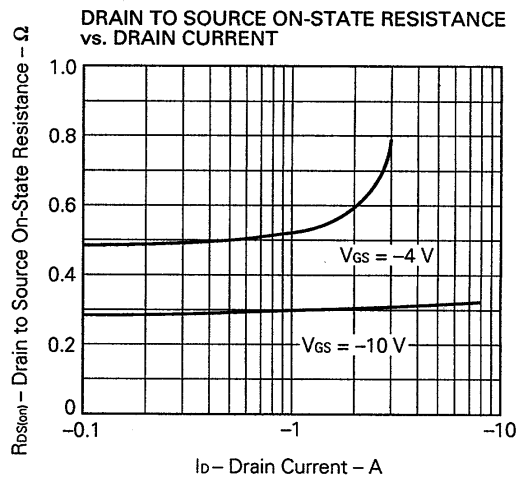
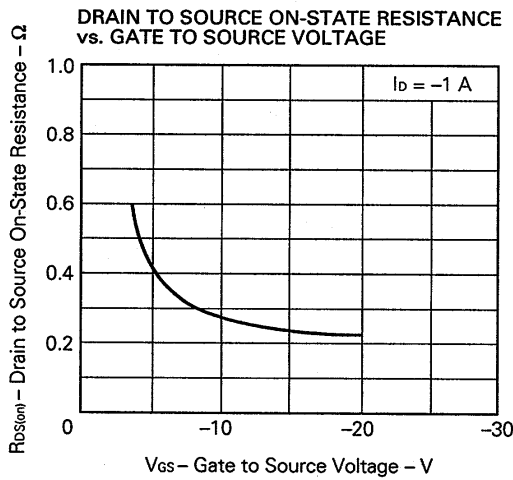
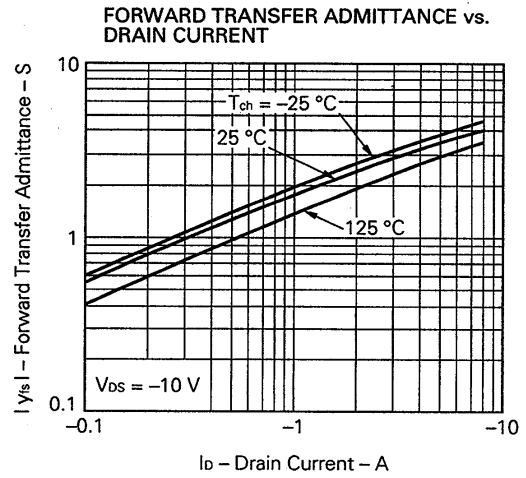
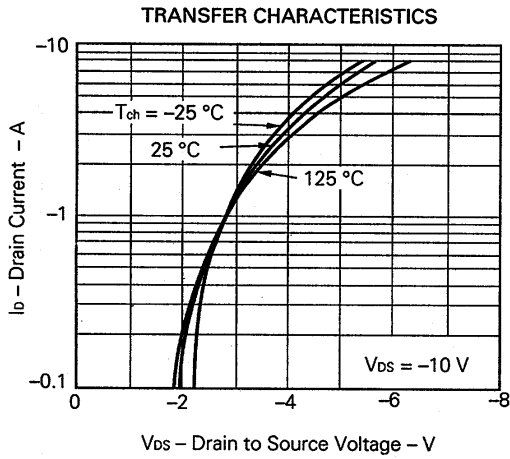


**Test Circuit 2: Gate Charge**

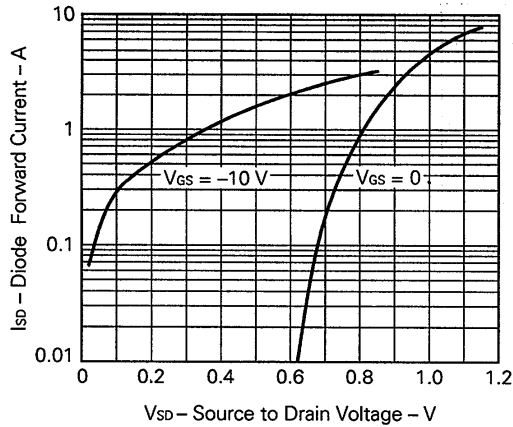


ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

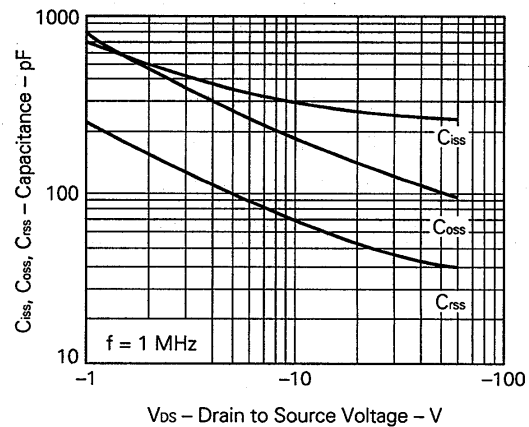




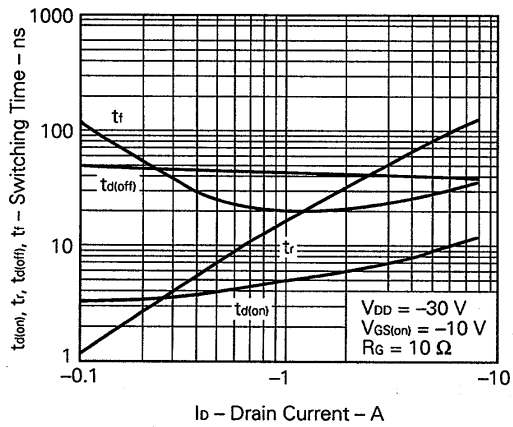
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



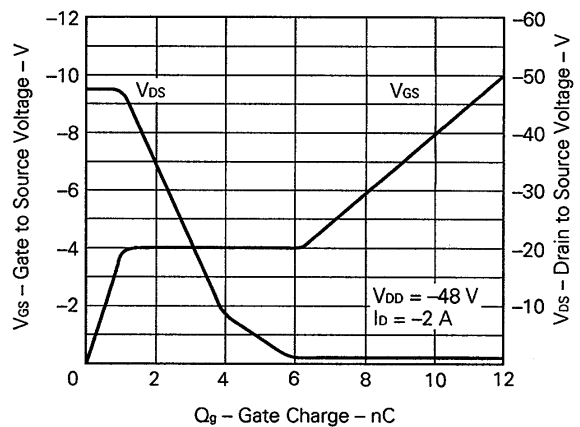
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



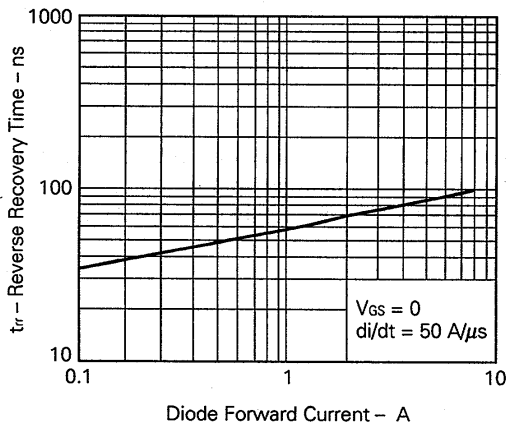
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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