

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR  
**2SJ328, 2SJ328-Z**

**SWITCHING**  
**P-CHANNEL POWER MOS FET**  
**INDUSTRIAL USE**

**DESCRIPTION**

The 2SJ328 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} = 48 \text{ m}\Omega \text{ TYP. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$   
 $R_{DS(on)} = 85 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4 \text{ V, } I_D = -8 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 2 \text{ 150 pF TYP.}$
- Built-in G-S Gate Protection Diodes

**QUALITY GRADE**

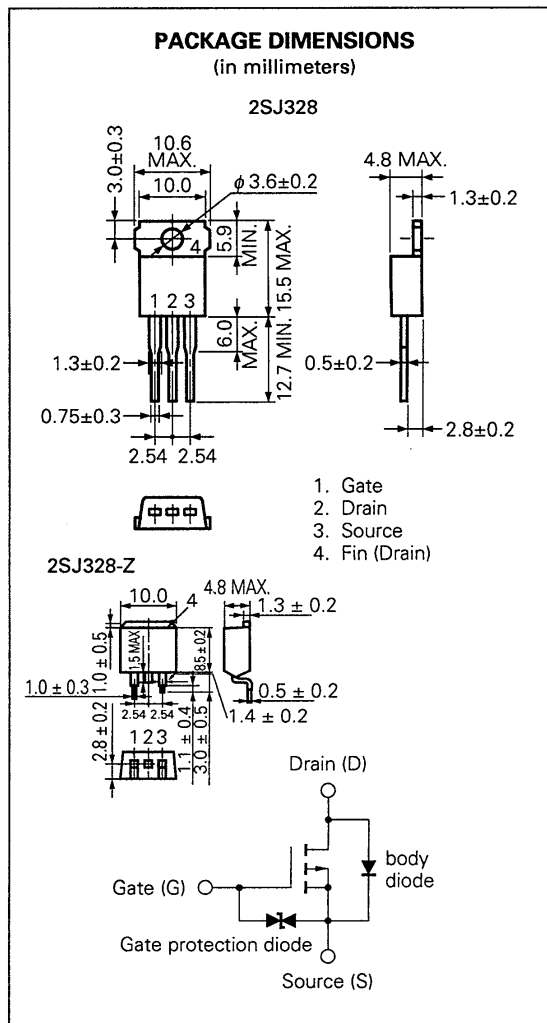
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = 25 °C)**

Drain to Source Voltage	V <sub>DSS</sub>	-60	V
Gate to Source Voltage	V <sub>GSS(AC)</sub>	±20	V
Gate to Source Voltage	V <sub>GSS(DC)</sub>	-20, +10	V
Drain Current (DC)	I <sub>D(DC)</sub>	±20	A
Drain Current (pulse)	I <sub>D(pulse)*</sub>	±80	A
Total Power Dissipation (T <sub>c</sub> = 25 °C)	P <sub>T1</sub>	75	W
Total Power Dissipation (T <sub>a</sub> = 25 °C)	P <sub>T2</sub>	1.5	W
Channel Temperature	T <sub>ch</sub>	150 °C MAX.	
Storage Temperature	T <sub>stg</sub>	-55 to +150 °C	

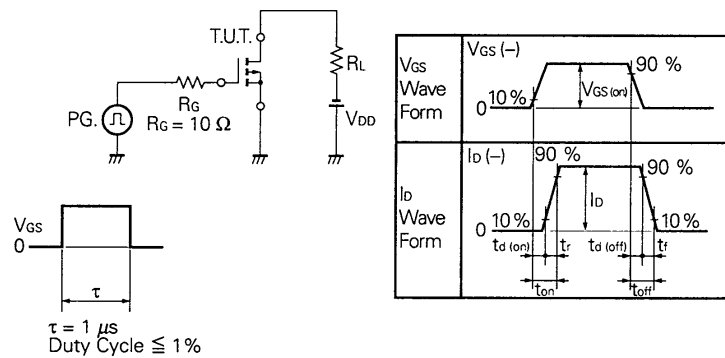
\* PW ≤ 10 μs, Duty Cycle ≤ 1 %



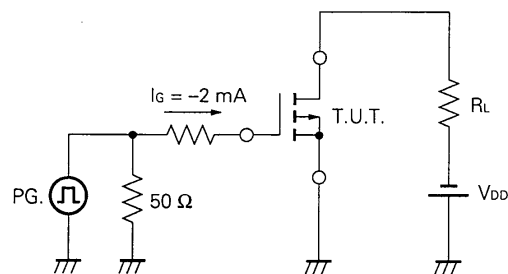
ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		48	60	mΩ	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		85	110	mΩ	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -8 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	-1.0	-1.5	-2.0	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA
Forward Transfer Admittance	y <sub>fs</sub>	8.0	13		S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A
Drain Leakage Current	I <sub>DSS</sub>			-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2 150		pF	V <sub>DS</sub> = -10 V
Output Capacitance	C <sub>oss</sub>		1 100		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		530		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		40		ns	V <sub>GS(on)</sub> = -10 V V <sub>DD</sub> = -30 V I <sub>D</sub> = -10 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 3.0 Ω
Rise Time	t <sub>r</sub>		180		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		240		ns	
Fall Time	t <sub>f</sub>		230		ns	
Total Gate Charge	Q <sub>G</sub>		85		nC	V <sub>GS</sub> = -10 V I <sub>D</sub> = -20 A V <sub>DD</sub> = -48 V
Gate to Source Charge	Q <sub>GS</sub>		7		nC	
Gate to Drain Charge	Q <sub>GD</sub>		35		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.0		V	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		120		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		260		nC	di/dt = 50 A/μs

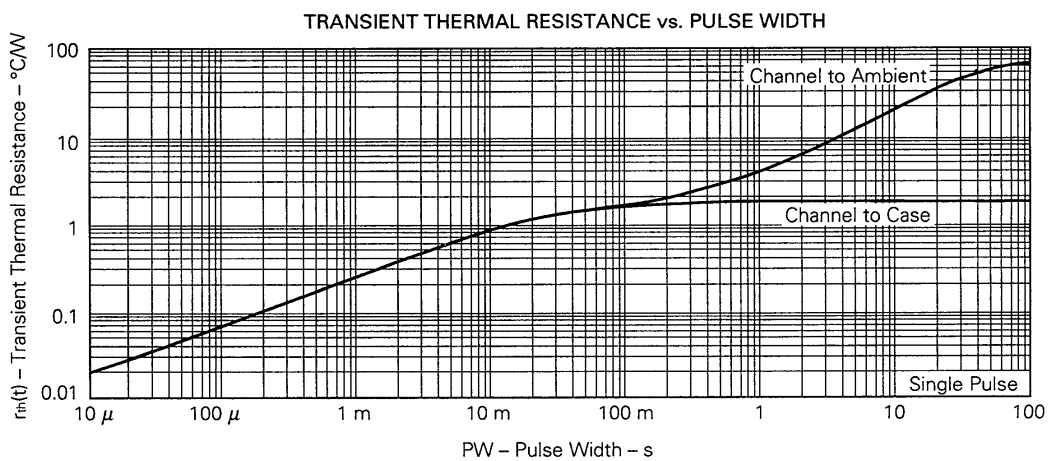
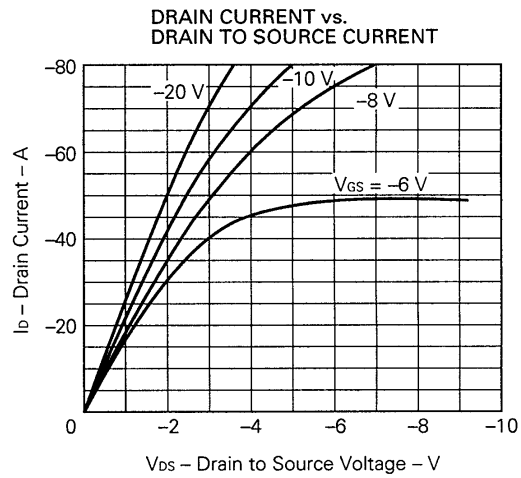
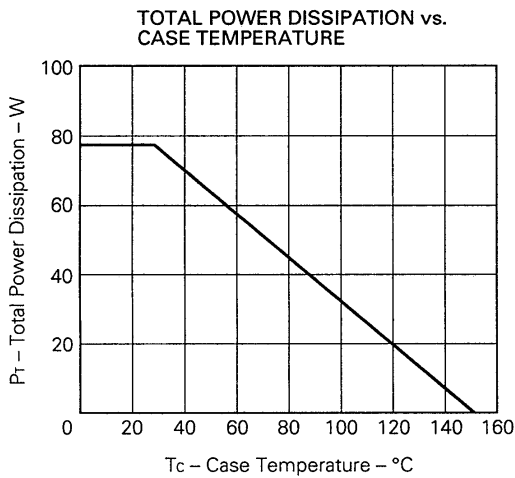
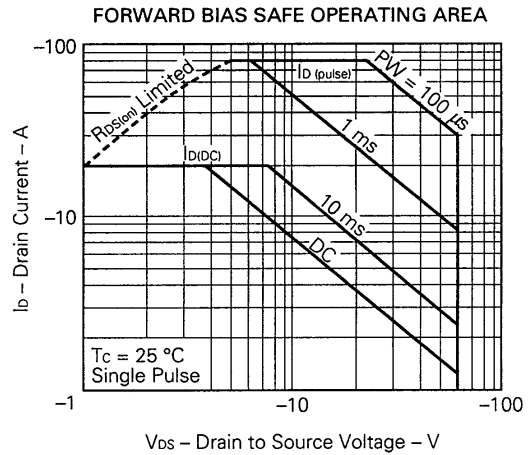
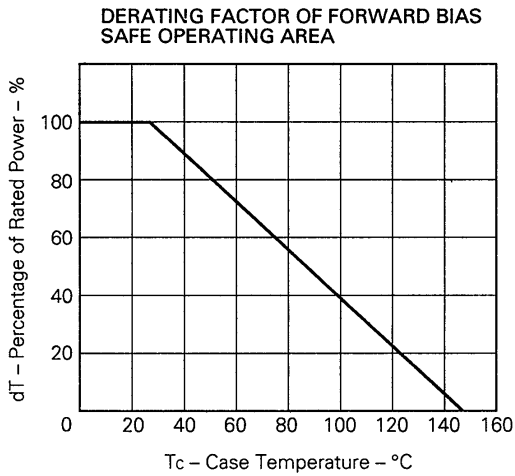
Test Circuit 1: Switching Time



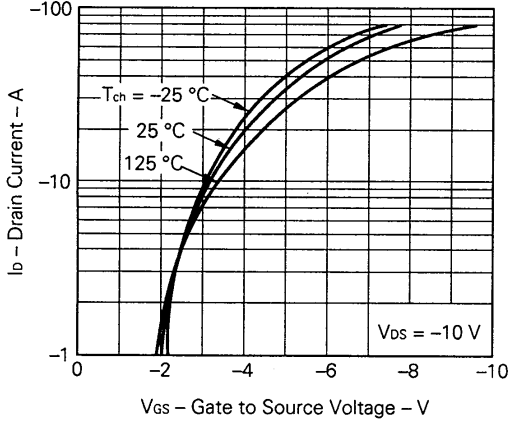
Test Circuit 2: Gate Charge



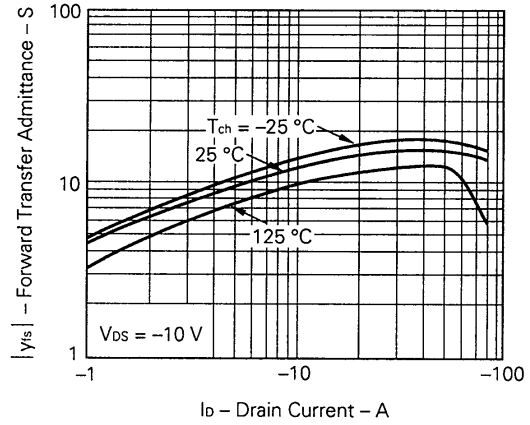
ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)



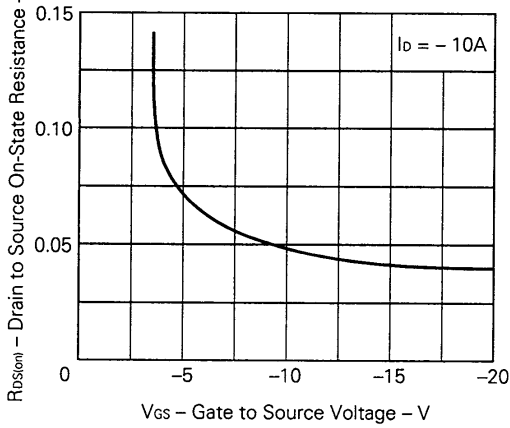
TRANSFER CHARACTERISTICS



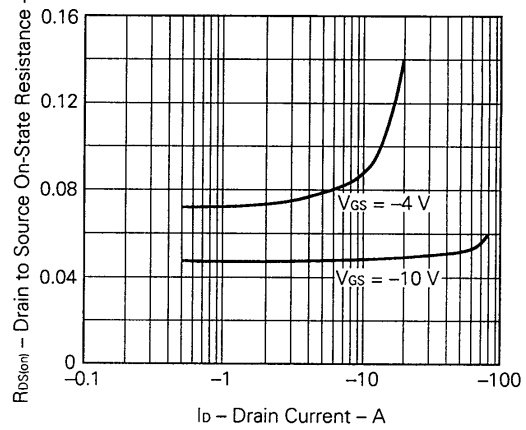
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



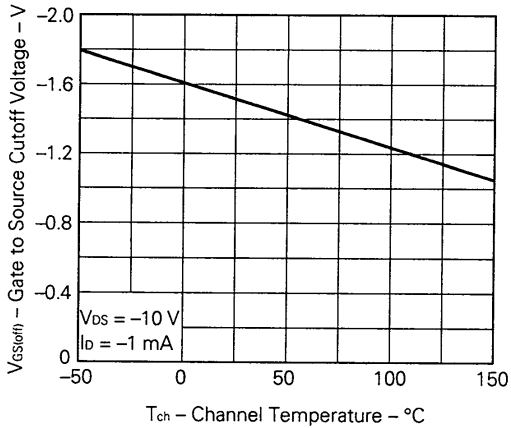
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



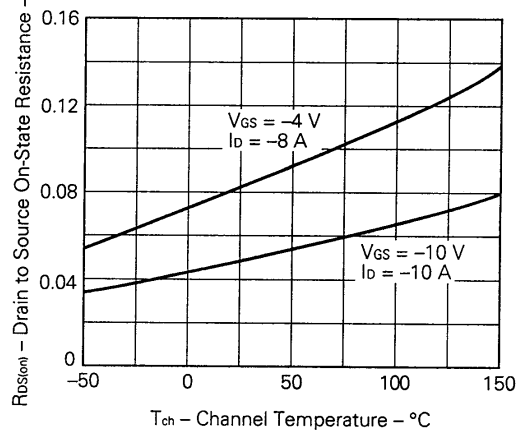
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



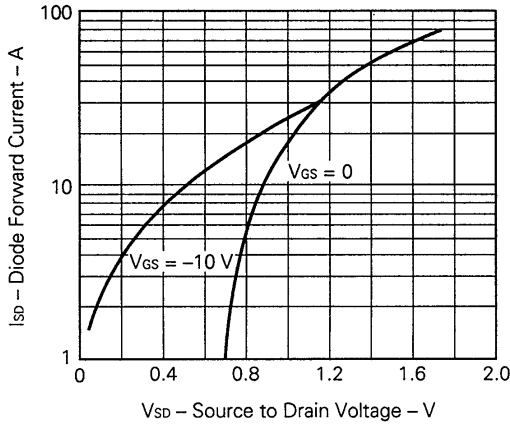
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



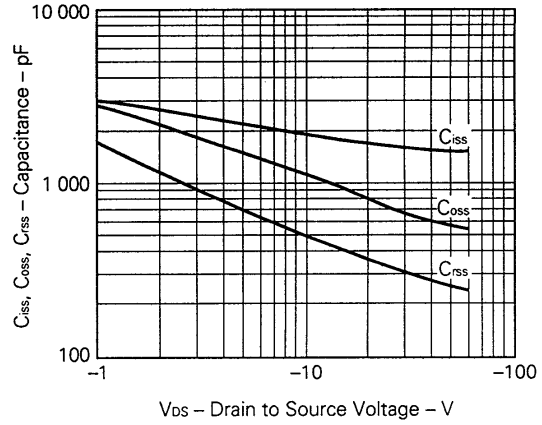
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



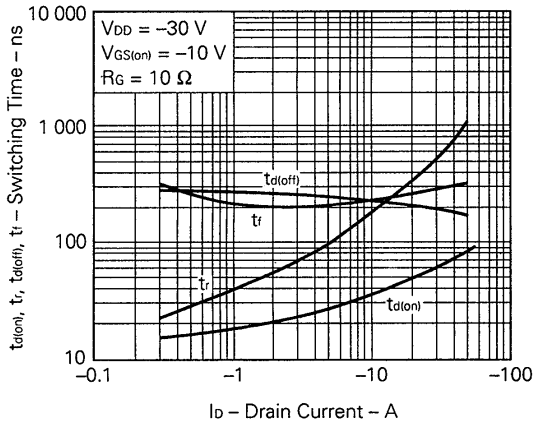
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



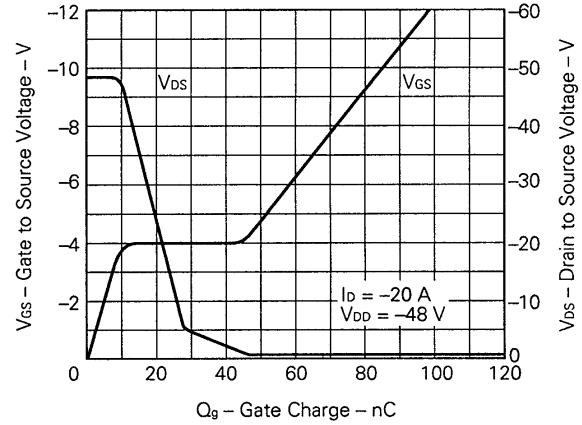
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



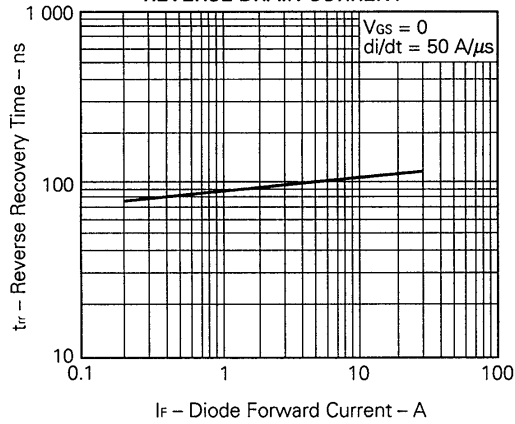
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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