

# SRAM

# 128K X 16 HIGH SPEED CMOS STATIC RAM

## FEATURES

- Fast access time : 8/10/12/15 ns
- Low-power consumption :  
Stand-by current (CMOS input/output)  
Max. 300 uA
- Single +3.0V to 3.6V Power Supply
- TTL compatible , Tri-state output
- Common I/O capability
- Automatic power-down when deselected
- Available in 44-PIN TSOP-II and 48-pin CSP packages

## PART NUMBER EXAMPLES

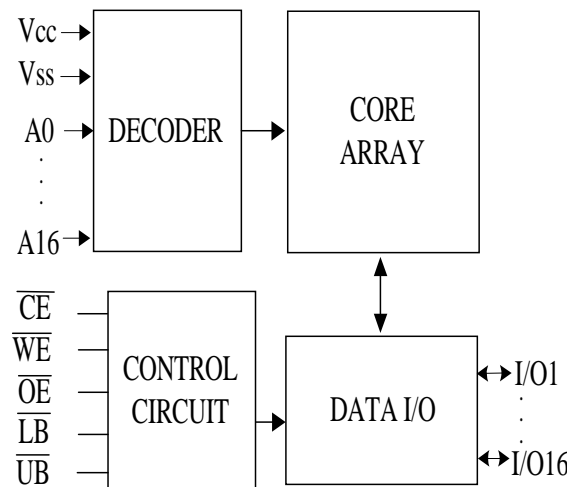
Part Number	Access time	Package
T14L2M16A-10S	10ns	TSOP-II
T14L2M16A-12C	12ns	CSP
T14L2M16A-10S	10ns	TSOP-II
T14L2M16A-12C	12ns	CSP

## GENERAL DESCRIPTION

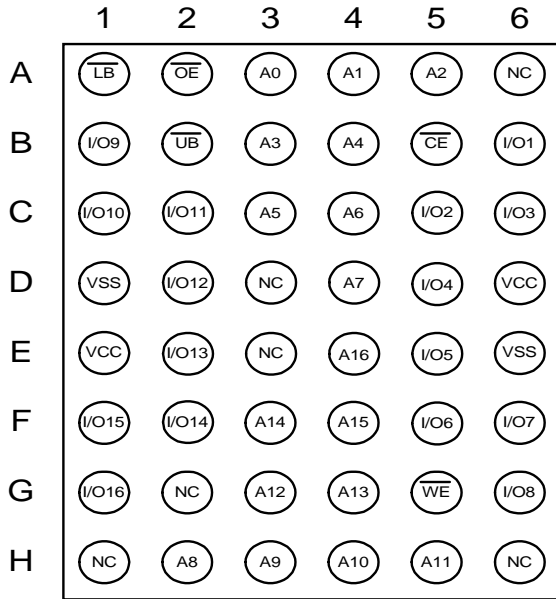
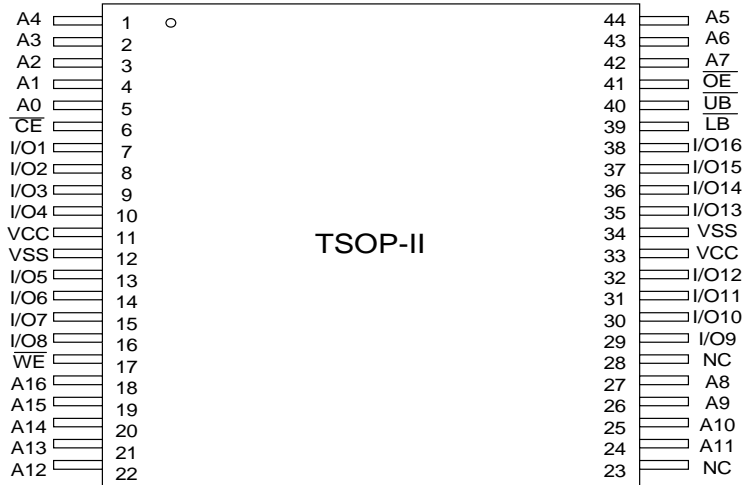
The T14L2M16A is a very fast access time CMOS Static RAM, organized as 131,072 words by 16 bits . This device is fabricated by high performance CMOS technology. It can be operated under wide power supply voltage range from +3.0V to +3.6V.

The T14L2M16A inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. Data retention is guaranteed at a power supply voltage as low as 2V.

## BLOCK DIAGRAM



**PIN CONFIGURATIONS**



48-Ball CSP TOP VIEW (Ball Down)

**PIN DESCRIPTIONS**

SYMBOL	DESCRIPTIONS		SYMBOL	DESCRIPTIONS
A0 ~ A16	Address inputs		$\overline{\text{LB}}$	Lower byte (I/O 1~8)
I/O1~I/O16	Data inputs/outputs		$\overline{\text{UB}}$	Upper byte (I/O 9~16)
$\overline{\text{CE}}$	Chip enable		VCC	Power supply
$\overline{\text{WE}}$	Write enable input		VSS	Ground
$\overline{\text{OE}}$	Output enable input		NC	No connection

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYM	MIN.	MAX.	UNIT
Voltage on Any Pin Relative to VSS	V <sub>R</sub>	-0.5	+4.6 V	V
Power Dissipation	P <sub>D</sub>	-	1.0	W
Storage Temperature	T <sub>STG</sub>	-55	+150	°C
Temperature Under Bias	I <sub>BIAS</sub>	0	+70	°C

\*Note: Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O 1~8	I/O 9~16	MODE	Power
H	X*	X*	X*	X*	High-Z	High-Z	Deselected	Standby
L	X*	X*	H	H	High-Z	High-Z	Output Disabled	Active
L	H	H	L	X*	High-Z	High-Z	Output Disabled	Active
L	H	H	X*	L	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	L	H	L	L	Data Out	Data Out	Word Read	Active
L	X*	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	X*	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	X*	L	L	L	Data In	Data In	Word Write	Active

\*Note: X = Don't Care (Must be low or high state), L = Low, H = High

**RECOMMENDED OPERATING CONDITIONS**

- (Ta = 0 ~ +70 °C)

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
	V <sub>SS</sub>	0.0	0.0	0.0	V
Input Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3	V
	V <sub>IL</sub>	-0.2	-	0.8	V

**OPERATING CHARACTERISTICS**

 - (V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V, Ta = 0 ~ +70 °C)

PARAMETER	SYM.	TEST CONDITIONS	-8		-10		-12		-15		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = Max, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-	1	-	1	-	1	-	1	uA
Output Leakage Current	I <sub>LO</sub>	$\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ V <sub>IO</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-	1	-	1	-	1	-	1	uA
Operating Power Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = Max, $\overline{\text{CE}} = V_{IL}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0mA, f = max	-	60	-	55	-	50	-	45	mA
Standby Power Supply Current (TTL Level)	I <sub>SB</sub>	$\overline{\text{CE}} = V_{IH}$ , other input = V <sub>IL</sub> or V <sub>IH</sub>	-	15	-	15	-	15	-	15	mA
Standby Power Supply Current (CMOS Level)	I <sub>SBI</sub>	$\overline{\text{CE}} \geq V_{CC} - 0.2V$ or V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	-	300	-	300	-	300	-	300	uA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	-	0.4	-	0.4	-	0.4	-	0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	2.4	-	2.4	-	V

**CAPACITANCE**

(f = 1 MHz, Ta = 25°C,)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	$C_{IN}$	$V_{IN} = 0V$	6	pF
Input/ Output Capacitance	$C_{I/O}$	$V_{IN} = V_{OUT} = 0V$	8	pF

**Note:** This parameter is guaranteed by device characterization and is not production tested.

**AC TEST CONDITIONS**

PARAMETER	CONDITIONS
Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	3.0 ns
Input and Output Timing Reference Level	1.4V
Output Load	$C_L = 30pF + 1TTL$ Load

**AC TEST LOADS AND WAVEFORM**

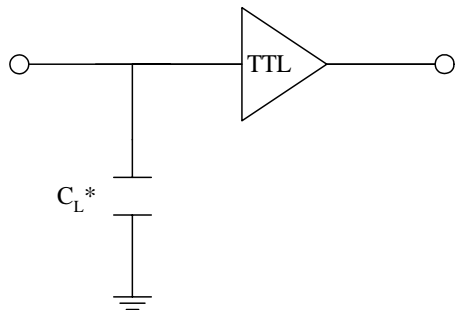


Fig.A \* Including Scope and Jig Capacitance

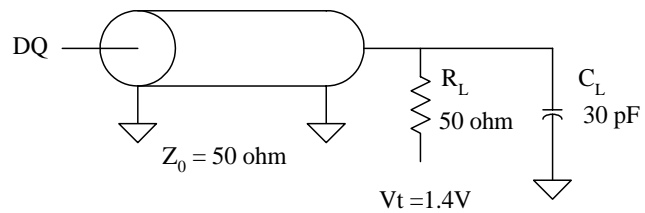


Fig.B Output Load Equivalent

**AC CHARACTERISTICS**( $V_{CC}=3.0$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a = 0 \sim +70 \text{ }^\circ\text{C}$ )

**(1) READ CYCLE**

PARAMETER	SYM.	-8		-10		-12		-15		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	8	-	10	-	12	-	15	-	ns
Address Access Time	$t_{AA}$	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	$t_{ACE}$	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	$t_{OE}$	-	3	-	4	-	5	-	6	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	3	-	ns
Chip Enable to Output in Low-Z	$t_{LZ}$	3	-	3	-	3	-	3	-	ns
Chip Disable to Output in High-Z	$t_{HZ}$	-	3	-	4	-	5	-	6	ns
Output Enable to Output in Low-Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High-Z	$t_{OHZ}$	-	3	-	4	-	5	-	6	ns
$\overline{LB}$ , $\overline{UB}$ Access Time	$t_{BA}$	-	3	-	4	-	5	-	6	ns
$\overline{LB}$ , $\overline{UB}$ Enable to Output in Low-Z	$t_{BLZ}$	0	-	0	-	0	-	0	-	ns
$\overline{LB}$ , $\overline{UB}$ Disable to Output in High-Z	$t_{BHZ}$	-	3	-	4	-	5	-	6	ns

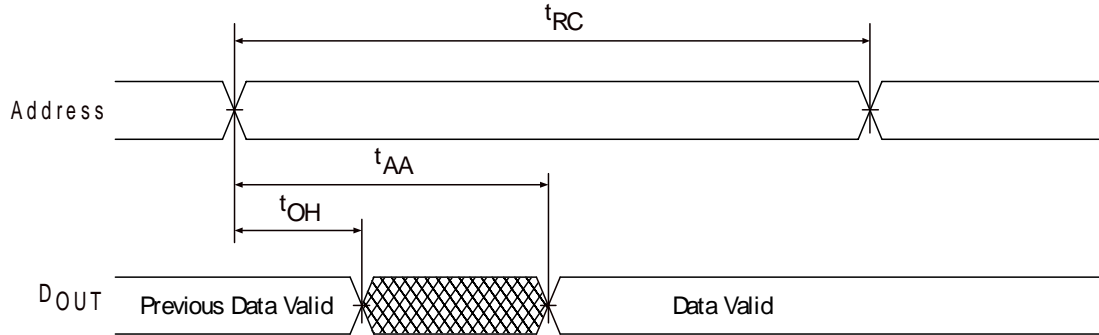
**(2)WRITE CYCLE**

PARAMETER	SYM.	-8		-10		-12		-15		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{WC}$	8	-	10	-	12	-	15	-	ns
Chip Enable to Write End	$t_{CW}$	7	-	8	-	8	-	10	-	ns
Address Valid to Write End	$t_{AW}$	7	-	8	-	8	-	10	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	6	-	7	-	8	-	10	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	0	-	ns
Data Valid to Write End	$t_{DW}$	4	-	5	-	6	-	7	-	ns
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Write Enable to Output in High-Z	$t_{WHZ}$	-	3	-	4	-	5	-	6	ns
Output Active from Write End	$t_{OW}$	0	-	0	-	0	-	0	-	ns

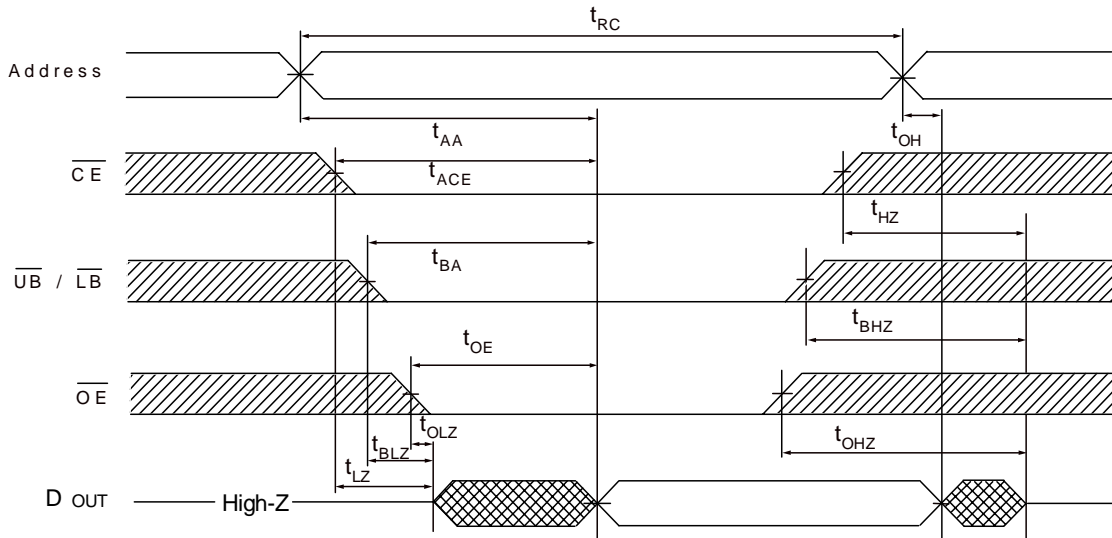
**TIMING WAVEFORMS**

**READ CYCLE 1**

(Address Controlled,  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{LB}$  or/and  $\overline{UB} = V_{IL}$ )



**READ CYCLE 2 ( $\overline{WE} = V_{IH}$ )**

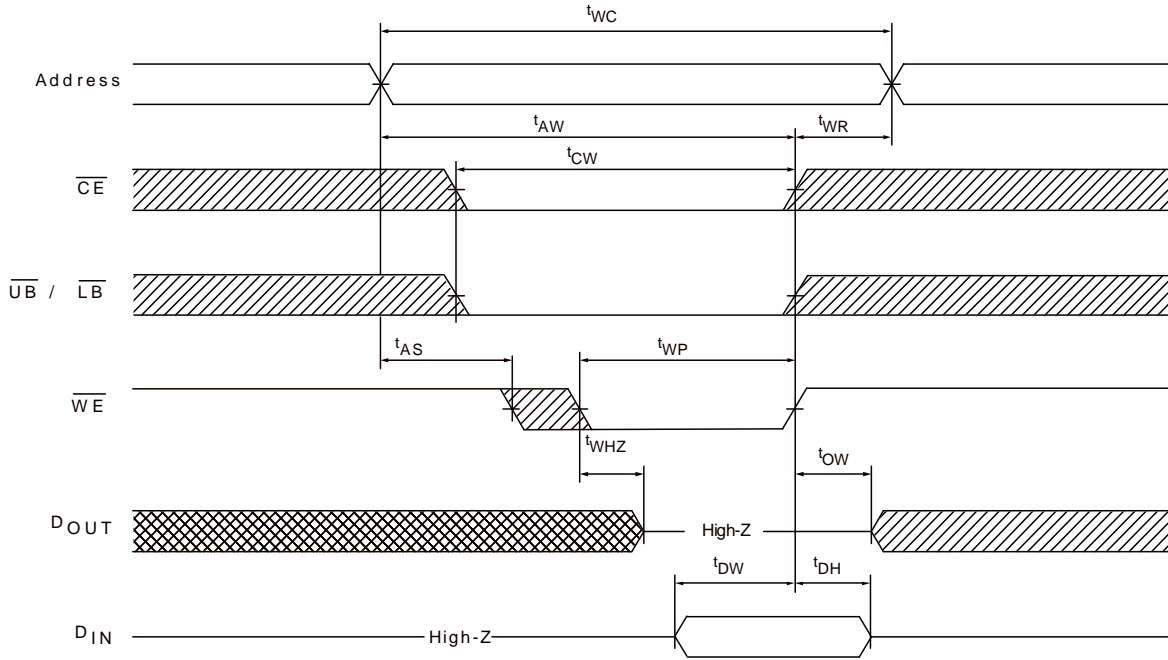


DON'T CARE  
 UNDEFINED

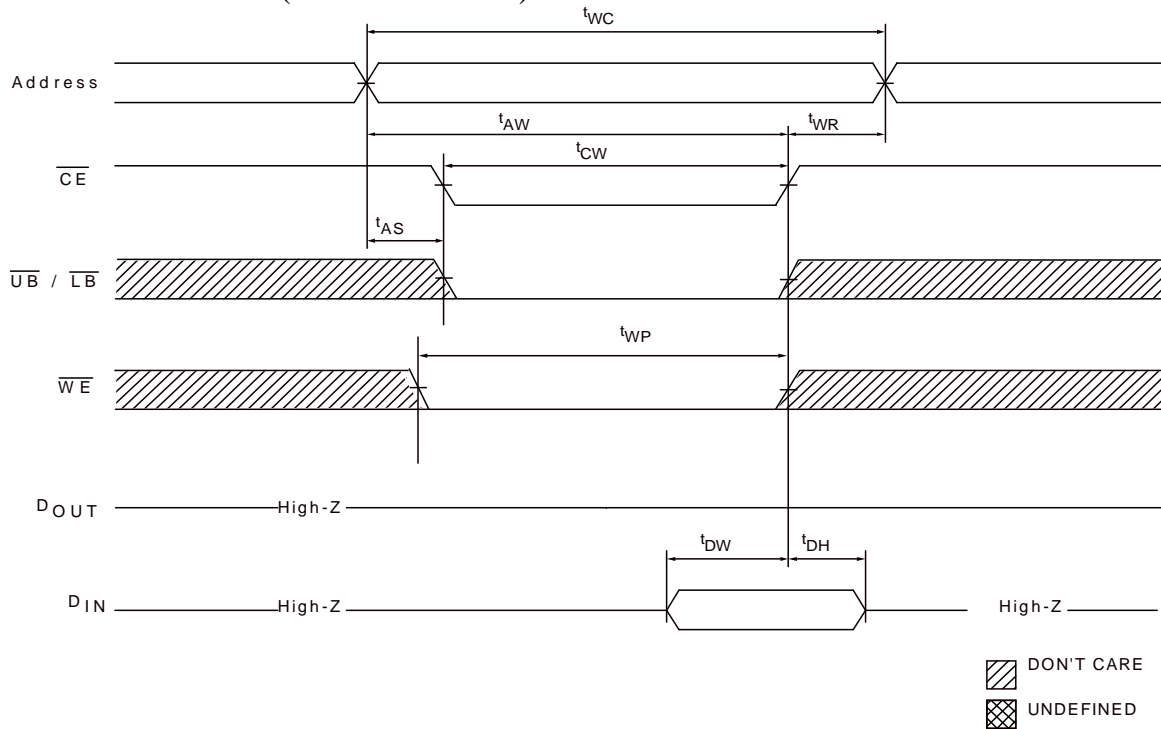
Notes (READ CYCLE) :

1.  $\overline{WE}$  are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition.  $t_{HZ}$  (max.) is less than  $t_{LZ}$  (min.) both for a given device and from device to device interconnection.
5. Transition is measured  $\pm 200mV$  from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CE} = V_{IL}$ .

**WRITE CYCLE 1 ( $\overline{WE}$  Controlled)**

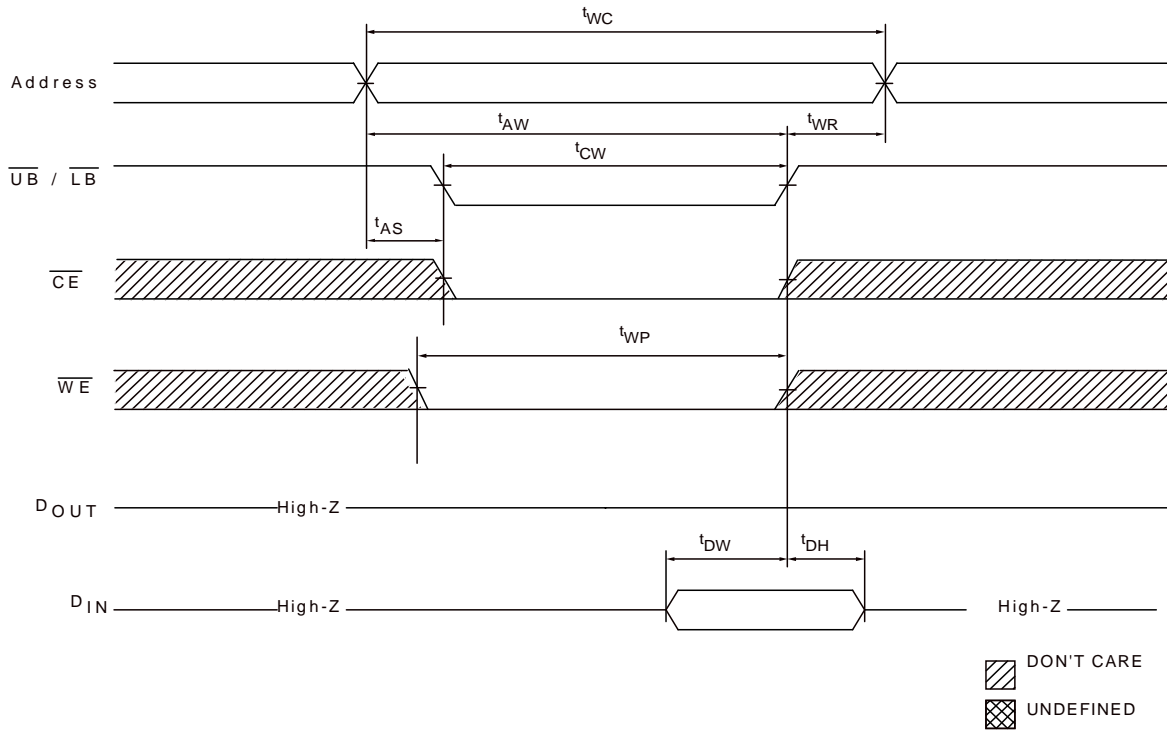


**WRITE CYCLE 2 ( $\overline{CE}$  Controlled)**





**WRITE CYCLE 3 (UB, LB Controlled)**



**NOTES ( WRITE CYCLE ) :**

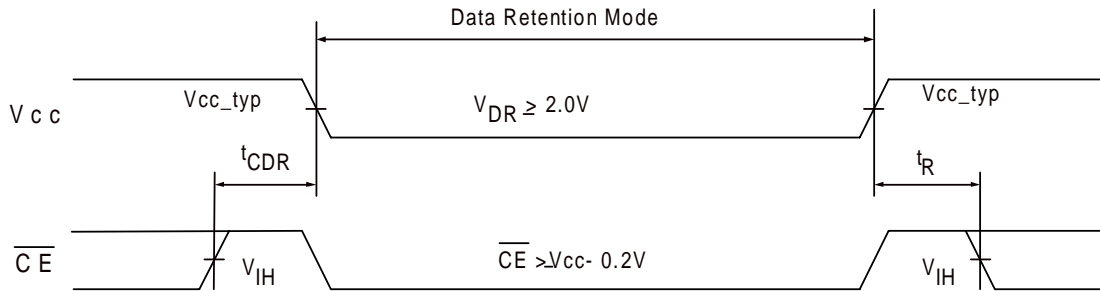
1. A write occurs during the overlap of a low  $\overline{CE}$ , a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE}$  going low,  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CE}$  going high,  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CE}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.

**DATA RETENTION CHARACTERISTICS**

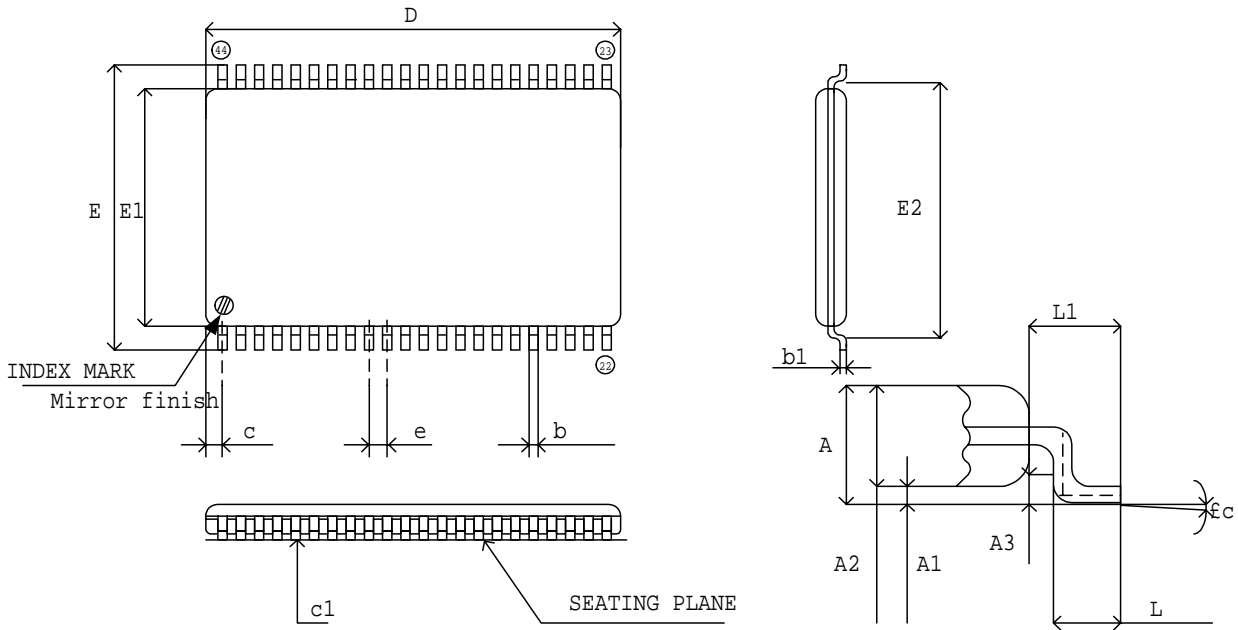
PARAMETER	SYM.	TEST CONDITION	MIN.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	-	V
Data Retention Current	I <sub>CCDR</sub>	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	300	uA
Chip Deselect to Data Retention Time	t <sub>CDR</sub>		0	-	ns
Operation Recovery Time	t <sub>R</sub>		t <sub>RC</sub>	-	ns

**DATA RETENTION WAVEFORM**

( Ta = 0 ~ +70 °C )



**PACKAGE DIMENSIONS**  
**44-LEAD TSOP-II**



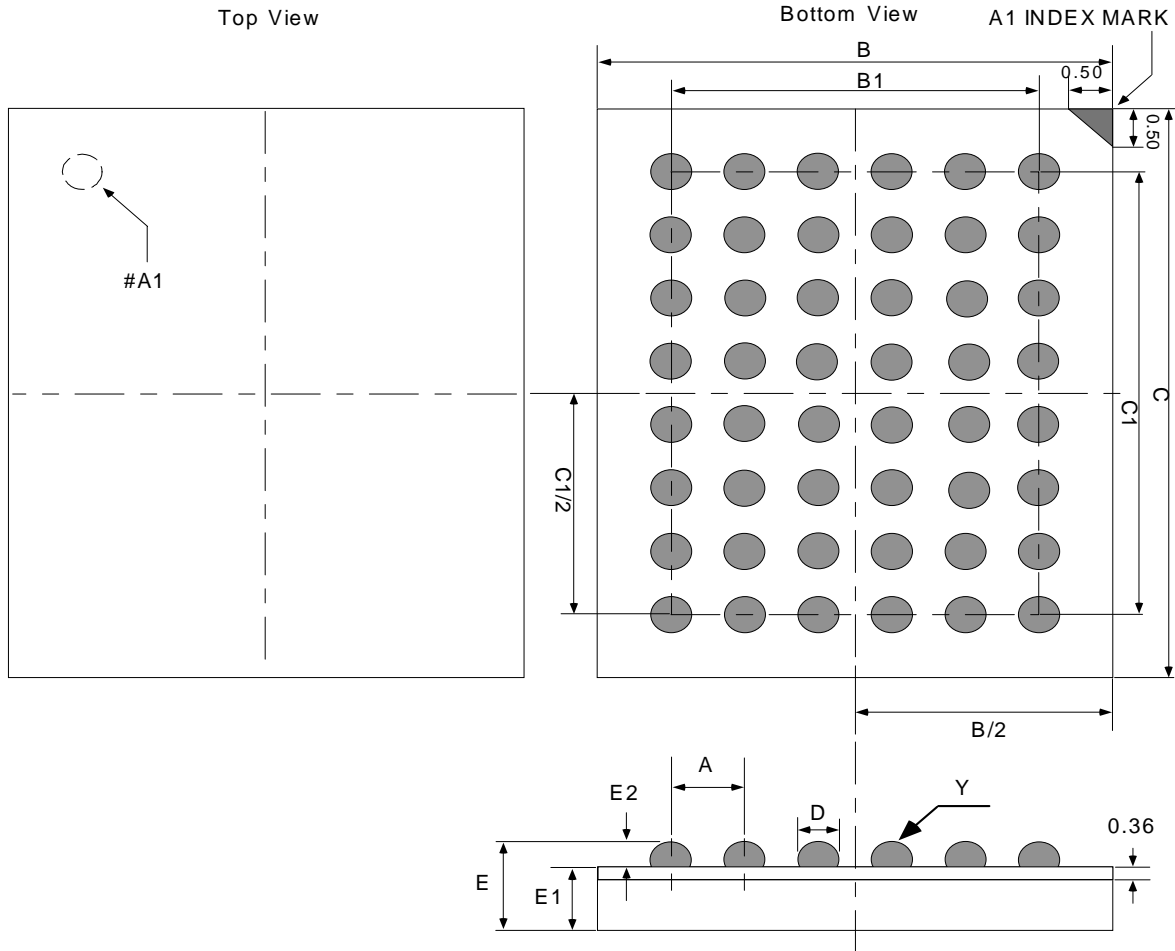
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.1	0.002	-	0.004
A2	0.95	1.00	1.05	0.037	0.039	0.041
A3	-	0.25	-	-	0.010	-
b	-	0.35(typ)	-	-	0.014(typ)	-
b1	0.10	0.15	0.25	0.004	0.006	0.010
c	-	0.805	-	-	0.032	-
c1	-	0.10	-	-	0.004	-
D	18.31	18.41	18.51	0.721	0.725	0.729
e	-	0.80(typ)	-	-	0.031(typ)	-
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
E2	-	10.76	-	-	0.458	-
L	0.4	0.5	0.6	0.016	0.020	0.024
L1	-	0.8(typ)	-	-	0.032(typ)	-
θ	0	-	8	0	-	8

**PACKAGE DIMENSIONS**

Units : millimeters

**48-pin CSP (8 row x 6 column)**

**48 BALL FINE PITCH BGA (0.75mm ball pitch)**



Symbol	min	typ	max
<b>A</b>	-	0.75	-
<b>B</b>	5.95	6.00	6.05
<b>B1</b>	-	3.75	-
<b>C</b>	7.95	8.00	8.05
<b>C1</b>	-	5.25	-
<b>D</b>	0.25	0.30	0.35
<b>E</b>	-	1.10	1.20
<b>E1</b>	-	0.95	-
<b>E2</b>	0.20	0.25	0.30
<b>Y</b>	-	-	0.08

Notes :

1. Bump counts : 48 (8 row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75) typ.
3. All tolerance are ±0.050 unless otherwise specified.
4. 'Y' is coplanarity : 0.08(max)
5. Units : mm