SaRonix

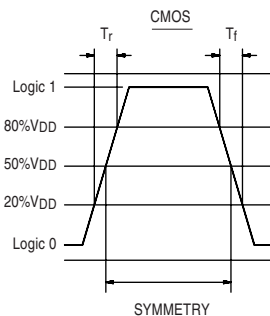## Voltage Controlled Crystal Oscillator   3.3V, LVCMOS

Technical Data

ACTUAL SIZE

Description

A 3.3V, voltage controlled oscillator with output logic levels compatible with LVCMOS and LVTTL logic families. The series is designed with excellent Jitter characteristics which makes it ideal for use in Telecom and Datacom applications. True SMD DIL versions for IR reflow are available, select option "S" in part number builder. See separate data sheet for SMD package dimensions.

Applications & Features

- Phase-Locked Loop (PLL) Clock and Data Recovery, Frequency Transaltion, Frequency Synthesis apps in Video, Video Compression, Telephony, and LAN/WAN Data Communication
- 3.3 Volt operations
- LVCMOS / LVTTL compatible
- 3.5ps max RMS period jitter
- Wide range of performance options:
  ±50 to ±100 ppm APR*
  ±20 to ±50 ppm Frequency Stability
- Tri-State option
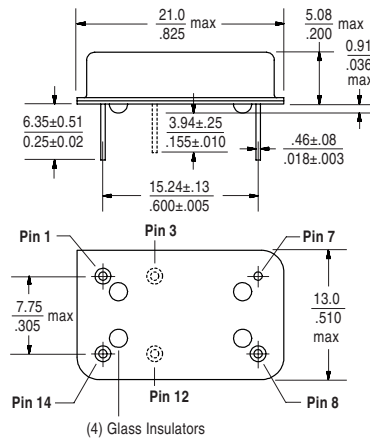- True SMD for IR reflow available

Output Waveform

Frequency Range:	1.5 MHz to 28.6363 MHz	
Frequency Stability:	±20, ±25 or ±50ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, shock and vibration, with V_C = 1.65V	
Aging @ 25°C:	± 3ppm max per year, ±10ppm max for 10 years	
Temperature Range:		
Operating:	0 to +70°C or -40 to +85°C	
Storage:	-55 to +125°C	
Supply Voltage:		
Recommended Operating:	3.3V ±10%	
Supply Current:	10mA typ, 15mA max	
Output Drive:		
Symmetry:	45/55% max @ 50% V_{DD}	
Rise & Fall Times:	9ns max 20% to 80% V_{DD}	
Logic 0:	10% V_{DD} max	
Logic 1:	90% V_{DD} min	
Load:	30pF	
Jitter:	3.5ps max RMS period jitter	

Pull Characteristics:

Input Impedance (pin 1):	50KΩ min
Frequency Response (-3dB):	10 kHz min
Pullability:	±50, ±70, ±100ppm APR* min
Control Voltage:	0.3 to 3.0V
Transfer Function:	Frequency Increases when Control Voltage Increases
Linearity:	5 or 10% max
Center Control Voltage:	1.65V

Mechanical:

Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Condition B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Conditions A, B or C (I or J for Gull Wing)

Environmental:

Gross Leak Test:	MIL-STD-883C, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883C, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883C, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883C, Method 1004

* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability)
NOTE: APR is inclusive of 10 Years Aging

DS-126   REV E

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www.pericom.com/saronix

Package Details

21.0 max / .825 max

5.08 max / .200 max

0.91 / .036 max

6.35±0.51 / 0.25±0.02

3.94±.25 / .155±.010

.46±.08 / .018±.003

15.24±.13 / .600±.005

Pin 1   Pin 3   Pin 7

7.75 / .305 max

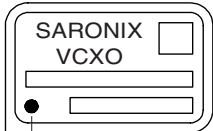13.0 / .510 max

Pin 14   Pin 12   Pin 8

(4) Glass Insulators

Pin Function:

Pin 1: Control Voltage
Pin 3: Tri-State control (optional)
Pin 7: GND/Case (V$_{SS}$)

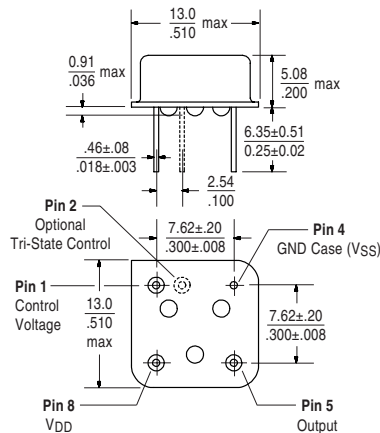Pin 8: OUTPUT
Pin 12: N/C (optional)
Pin 14: +3.3VDC (V$_{DD}$)

Marking Format**
Includes Date Code, Frequency & Part Number

SARONIX
VCXO

Denotes Pin 1

HALF SIZE PACKAGE

13.0 / .510 max

0.91 / .036 max

5.08 / .200 max

.46±.08 / .018±.003

6.35±0.51 / 0.25±0.02

2.54 / .100

Pin 2
Optional
Tri-State Control

7.62±.20 / .300±.008

Pin 4
GND Case (V$_{SS}$)

Pin 1
Control
Voltage

13.0 / .510 max

7.62±.20 / .300±.008

Pin 8
V$_{DD}$

Pin 5
Output

Marking Format**
Includes Date Code, Frequency & Part Number

SARONIX
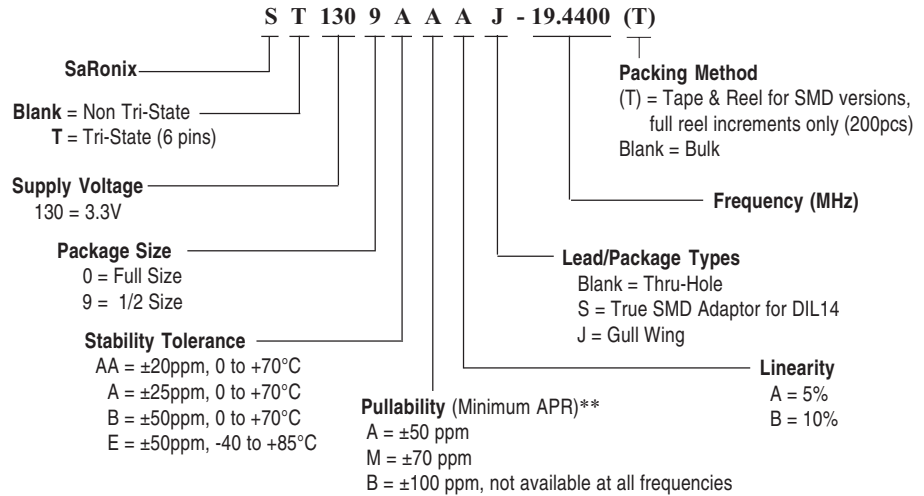
Denotes Pin 1

**Exact location of items may vary

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

S T 130 9 A A A J - 19.4400 (T)

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Blank = Non Tri-State
T = Tri-State (6 pins)

Supply Voltage
130 = 3.3V

Package Size
0 = Full Size
9 = 1/2 Size

Stability Tolerance
AA = ±20ppm, 0 to +70°C
A = ±25ppm, 0 to +70°C
B = ±50ppm, 0 to +70°C
E = ±50ppm, -40 to +85°C

Pullability (Minimum APR)**
A = ±50 ppm
M = ±70 ppm
B = ±100 ppm, not available at all frequencies

Lead/Package Types
Blank = Thru-Hole
S = True SMD Adaptor for DIL14
J = Gull Wing

Packing Method
(T) = Tape & Reel for SMD versions,
full reel increments only (200pcs)
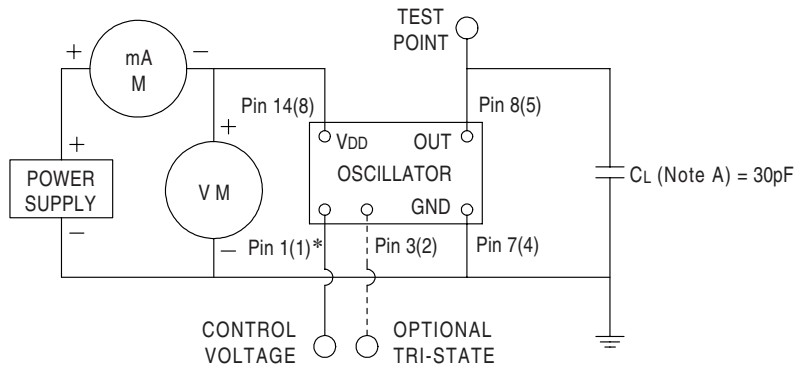Blank = Bulk

Frequency (MHz)

Linearity
A = 5%
B = 10%

** APR = (VCXO Pull relative to specified Output Frequency) − (VCXO Frequency Stability)
NOTE: APR is inclusive of 10 Years Aging

Tri-State Logic Table

Pin 3(2) Input	Pin 8(5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 3(2):
Logic 1 = 0.7 V$_{DD}$ min
Logic 0 = 0.3 V$_{DD}$ max

Test Circuit

TEST POINT

mA
M

Pin 14(8)   Pin 8(5)

POWER SUPPLY

V M

VDD   OUT
OSCILLATOR
GND

C$_L$ (Note A) = 30pF

Pin 1(1)*   Pin 3(2)   Pin 7(4)

CONTROL VOLTAGE   OPTIONAL TRI-STATE

NOTE A: C$_L$ includes probe and fixture capacitance
* Items in brackets( ) represent Half Size model

All specifications are subject to change without notice.

DS-126   REV E

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True SMD Adaptor

Technical Data

RECOMMENDED LAND PATTERN