

ST2221A

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8-Bit CONSTANT CURRENT LED DRIVERS



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8-Bit CONSTANT CURRENT LED DRIVERS

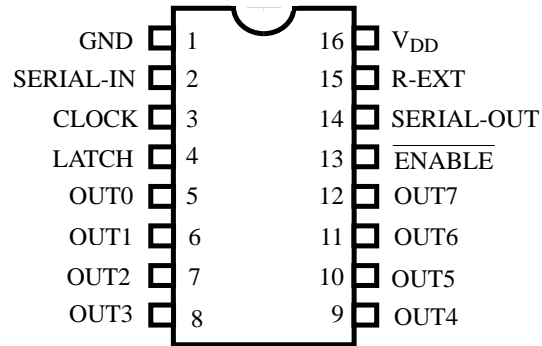
General Description

The ST2221A is specifically designed for LED and LED DISPLAY constant current drivers. The value of constant current can be varied using an external resistor ($I_{out} = 5 \sim 90\text{mA}$). The devices include an 8-bit shift registers, latches, and constant current drivers on a single Silicon CMOS chip.

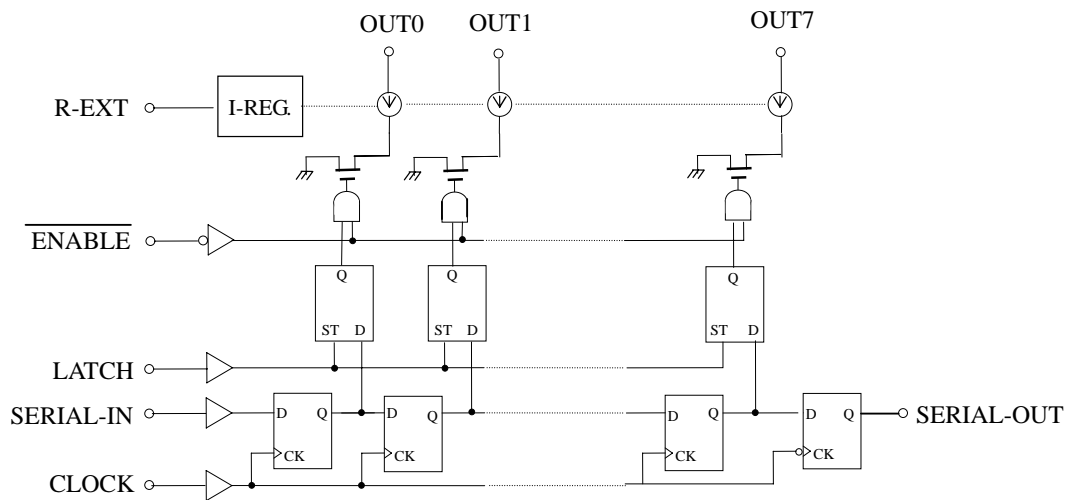
Features

- Constant Current Output : Current with one resistor for 5mA to 90mA
- Maximum Clock Frequency : 25MHz (Cascade Operation)
- 5V CMOS Compatible Input
- Package : PDIP16,SOP16,SSOP16
- Constant Current Matching: ($T_a = 25^\circ\text{C}$ 、 $V_{DD} = 5.0\text{V}$)
 - Bit-to-Bit : $\pm 6\%$ 、Chip-to-Chip : $\pm 10\%$ 、
@ $I_{OUT} = 5 \sim 40\text{mA}$
 - Bit-to-Bit : $\pm 6\%$ 、Chip-to-Chip : $\pm 10\%$ 、
@ $I_{OUT} = 40 \sim 90\text{mA}$

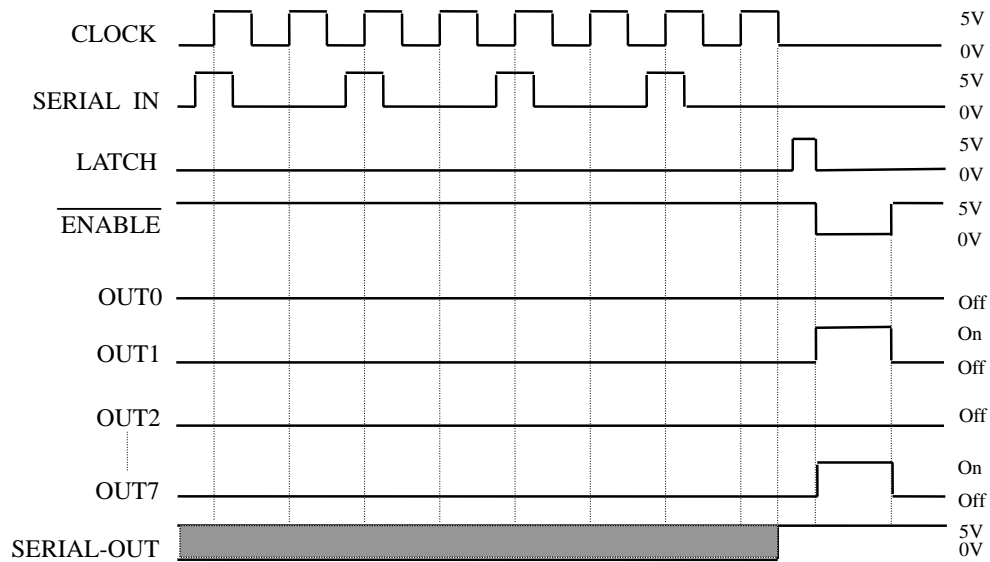
Pin Connection (Top view)



Block Diagram



Timing Diagram



(Note) Latches are level sensitive (not edge triggered).

LATCH-terminal = H level, latches become transparent; LATCH-terminal = L level, latches hold data.

ENABLE-terminal = H level, all outputs (OUT0~7) are off.

An external resistor is connected between R-EXT and GND for setting up the value of constant current.

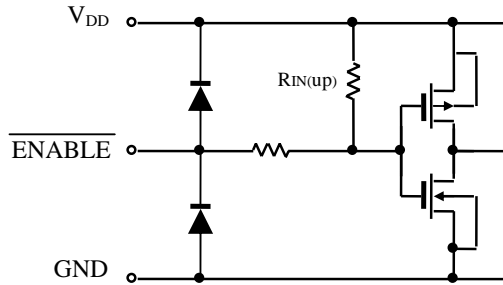
SERIAL-OUT changes state on the falling edges of clock.

Pin Description

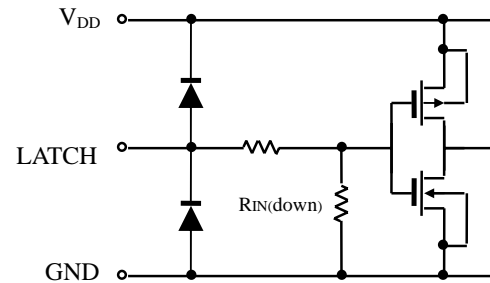
PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal
2	SERIAL-IN	Input terminal of a data shift register
3	CLOCK	Input terminal of a clock for shift register
4	LATCH	Input terminal for data strobe
5~12	OUT0~7	Output terminals
13	$\overline{\text{ENABLE}}$	Input terminal for output enable (active low)
14	SERIAL-OUT	Output terminal of a data shift register
15	R-EXT	Input terminal of an external resistor
16	V _{DD}	5V Supply voltage terminal

Equivalent Circuit of Inputs and Outputs

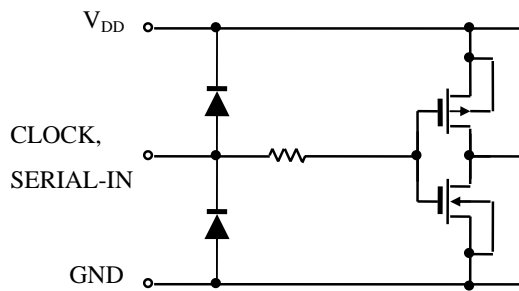
1. $\overline{\text{ENABLE}}$ terminal



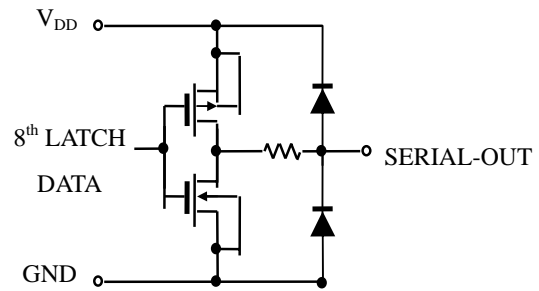
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



Maximum Ratings (Ta=25°C, Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0 ~ 7.0	V
Input Voltage	VIN	-0.4 ~ VDD+0.4	V
Output Current	IOUT	90	mA
Output Voltage	VOUT	-0.5 ~ 9.5	V
Clock Frequency	fCLK	25	MHz
GND Terminal Current	IGND	720	mA
Power Dissipation	PD	1.35 (PDIP-16 : Ta=25°C)	W
		1.03 (SOP-16 : Ta=25°C)	
		0.99 (SSOP-16 : Ta=25°C)	
Thermal Resistance	Rth(j-a)	85 (PDIP-16)	°C/W
		110.9 (SOP-16)	
		115.9 (SSOP-16)	
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	4.5	5.0	5.5	V
Output Voltage	VOUT	—	—	—	9	V
Operating temperature	T _{OPR}	—	-40	—	85	°C
Output Current	I _O	OUT _n	5	—	88	mA
	I _{OH}	SERIAL-OUT	—	—	1.0	
	I _{OL}	SERIAL-OUT	—	—	-1.0	
Input Voltage	V _{IH}	—	0.7VDD	—	VDD+0.3	V
	V _{IL}	—	-0.3	—	0.3VDD	
LATCH Pulse Width	tw _{LAT}	VDD = 4.5 ~ 5.5 V	15	—	—	ns
CLOCK Pulse Width	tw _{CLK}		15	—	—	ns
Set-up Time for DATA	t _{setup(D)}		20	—	—	ns
Hold Time for DATA	t _{hold(D)}		20	—	—	ns
Set-up Time for LATCH	t _{setup(L)}		15	—	—	ns
Clock Frequency	fCLK	Cascade operation	—	—	25	MHz
Power Dissipation	PD	Ta = 85°C(PDIP-16)	—	—	0.41	W
		Ta = 85°C(SOP-16)	—	—	0.32	
		Ta = 85°C(SSOP-16)	—	—	0.30	

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	V _{IH}	—	0.7VDD	—	VDD	V
Input Voltage "L" Level	V _{IL}	—	GND	—	0.3VDD	
Output Leakage Current	I _{OH}	VOH = 7.5 V	—	—	1.0	μA
Output Voltage (S - OUT)	V _{OL}	I _{OL} = 1.0 mA	—	—	0.4	V
	V _{OH}	I _{OH} = -1.0 mA	4.6	—	—	
Output Current (Bit-Bit)	I _{OL1}	V _{OUT} = 0.7±0.25V R _{EXT} = 910Ω	—	3	6	%
	I _{OL2}	V _{OUT} = 0.7±0.25V R _{EXT} = 360Ω	—	3	6	%
Output Current (Chip-Chip)	I _{OL3}	V _{OUT} = 0.7V R _{EXT} = 910Ω	—	5	10	%
	I _{OL4}	V _{OUT} = 0.7V R _{EXT} = 360Ω	—	5	10	%
Supply Voltage Regulation	% / VDD	R _{EXT} = 470Ω, Ta = -40 ~ 85°C	—	1.5	5.0	% / V
Pull-Up Resistor	R _{IN(up)}	—	150	300	600	KΩ
Pull-Down Resistor	R _{IN(down)}	—	100	200	400	KΩ
Supply Current "OFF"	IDD(off)1	R _{EXT} = OPEN, OUT0~7 = off	—	0.3	0.6	mA
	IDD(off)2	R _{EXT} = 470Ω, OUT0~7 = off	4.0	5.6	7.8	
	IDD(off)3	R _{EXT} = 250Ω, OUT0~7 = off	7.3	10.2	14.3	
Supply Current "ON"	IDD(on)1	R _{EXT} = 470Ω, OUT0~7 = on	4.0	5.6	7.8	
	IDD(on)2	R _{EXT} = 250Ω, OUT0~7 = on	7.3	10.2	14.3	

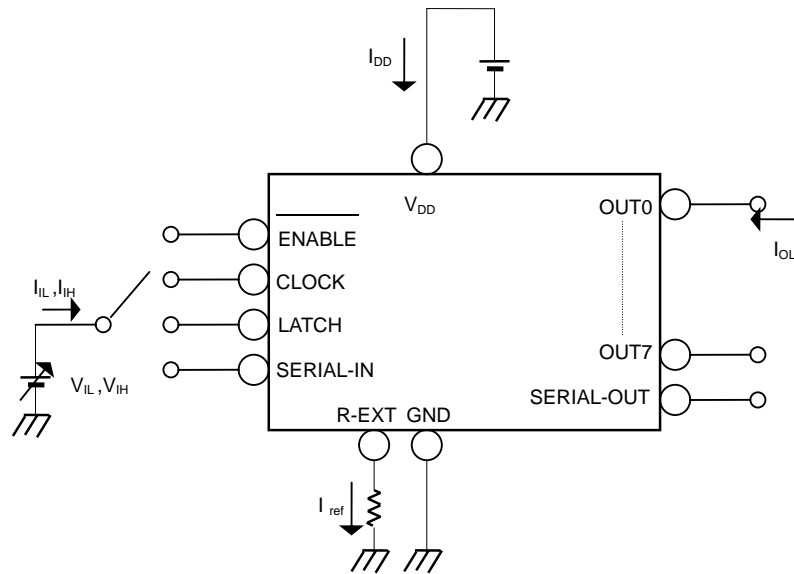
Switching Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	SIN-OUT _n	V _{DD} =5.0V V _{IH} =VDD V _{IL} =GND R _{EXT} =470Ω ¹ V _L =3.0V	—	115	230	ns
	LATCH-OUT _n		—	115	230	
	ENABLE-OUT _n		—	115	230	
	CLK-SOUT		—	15	20	
Propagation Delay Time ("H" to "L")	SIN-OUT _n	R _L =65Ω C _L =13pF	—	120	160	ns
	LATCH-OUT _n		—	120	160	
	ENABLE-OUT _n		—	120	160	
	CLK-SOUT		—	15	20	
Output Current Rise Time	t _{or}		70	140	280	ns
Output Current Fall Time	t _{of}		55	110	220	ns

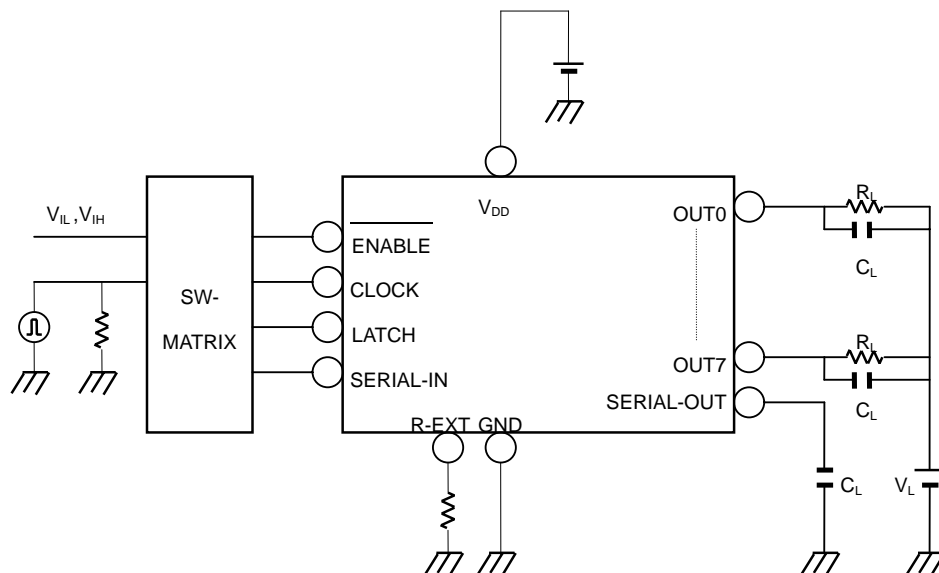
¹ Delay Time t_{plH} and Rise Time t_{or} will both increase as the R_{ext} value increased.

Test Circuit

DC characteristic

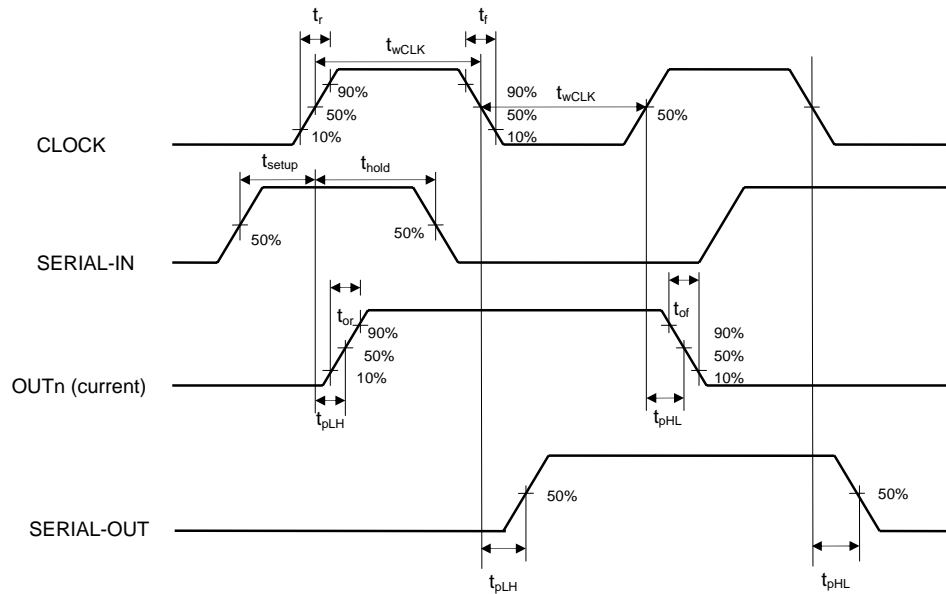


AC characteristic

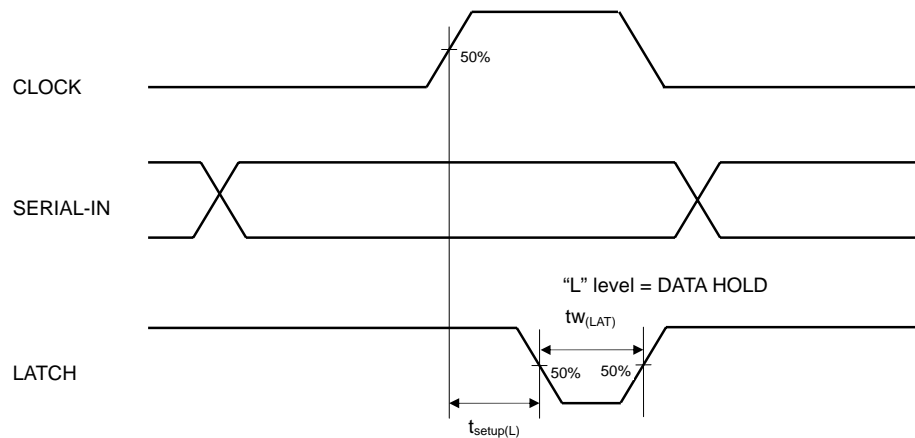


Timing Diagram

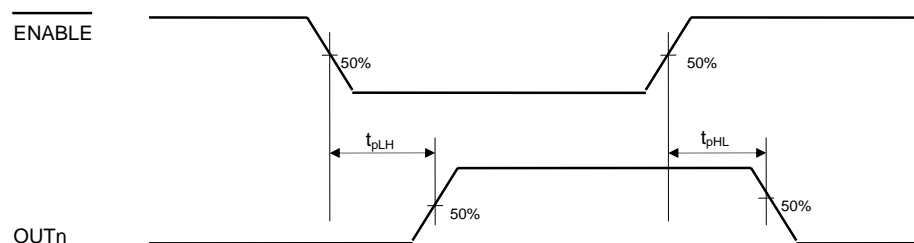
1. CLOCK-SERIAL OUT, OUTn

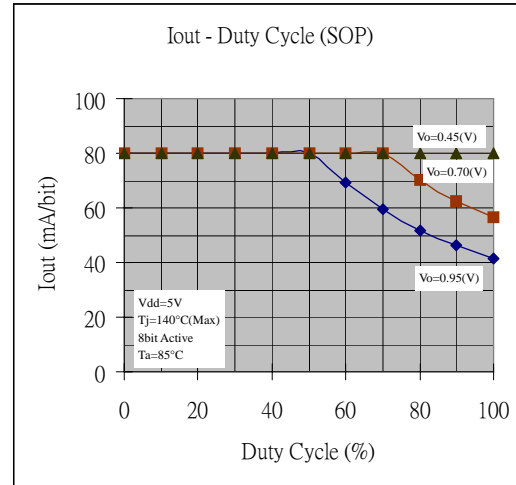
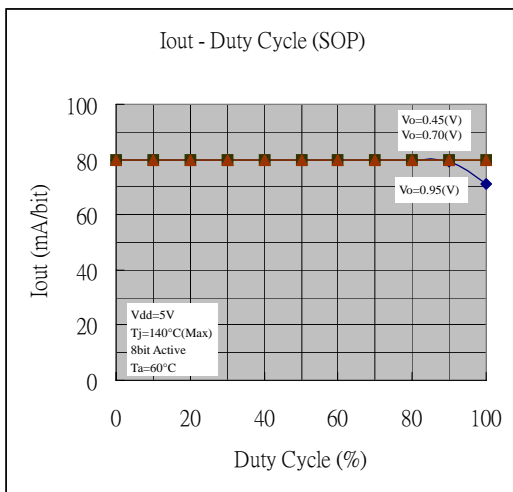
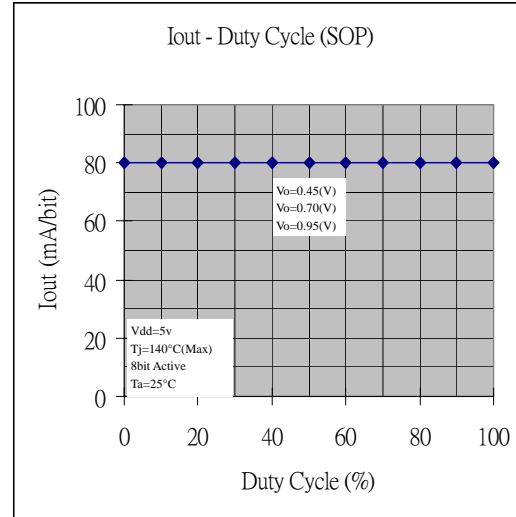
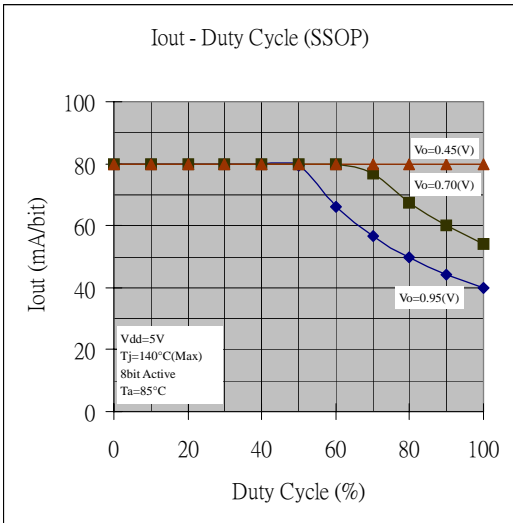
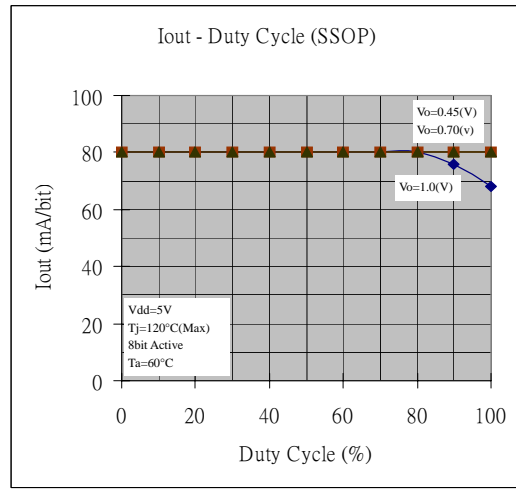
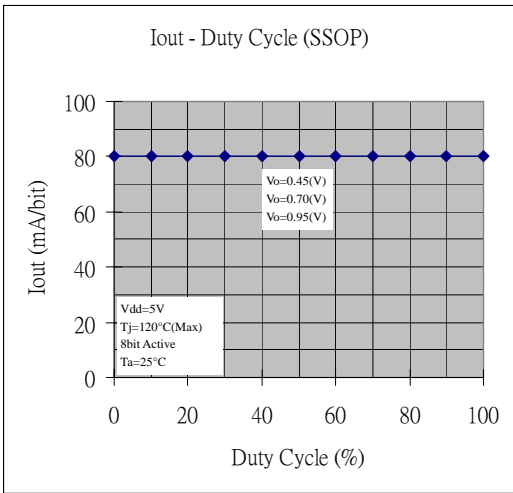


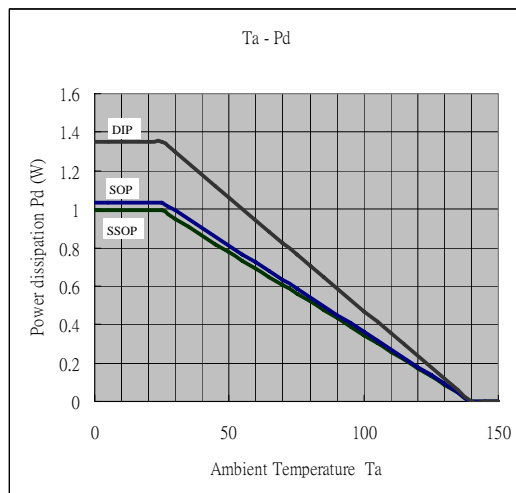
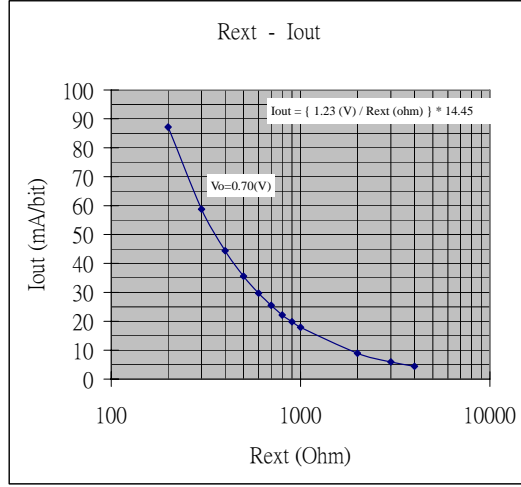
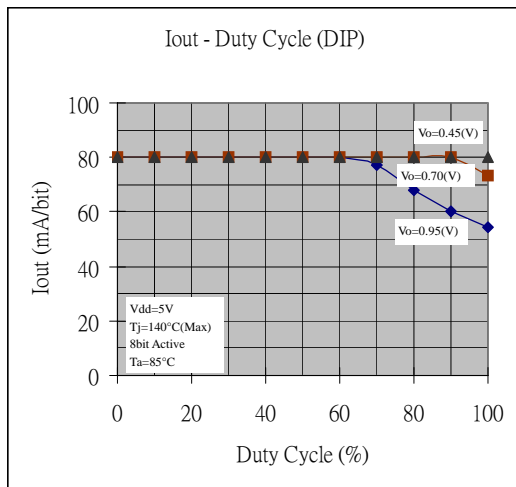
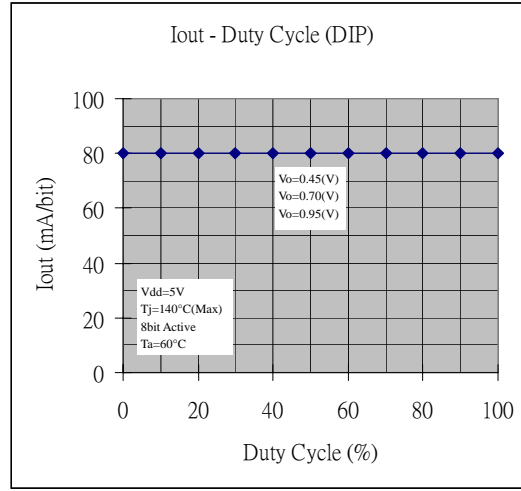
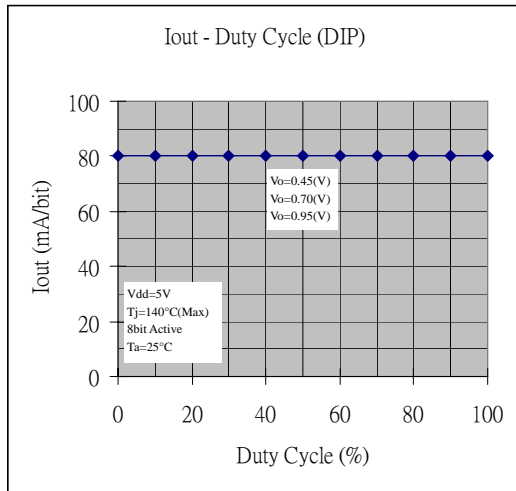
2. CLOCK-LATCH

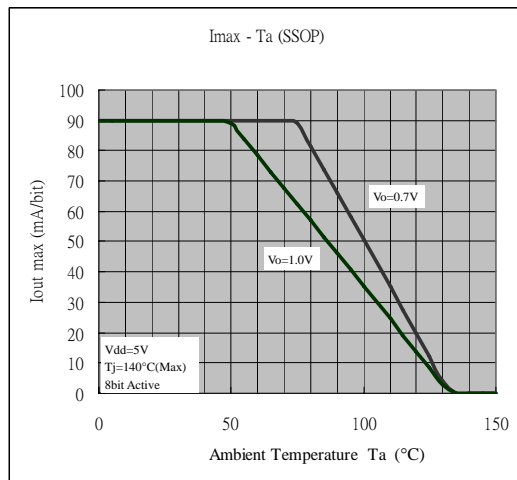
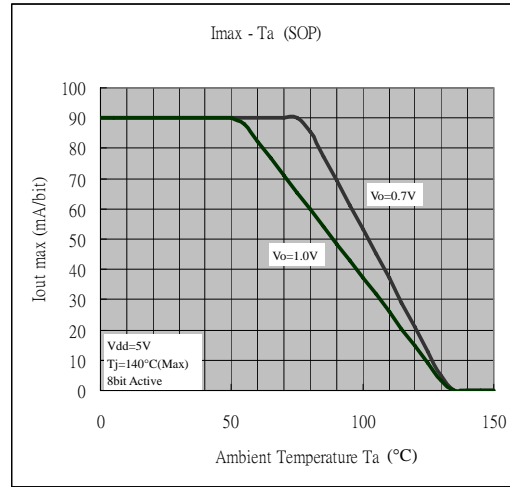
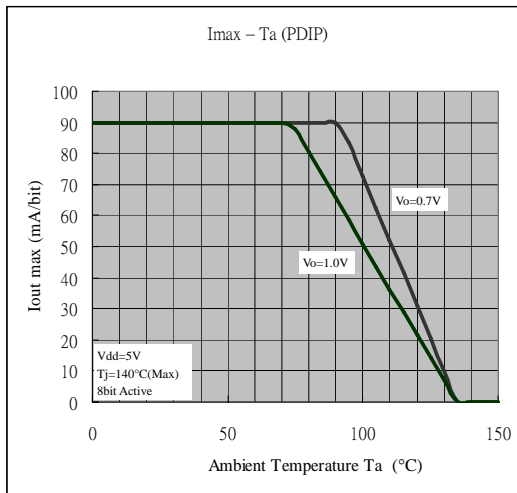


3. $\overline{\text{ENABLE}}$ -OUTn









Note

As the power dissipation of a semiconductor chip is limited its package and ambient temperature, this device requires a maximum output current be calculated for a given operating condition. The maximum allowable power consumption (Pd (max)) of this device is calculated as follows:

$$Pd(max)(Watt) = \frac{(Tj(\text{junction temperature})(max) - Ta(\text{ambient temperature}))(\text{°C})}{Rth(\text{°C/Watt})}$$

Based on the Pd (max), the maximum allowable current can be calculated as follows:

$$Iout = (Pd - V_{DD} \cdot I_{DD}) / (\# \text{ outputs} \cdot Vo \cdot \text{Duty})$$

System Configuration Example

[1] Output current (I_{OUT})

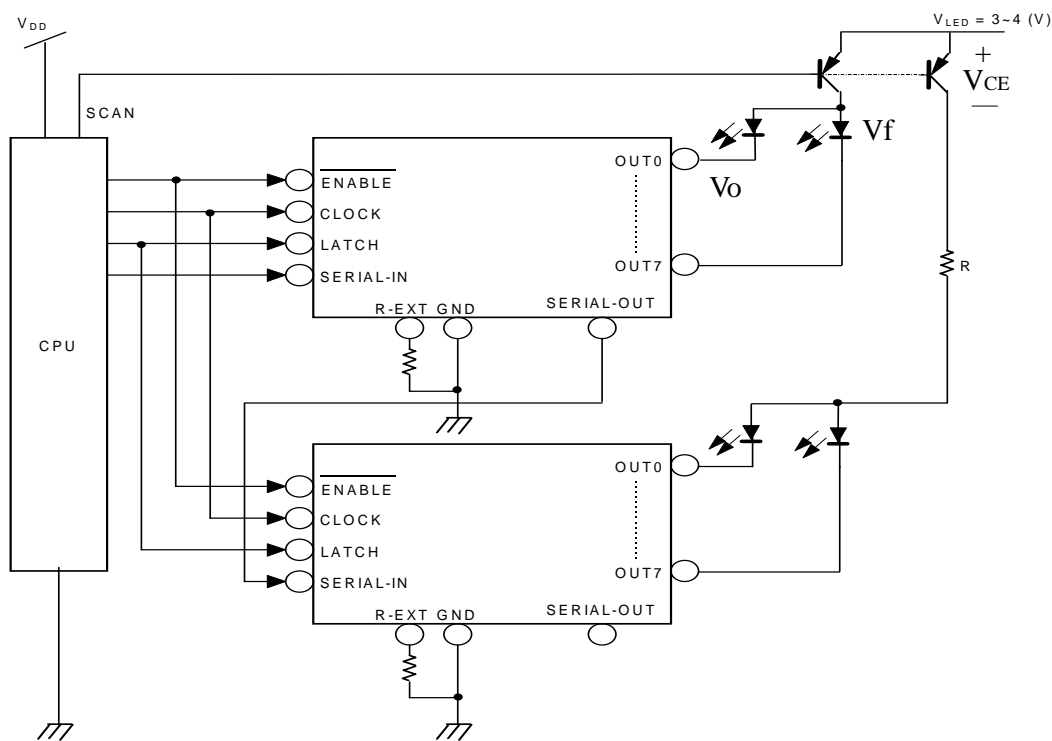
Sink current is set by the external resistor as shown in figure (I_{out} vs. R_{ext}).

[2] LED supply voltage (V_{LED}) setup

$$V_{LED} = V_{CE} (T_r V_{sat}) + V_f (\text{LED forward voltage}) + V_O (\text{IC supply voltage})$$

To prevent too much power dissipated by the device due to higher V_{LED} , an additional R can be used to reduce the V_{out} when the outputs consume current:

$$R = \frac{V_{LED} - V_f - V_O(\min)}{I_o(\max) \bullet \text{Bit}(\max)}$$



Note

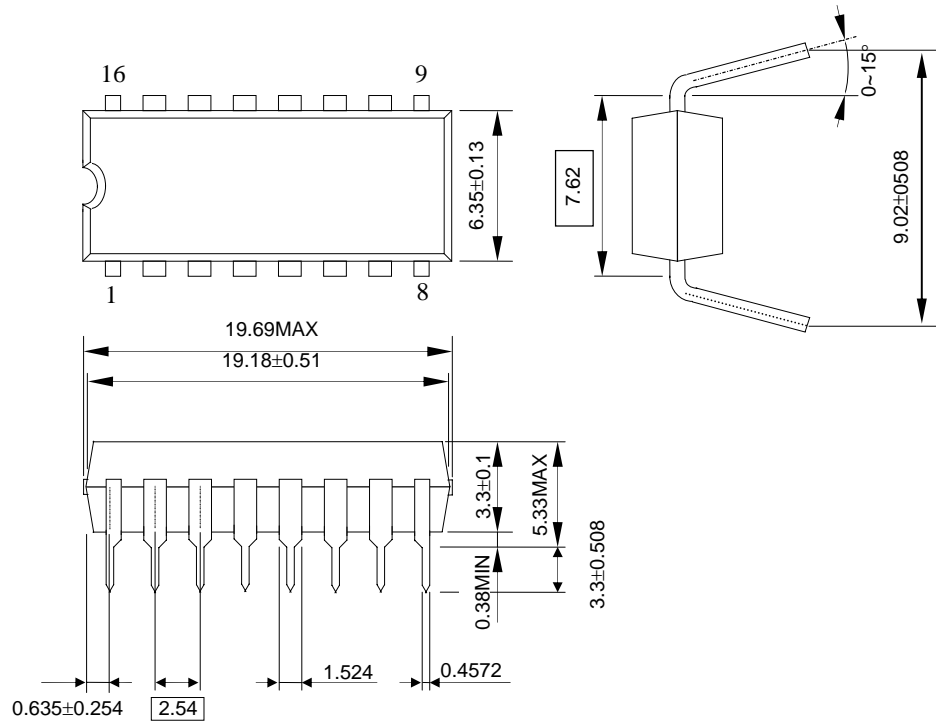
This device has only one ground pin shared by signal, output sink current, and power ground.

It is advisable to pattern the ground layout with minimized inductance such that the switching noise induced by the input signals and the output sink current would not cause chip malfunction. To prevent the drivers' outputs from damage by overshoot stress, it is also advisable not to turn off the drivers and scan transistors simultaneously.

Package Outline

PDIP16 (ST2221A-1)

Unit: mm

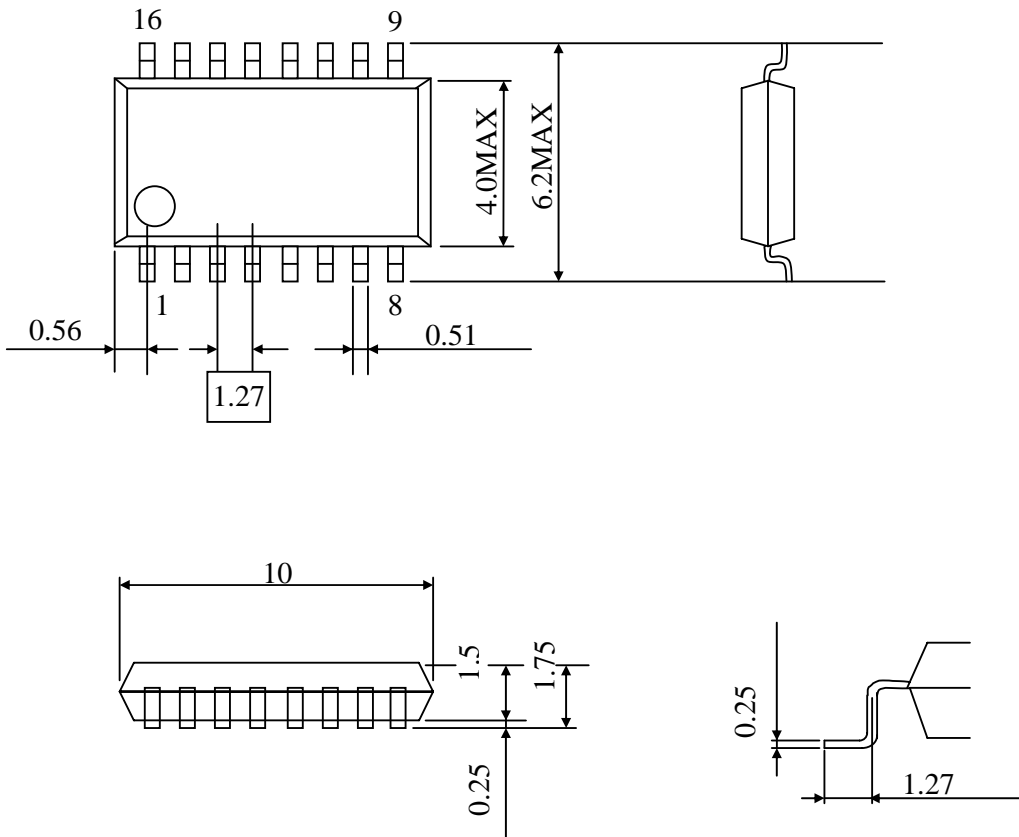


Weight : 1.11g(Typ.)

Package Outline

SOP16 (ST2221A-3)

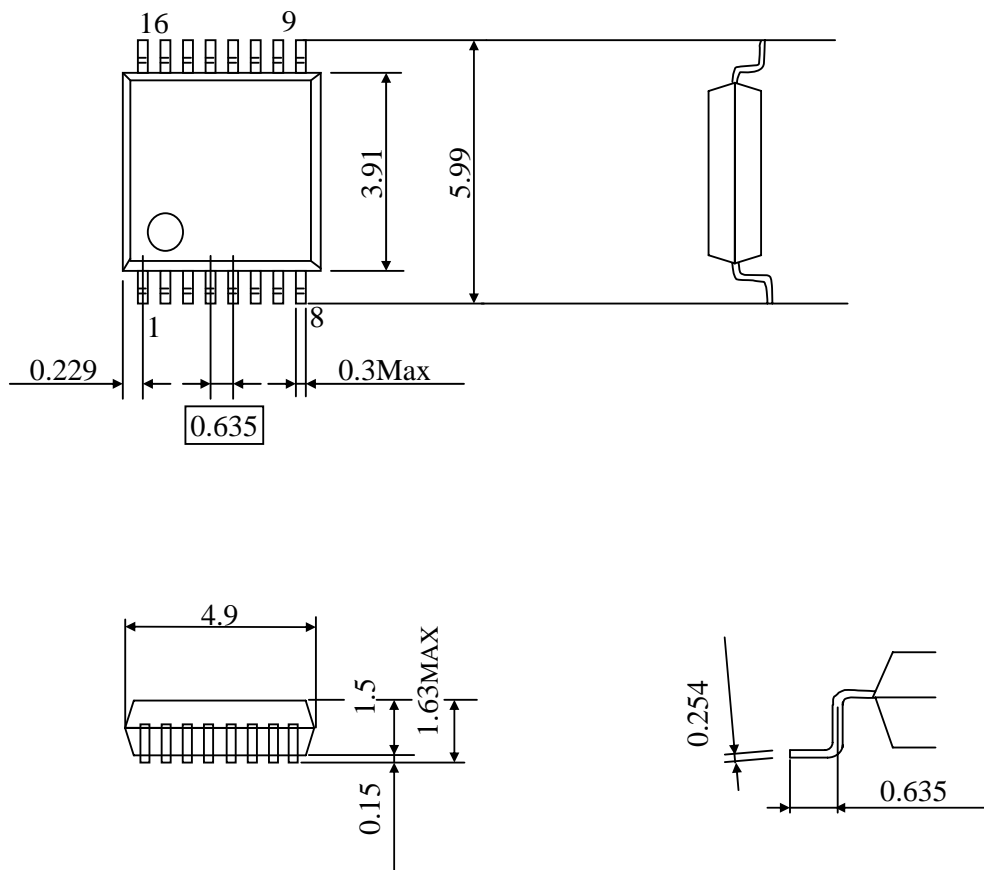
Unit: mm



Package Outline

SSOP16 (ST2221A-2)

Unit: mm





The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss. Silicon Touch Technology, Inc. will not take any responsibilities regarding the misuse of the products mentioned above. Anyone who purchases any products described herein with the above-mentioned intention or with such misused applications should accept full responsibility and indemnify. Silicon Touch Technology, Inc. and its distributors and all their officers and employees shall defend jointly and severally against any and all claims and litigation and all damages, cost and expenses associated with such intention and manipulation.