ST2301M

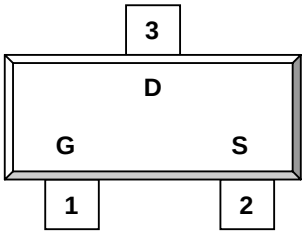
P Channel Enhancement Mode MOSFET

-3.0A

DESCRIPTION

The ST2301M is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

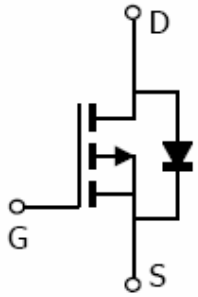
PIN CONFIGURATION
SOT-23



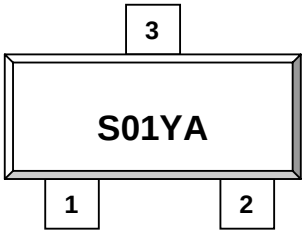
1.Gate 2.Source 3.Drain

FEATURE

- -20V/-2.8A, $R_{DS(ON)}$ = 130m-ohm (Typ.) @V_{GS} = -4.5V
- -20V/-2.0A, $R_{DS(ON)}$ = 220m-ohm @V_{GS} = -2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design



PART MARKING
SOT-23



Y: Year Code A: Process Code

ORDERING INFORMATION

Part Number	Package	Part Marking
ST2301MSRG	SOT-23	S01YA

※ Process Code : A ~ Z ; a ~ z
※ ST2301MSRG S : SOT-23 ; R : Tape Reel ; G : Pb – Free

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	-2.5 -1.5	A
Pulsed Drain Current		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)		I_S	-1.6	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS, I_D=-250uA	-0.48		-1.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	uA
		V_{DS}=-20V, V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V, V_{GS}=-4.5V V_{DS}≦-5V, V_{GS}=-2.5V	-6 -3			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-2.8A V_{GS}=-2.5V, I_D=-2.0A		0.135 0.220		Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_D=-2.8V		6.5		S
Diode Forward Voltage	V_{SD}	I_S=-1.6A, V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-6V V_{GS}=-4.5V I_D≡-2.8A		4.8	8	nC
Gate-Source Charge	Q_{gs}			0.75		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	V_{DS}=-6V V_{GS}=0V F=1MHz		35		pF
Output Capacitance	C_{oss}			150		
Reverse Transfer Capacitance	C_{rss}			60		
Turn-On Time	$t_{d(on)}$ tr	V_{DD}=-6V R_L=6Ω I_D=-1A V_{GEN}=-4.5V R_G=6Ω		10	20	nS
				32	45	
Turn-Off Time	$t_{d(off)}$ tf			38	55	
				30	50	

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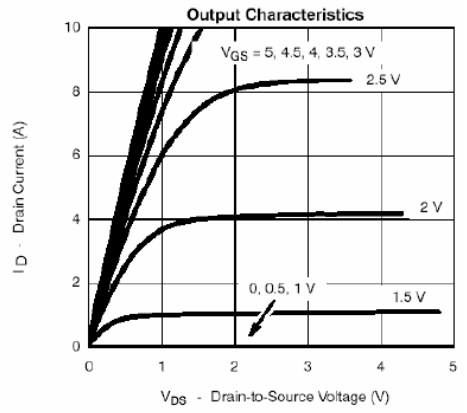
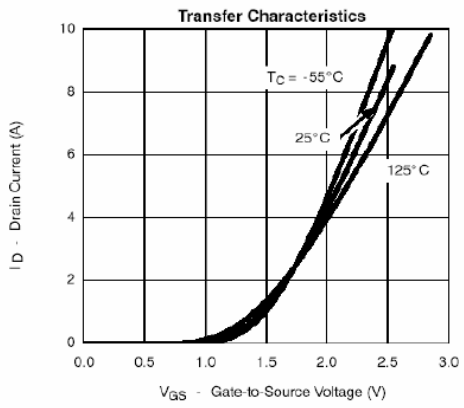
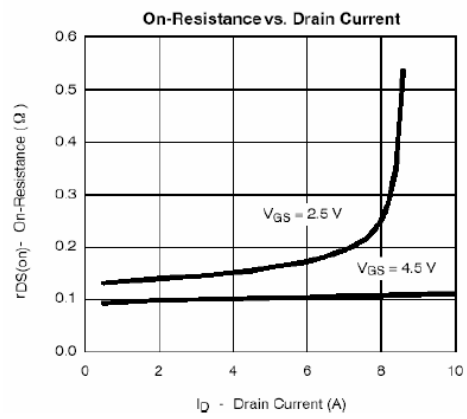
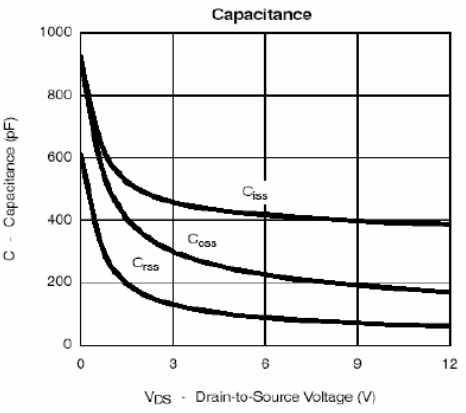
TYPICAL CHARACTERICTICS (25℃ Unless noted)









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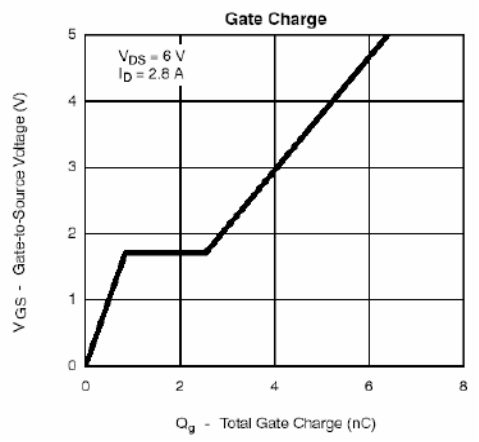

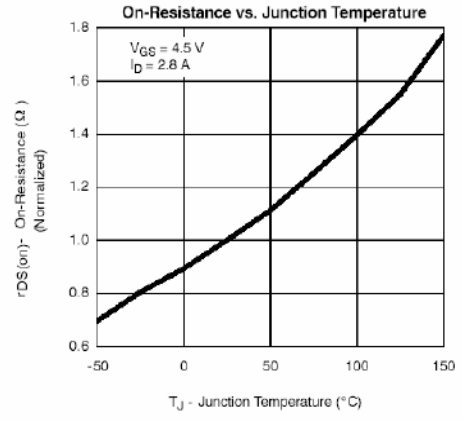

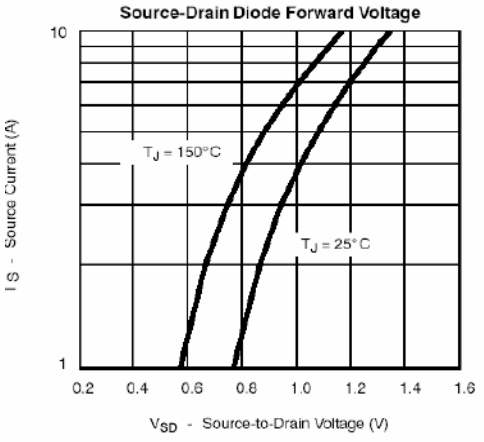

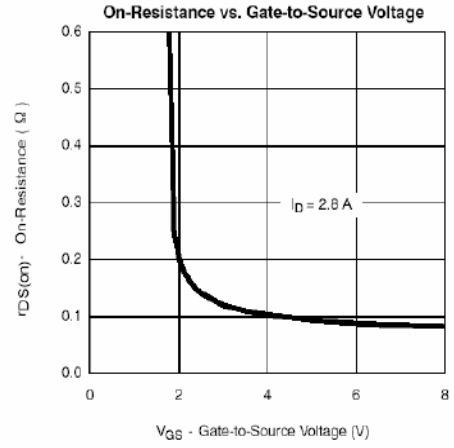

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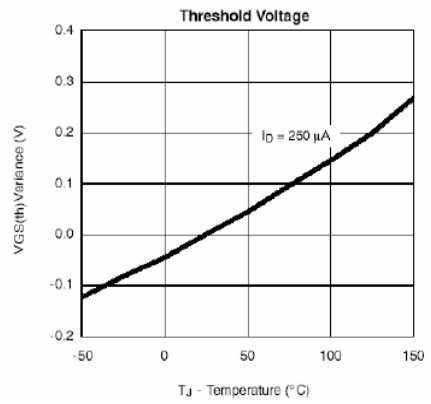

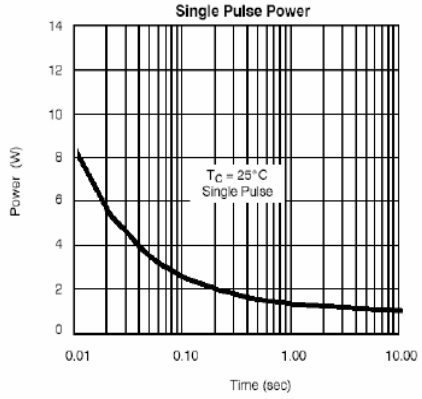

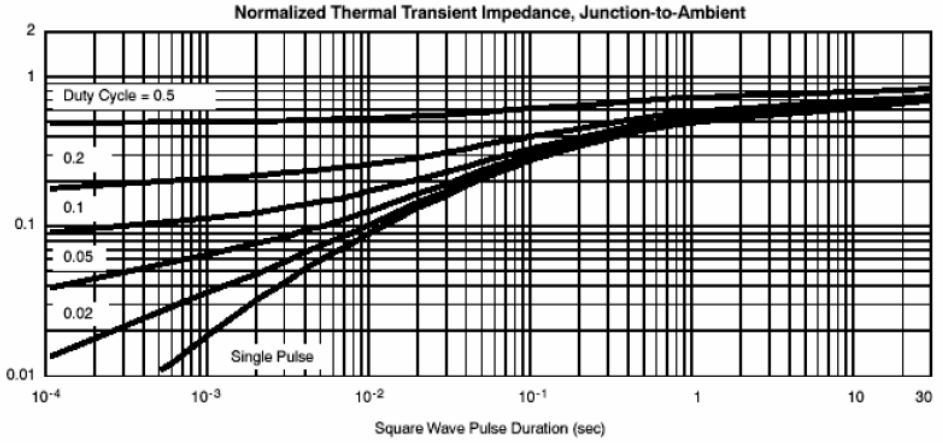

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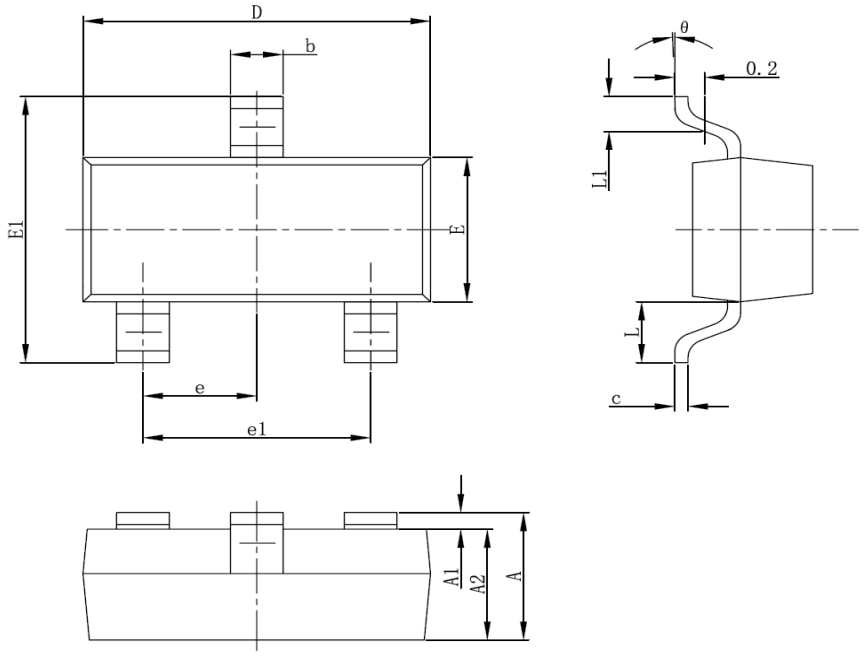
SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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