Ethernet Twisted Pair Transceiver

FEATURES

- Digital Implementation of IEEE 802.3 10BASE-T Media Attachment Unit (MAU).
- Synchronous design for embedded MAU applications.
- Digital Equalization Control for use with external summing resistors.
- Collision Detection of simultaneous transmit and receive packets.
- Smart Squelch requires at least two voltage threshold excursions to unsquelch. Squelches within 200 ns of last excursion.
- False Collision Protection provides additional squelch filtering during transmit to guard against impulse noise.
- Automatic AUI loopback mimics operation of coax MAU.
- Signal Quality Error (SQE) Test automatically tests collision detection circuitry by asserting a collision signal after every transmission.
- Jabber Timer provides a 26 ms timer for jabbering transmitter protection and a 0.42 second timer for self-healing after jabbering ends.
- Link Beat Test provides generation of link beat pulses and detection of link beat fail condition. A link fail status indicator is included.
- A select signal (SEL) allows the MAU to be disabled when integrated into a multiport repeater.
- Available in a 22-pin plastic DIP or a 28-pin PLCC.

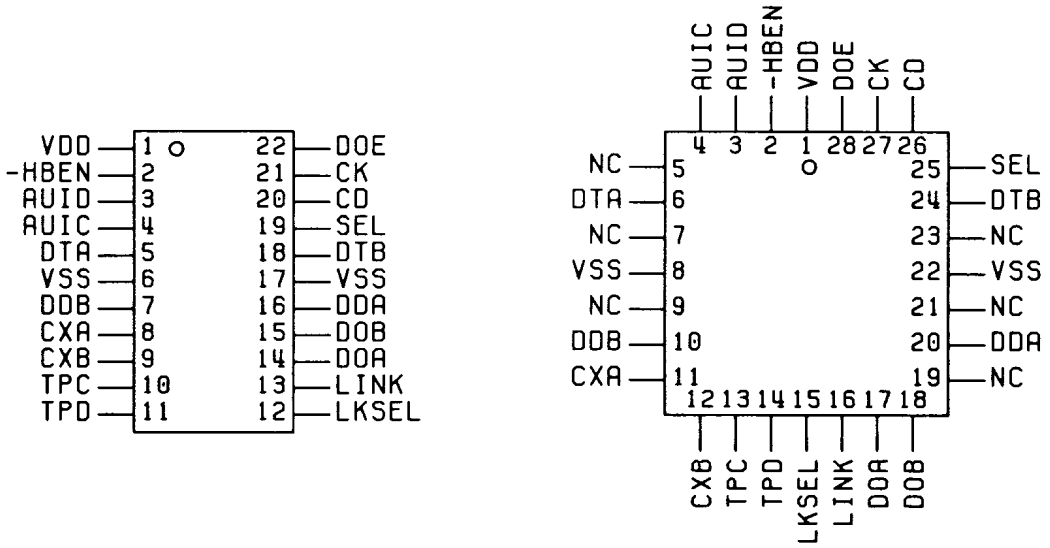


Figure 1 Pinout Diagrams

Signal Name	Type	Pin Number		Pin Description
		22-pin DIP	28-pin PLCC	
VDD	Power	1	1	Power
-HBEN	Input	2	2	SQE Test Disable
AUID	Input	3	3	AUI Data
AUIC	Input	4	4	AUI Carrier
NC		-	5	No Connect
DTA	Output	5	6	Data Transmit A
NC		-	7	No Connect
VSS	Ground	6	8	Ground
NC			9	No Connect
DDB	Output	7	10	Data Delayed B
CXA	Output	8	11	Collision A
CXB	Output	9	12	Collision B
TPC	Input	10	13	Twisted Pair Carrier
TPD	Input	11	14	Twisted Pair Data
LKSEL	Input	12	15	Link Select
LINK	Output	13	16	Link Status
DOA	Output	14	17	Data Out A
DOB	Output	15	18	Data Out B
NC		-	19	No Connect
DDA	Output	16	20	Data Delayed A
NC		-	21	No Connect
VSS		17	22	Ground
NC		-	23	No Connect
DTB	Output	18	24	Data Transmit B
SEL	Input	19	25	Select
CD	Output	20	26	Collision Detect
CK	Input	21	27	20 MHz Clock
DOE	Output	22	28	Data Output Enable

GENERAL DESCRIPTION

The NCR92C02A is a digital transceiver interface used to connect IEEE 802.3 LAN stations into networks constructed from twisted pair media (10BASE-T). The NCR92C02A contains all of the digital functions necessary to implement a 10BASE-T Media Adapter Unit (MAU). Analog circuitry is added for the twisted pair driver, receiver, threshold circuits and for the AUI receiver.

SYSTEM DESCRIPTION

Figure 2 shows an IEEE 802.3 station including an embedded 10BASE-T Media Attachment Unit (MAU) implemented with the NCR92C02A. A typical station includes a Manchester Encoder/ Decoder (MENDEC), the NCR92C02A Twisted Pair Transceiver, a twisted pair interface, and an RJ45 twisted pair connector. The twisted pair interface conditions the signals between the NCR92C02A and the twisted pair media.

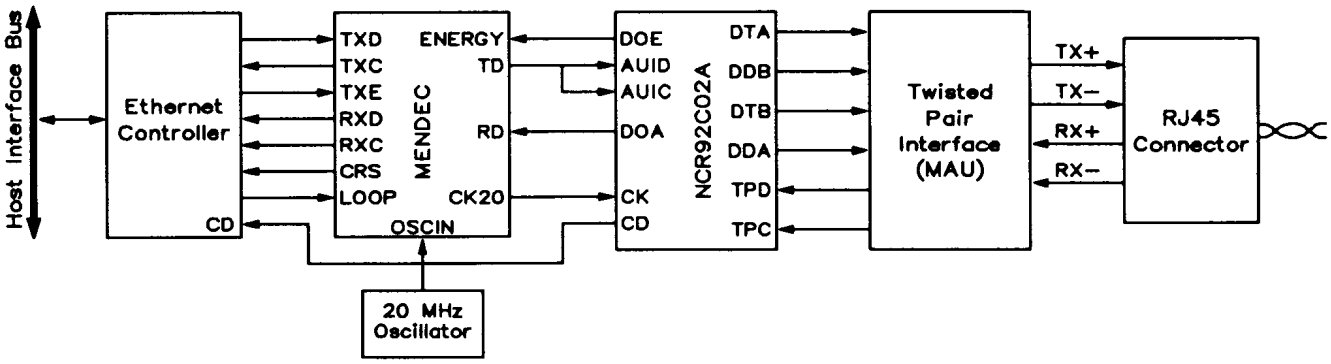


Figure 2 System Block Diagram

MAU TO MENDEC INTERFACE

The NCR92C02A interfaces to the Manchester Encoder/Decoder (MENDEC) as shown in Figure 2. All signals shown in this interface are digital TTL levels. The CK input is a 20 MHz clock with the positive edges occurring at the mid-bit transitions of the data from the MENDEC.

To connect the NCR92C02A to a MENDEC which uses AUI analog signaling, interface components are required as shown in Figure 3. Two comparators are required to sense the DO+/– data from the MENDEC and output to the NCR92C02A AUID and AUIC inputs. The zero comparator translates the differential data into a single-ended logic signal by slicing the data without any offset while the threshold comparator has a bias which requires the input data to reach at least 320 mV before the output changes state. The threshold comparator output must be low when no data is being received.

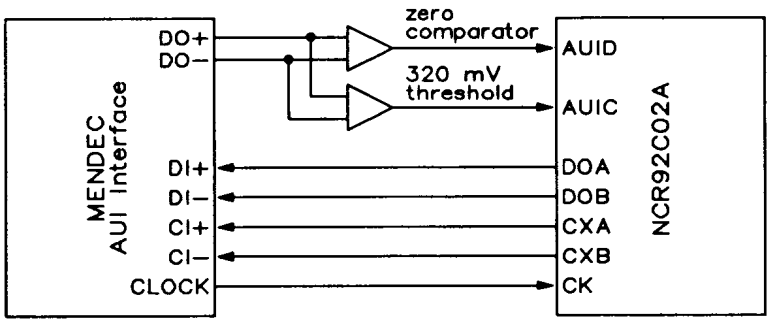


Figure 3 AUI Interface to the NCR92C02A

TWISTED PAIR INTERFACE

Figure 4 shows how the NCR92C02A interfaces to the twisted pair cable through six signals. Four signals are used for data transmission and two are used for data reception from the twisted pair. The Data Transmit signals (DTA and DTB) are used to transmit data from the NCR92C02A to the cable. The Delayed Data signals (DDA and DDB) are used to perform equalization on the transmit data signals. The Twisted Pair Data (TPD) and Twisted Pair Carrier (TPC) signals receive data from the twisted pair.

Transmit Equalization

Transmit equalization reduces the signal jitter caused by interference at the end of a long twisted pair cable. A typical twisted pair cable attenuates a 10 MHz signal more than a 5 MHz signal. Equalization of the transmit signal is needed to decrease the relative power content of the 5 MHz component of the Manchester encoded signal produced by the NCR92C02A. This causes the two components to have approximately the same power content at the far end of the twisted pair link.

A "10" or "01" bit pattern generates a Manchester encoded signal which has a 5 MHz peak frequency component. In a "10" bit pattern, there is a positive signal transition in the middle of the first bit cell followed by a negative transition in the middle of the second. The distance between the transitions is 100 ns. The distance between the transitions of a "01" bit pattern is also 100 ns. This pulse is known as a "long bit." Similarly, the distance between the transitions of a "11" or "00" data bit pattern is 50 ns. This pulse generates the 10 MHz signal component and is known as a "short bit."

The 5 MHz signal component power is reduced by reducing the voltage level of all long bits. This is done with two pairs of output drivers in the NCR92C02A. The pair DTA and DTB are the transmit data and its complement. The pair DDA and DDB are the transmit data delayed by 50 ns. These four data outputs are summed together as shown in Figure 4. The source resistance of these four outputs (see *DC Characteristics* in the *ELECTRICAL SPECIFICATIONS* section on page 15) should be considered in selecting these summing resistors. The values of these four resistors are chosen to allow the twisted pair line to be terminated in 96 Ω ±2 Ω.

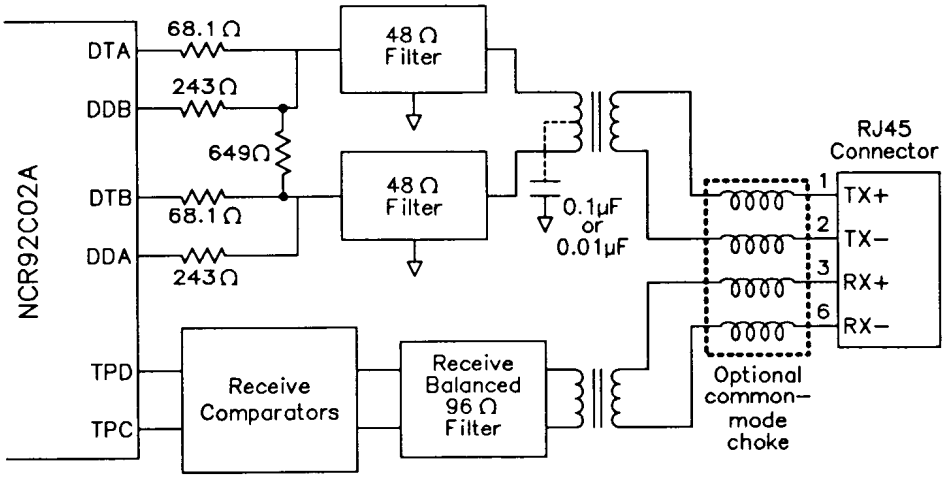


Figure 4 Twisted Pair Interface

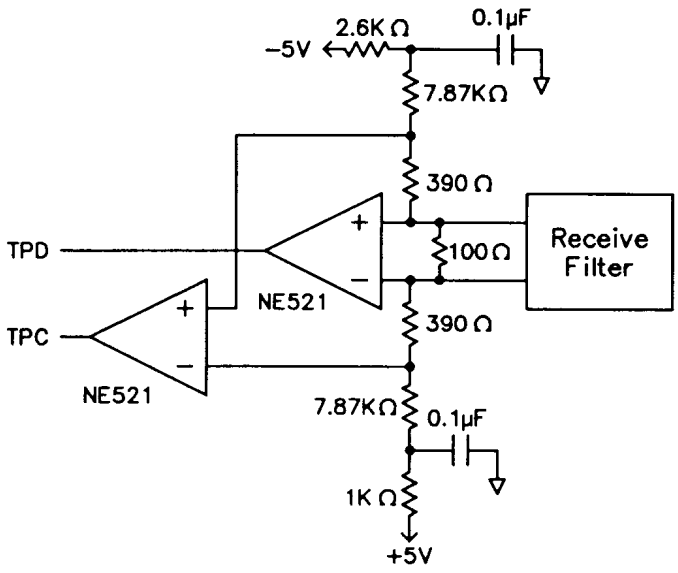


Figure 5 Receive Comparators

Transmit Filter

The transmit filter limits the amount of high frequency energy put onto the cable. This should be accomplished with minimum distortion to both the amplitude and phase of the signal. The signals on the cable have both differential and common-mode components. Common-mode components generate the most radiated energy. In Figure 4, the two transmit filters will attenuate both the differential and common-mode energy before reaching the transformer. For additional attenuation, common-mode chokes can be added. The filters should be at least five pole sections and must have a pass-band impedance that will properly terminate the twisted pair cable. In addition, the filters and the resistors must not cause DDA and DDB to drive more than 32 mA.

Isolation Transformers

Two isolation transformers are needed, one for each signal pair in the twisted pair cable. These transformers isolate the MAU from voltages on the cable. Typically, 1:1 transformers are used with inductance values of 200μH. A different value may be used for transmitter isolation providing the 10BASE-T start-of-idle specifications are met. A 200μH receive transformer with 10% tolerance is not required but will ensure that the received start-of-idle waveform conforms to standard requirements. The capacitor shown in Figure 4 attenuates common-mode energy providing that its value is between 0.1μF and 0.01μF.

Receive Filters

The receive filter is used to remove high frequency noise from the received signal. Typically, a 3-pole elliptic or a 5-pole Butterworth filter is required to meet the return loss specifications of the 10BASE-T standard.

Receive Threshold Detector

The receive threshold detector is part of the twisted pair smart squelch as shown in Figure 5. Two types of signals are rejected (squelched):

1. Any signal whose differential voltage does not exceed 300 mV peak.
2. Any signal that does not make more than two threshold crossings within 400 ns.

The threshold detector rejects the first type of signal since it does not provide voltage transitions on the TPC input unless the signal has a differential

voltage of at least 300 mV peak. The smart squelch logic internal to the NCR92C02A provides the screening against the second type of signal.

Receive Zero Comparator

The receive zero comparator shown in Figure 5 converts the differential twisted pair signal into a signal with digital logic levels and well defined, level transitions. The output of the receiver is the Twisted Pair Data (TPD) input to the NCR92C02A.

PIN DESCRIPTIONS

AUIC: AUI Carrier.
This input must be low when no data is being received from the Manchester Encoder/Decoder (MENDEC). Positive transitions on this signal indicate that data is being transmitted on the AUID signal. The AUIC signal high for more than two bit-times is the start-of-idle pulse which indicates the end of a transmitted packet.

AUID: AUI Data.
This input contains Manchester encoded transmit data. It must be low when receiving a negative signal and high when receiving a positive signal.

CD: Collision Detect.
This output is high only when a collision is detected by the NCR92C02A.

CK: 20 MHz Clock.
This input is used to drive all internal counters and the equalization logic. The positive edges of this 20 MHz clock must be at the mid-bit transitions of the incoming data on AUID.

CXA: Collision A.
When the NCR92C02A detects a collision, a 10 MHz square wave is output on this signal. It is low when no collision is detected.

CXB: Collision B.
When the NCR92C02A detects a collision, a 10 MHz square wave is output on this signal (the inverse of CXA). It is low when no collision is detected.

DDA: Data Delayed A.
This output contains delayed Manchester encoded twisted pair transmit data. Data received from the AUI is transmitted on this signal. DDA is low when no data is being transmitted. When data is being transmitted, DDA is the DTA signal delayed by 50 ns.

DDB: Data Delayed B.
This output contains delayed, inverted Manchester encoded twisted pair transmit data. Data received from the AUI is transmitted on this signal. DDB is low when no data is being transmitted. When data is being transmitted, DDB is the DTB signal delayed by 50 ns.

DOA: Data Out A.
This output contains Manchester encoded receive data. Data received from the twisted pair during receive or from the AUI during transmit loopback is transmitted on this signal. This signal is low when no data is received or looped back. When data is transmitted, DOA is high when a positive differential voltage signal is output on the AUI interface, and low during a negative signal.

DOB: Data Out B.
This output contains inverted Manchester encoded receive data. Data received from the twisted pair during receive or from the AUI during transmit loopback is transmitted on this signal. This signal is low when no data is received or looped back. When data is being transmitted, DOB is low when a positive differential voltage signal is output on the AUI interface, and high during a negative signal.

DOE: Receive Data Enable.
This output is high when data is output on DOA and DOB. It is low when no data is output.

DTA: Data Transmit A.
This output contains the Manchester encoded twisted pair transmit data. Data received from the AUI is transmitted on this signal. DTA is low when no data is being transmitted. When data is transmitted, the DTA signal is high when a positive differential voltage signal is transmitted on the twisted pair cable, and low during a negative signal.

DTB: Data Transmit B.
This output contains the inverted Manchester encoded twisted pair transmit data. Data received from the AUI is transmitted on this signal. DTB is low when no data is being transmitted. When data is transmitted, the DTB signal is low when a positive differential voltage signal is transmitted on the twisted pair cable, and high during a negative signal.

-HBEN: Heart Beat Enable.
This input is used to configure the NCR92C02A for operation in a repeater or station. When high, the SQE test function and loopback of AUI data are disabled. When low (station select), the SQE test function and loopback of AUI data are enabled. See the description for the SEL input below.

LINK: Link Status.
When this output is low, the NCR92C02A is in its link fail state. Otherwise, this signal is high.

LKSEL: Link Select.
This input enables the link beat test function. When high (disabled), no link beat pulses are generated by the NCR92C02A, and a lack of received link beat pulses will not cause the NCR92C02A to enter its link fail state. When low (enabled), the NCR92C02A generates link beat pulses every 13 ms, and expects to receive link beat pulses with spacing between 6.5 and 105 ms.

SEL: Select.
This input is used to select the NCR92C02A in a multiport repeater application. When this signal is high, the NCR92C02A accepts data from the AUID and AUIC signals, and transmits it on the DTA, DTB, DDA, and DDB twisted pair signals. When low, the AUID and AUIC signals are ignored, and no twisted pair transmit or AUI loopback occurs.

NOTE: There are only three valid combinations of the -HBEN and SEL inputs:

SEL	-HBEN	Description
0	0	This is an illegal condition. The NCR92C02A does not function properly with this combination.
0	1	This combination is used with a multiport repeater. In a multiport repeater, there are typically 12 to 16 NCR92C02As that work with a single repeater controller. The SQE test function and AUI loopback are always disabled. Data received from the AUI input is not transmitted to the twisted pair.
1	0	This is used for an IEEE 802.3 station. The SQE test function and AUI loopback are enabled and data received from the AUI input is transmitted to the twisted pair.
1	1	This is used with a multiport repeater. In a multiport repeater, there are 12 to 16 NCR92C02As that work with a single repeater controller. The SQE test function and AUI loopback are always disabled. When SEL is high for a particular NCR92C02A, data received from AUID is transmitted on the twisted pair. Data received at TPD is transmitted on DOA and DOB.

TPC: Twisted pair Carrier.
Rising edges on this input indicate that data is being received on the TPD signal. This signal must be low when no data is being received from the twisted pair interface. The start of an idle pulse is indicated by the TPC signal staying high for more than two bit-times. The idle pulse indicates the end of a received packet.

TPD: Twisted Pair Data.
This input contains Manchester encoded data from the twisted pair media. TPD must be low when a negative differential voltage signal is received from the twisted pair cable, and high when a positive signal is received.

FUNCTIONAL DESCRIPTION

Figure 6 shows the major functions of the NCR92C02A. Each function is described below.

OUTPUT CONTROL

The output control section of the NCR92C02A performs three functions. First, it controls the gating of data between the AUI and the twisted pair cable. Second, it performs equalization control when transmitting data on the twisted pair. Third, it detects collision conditions and generates the collision presence signal to the Manchester Encoder/Decoder (MENDEC).

Gating Control

The gating control logic of the NCR92C02A can be in one of three states: receive, transmit or idle.

In the receive state, data is being received from the twisted pair cable, and transmitted to the DOA and DOB outputs.

In the transmit state, data is received from the AUI and transmitted to the twisted pair cable through DTA, DTB, DDA, and DDB. DTB is inverse of DTA. DDA and DDB are the DTA and DTB outputs delayed by 50 ns. The AUI data is also looped back to the AUI using the DOA and DOB outputs.

In the idle state, no data is transmitted or received by the NCR92C02A. The NCR92C02A is normally in idle state. The receive state is entered when the twisted pair smart squelch indicates to the gating control logic that data is being received from the twisted pair. The transmit state is entered when the AUI squelch indicates to the gating control logic that data is being received from the AUI. If a collision occurs during transmit, the gating control logic switches to the receive state until the end of the collision.

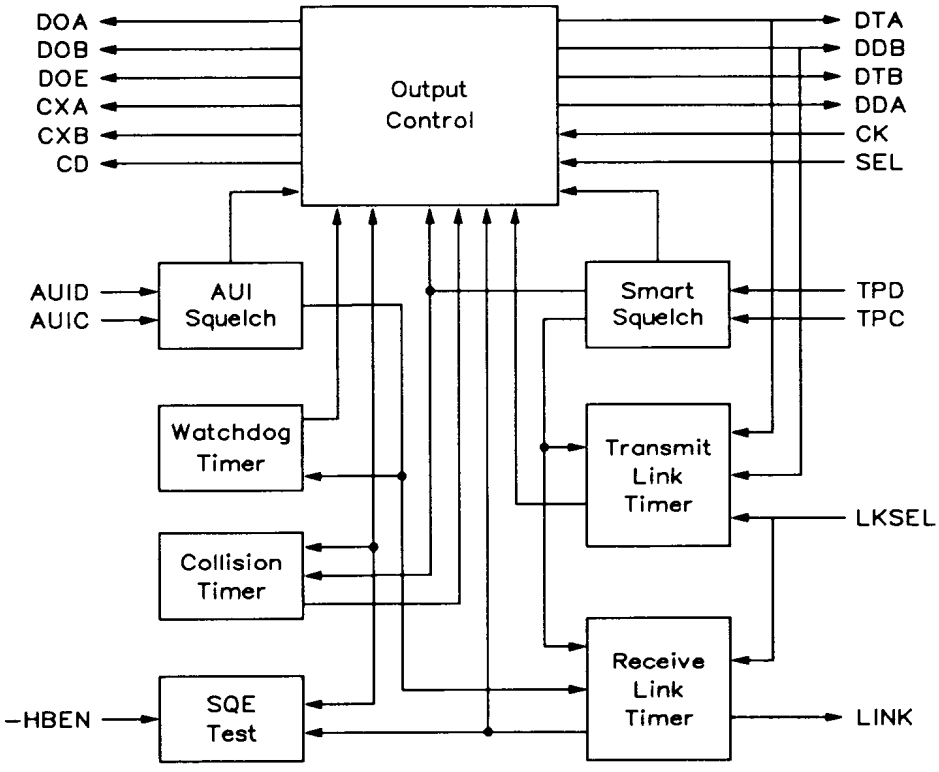


Figure 6 NCR92C02A Block Diagram

Equalization

Four signals are used to transmit data on the twisted pair cable as shown in Figure 7. The DTA signal is the Manchester encoded data being transmitted. The DTB output is the inverse of DTA. DDA and DDB are the DTA and DTB outputs delayed by 50 ns. DTA and DDB outputs are externally summed together to generate the positive twisted pair transmit signal. Likewise, DTB and DDA are summed together.

During short bits which have a duration of 50 ns, the DTA and DDB outputs are identical and so are DTB and DDA. During a long bit, DTA and DDB are identical only for the first 50 ns. For the second half of the bit, DDB is the inverse of DTA. The strength of the 5 MHz signal composed of long bits is reduced by reducing the voltage level of the second half of the bit.

Collision Detection

The collision detection logic detects when transmit and receive signals occur simultaneously on the twisted pair lines. In this case, the collision condition is signaled to the AUI by the CD output signal high. A 10 MHz collision presence signal is generated on both the CXA and CXB outputs.

SMART SQUELCH

The TPC input to the NCR92C02A is used to determine when valid data is being received from the twisted pair cable. When valid data is received, both the TPC and TPD inputs transition from low to high as the cable RX signal pair transitions from a negative to positive differential voltage.

At the beginning of a reception, the smart squelch accepts no data from the twisted pair and the DOE, DOA, and DOB outputs are all low. When data begins to arrive, both the TPD and TPC inputs begin to transition. The smart squelch enters its unsquelch state after the second rising edge of TPC. The DOE output goes high, and the TPD input is sent to the DOA and DOB outputs. The smart squelch continues in this state until it receives the start-of-idle waveform.

If there is already activity on the AUID and AUIC inputs, then activity on the TPD and TPC inputs indicates a collision. In this case, the smart squelch takes longer to enter its unsquelch state to protect against false collisions due to impulse noise on the twisted pair cable. The smart squelch enters its unsquelch state after the third rising edge of TPC instead of the second. The CD output goes high, and a 10 MHz collision presence signal is generated on the CXA and CXB outputs. An internal 350-400 nanosecond timer is reset after the third rising edge of TPC. When this timer expires, the twisted pair data on the TPD input is sent to the AUI using the DOA and DOB outputs. This ensures that the NCR92C05A will detect the collision signal on CD before any glitches occur on DOA and DOB during the switch.

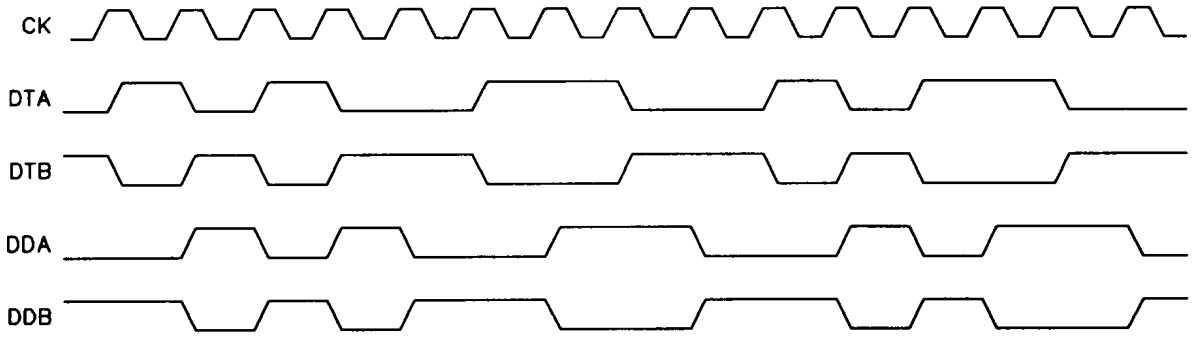


Figure 7 Output Control Timing: Equalization

The collision condition ends when either the AUI or the twisted pair goes inactive. If the collision is ended by the twisted pair interface, then the internal timer is reset, and it is used to extend the collision signal on CD, CXA, and CXB while the AUI data is sent to the DOA and DOB outputs.

The start-of-idle waveform is a long, high pulse following the last low-to-high transition of the receive data from the twisted pair cable. When no transitions occur on TPC for 150-175 ns, the data on TPD is squelched and a start-of-idle pulse is generated on the DOA and DOB outputs.

While in idle, successive rising edges of the TPC signal farther apart than 350-400 ns will be ignored to reject out-of-band signals such as noise and low frequency interference.

AUI SQUELCH

The AUIC input to the NCR92C02A is used to determine when there is valid data being transmitted from the AUI to the NCR92C02A. When valid data is being transmitted, both the AUIC and AUID inputs transition.

At the beginning of a transmission, the AUI squelch is in its squelch state. No data is accepted from the AUI, the DOE, DOA, and DOB outputs are all low, and the DTA, DTB, DDA, and DDB twisted pair outputs are all low. When data begins to arrive, the AUIC input begins to transition. The AUI squelch enters its unsquelch state after the first rising edge of AUIC. The DOE output goes high and the AUID input is looped back to the DOA and DOB outputs. The transmit data from the AUID input is sent to the twisted pair, and transmitted on the DTA, DTB, DDA, and DDB outputs. The AUI squelch continues in this state until the start-of-idle waveform is received on the AUIC input.

If there is already activity on the TPD and TPC inputs, then activity on the AUID and AUIC inputs indicates a collision condition. The CD output goes high after the first rising edge of AUIC, and a 10 MHz collision presence signal is generated on the CXA and CXB outputs. When the collision condition is ended by the AUI going inactive, the CD signal goes low, and the collision presence signal ends on the CXA and CXB outputs after the last rising edge of AUIC.

The start-of-idle waveform is a long, high pulse following the last low-to-high transition of the transmit data from the AUI. Each rising and falling edge of AUIC resets an internal 125-250 nanosecond timer. When this timer expires, the AUI squelch enters its squelch state and generates a start-of-idle pulse on AUI using the DOA and DOB outputs, and on the twisted pair interface using the DTA, DTB, DDA, and DDB outputs.

If the SEL input is low, then the AUI squelch is disabled and the AUID signal is blocked. The NCR92C02A still receives data from the twisted pair interface and sends the data to the AUI, but data received from the AUI is ignored. AUI data will not be looped back to the DOA and DOB outputs, and will not cause a collision condition if there is simultaneous twisted pair activity. The SEL input can be used with a multiport repeater to disable the NCR92C02A device from which data is being received, while broadcasting to all the other NCR92C02A devices connected to the repeater.

TRANSMIT LINK TIMER

When the NCR92C02A is not transmitting data on the twisted pair cable, it generates periodic link beat test pulses. These test pulses are used to inform the MAU at the other end of the twisted pair cable that the twisted pair link is still intact and has not been broken or shorted.

An internal timer determines when the twisted pair has been inactive long enough to require a link beat pulse. This timer resets when DTA is high and DDB is low which occurs during the link beat pulse and during the start-of-idle pulse; the timer resets at the end of each normal transmission.

When the timer expires, a link beat pulse is generated as shown in Figure 8 and the timer is reset. Another pulse is generated if no further transmit activity occurs before the timer expires again. The link beat pulse contains positive voltage transitions only, instead of the positive and negative transitions seen in normal data.

The NCR92C02A generates a link beat test pulse whenever there is no transmit activity on the DTA, DTB, DDA, and DDB outputs for 13 ms. If the LKSEL input is high, the NCR92C02A does not generate link beat test pulses even if there is activity on the twisted pair link. This allows the NCR92C02A to be used in applications with equipment predating the 10BASE-T standard that does not implement active link testing.

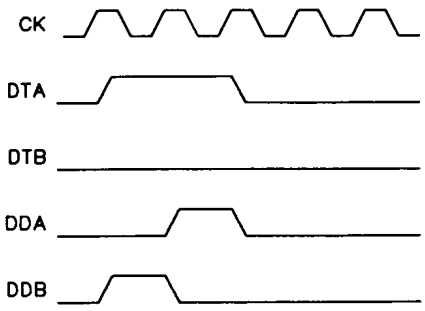


Figure 8 Transmit Link Test Timing

RECEIVE LINK TIMER

As the NCR92C02A is transmitting link beat test pulses, it expects to receive normal data or periodic link beat test pulses. An internal 105 ms timer is used and reset when the twisted pair smart squelch is active. If the timer expires, no data or link beat pulses have been received and the twisted pair link is assumed to be broken.

Since a link beat pulse is a single positive voltage transition, the receive link timer expects to see a single, isolated pulse on the TPC input. These pulses must not be spaced closer together than specified, or they are assumed to be caused by impulse noise and ignored.

If no link beat pulses are received before the receive link timer expires, the NCR92C02A enters its link fail state. The AUI squelch is disabled so that transmissions from the AUI are ignored. The NCR92C02A will not transmit data but can receive data. The SQE test function is not performed. The LINK output is low to indicate that the link fail state is effective; LINK is high otherwise.

At least two link beat pulses must be received before the NCR92C02A will exit its link fail state. If data is currently being received from the AUI when the third link beat pulse is received, the NCR92C02A waits until the end of the transmission before exiting the link fail state.

If LKSEL is high, received link test pulses are ignored, and the NCR92C02A does not enter its link fail state even if the LINK output is still low.

SQE TEST

After every transmission received from the AUI, a short collision presence signal is generated using the CD, CXA, and CXB outputs. This signal is used to test the output drivers and to test the ability of the Manchester Encoder/Decoder (MENDEC) to detect the collision signal. If the output drivers or the collision signal cannot be detected, then collisions cannot be detected. In the case, transmissions which collide need to be transmitted again; they appear to be correctly transmitted because the collision goes unnoticed.

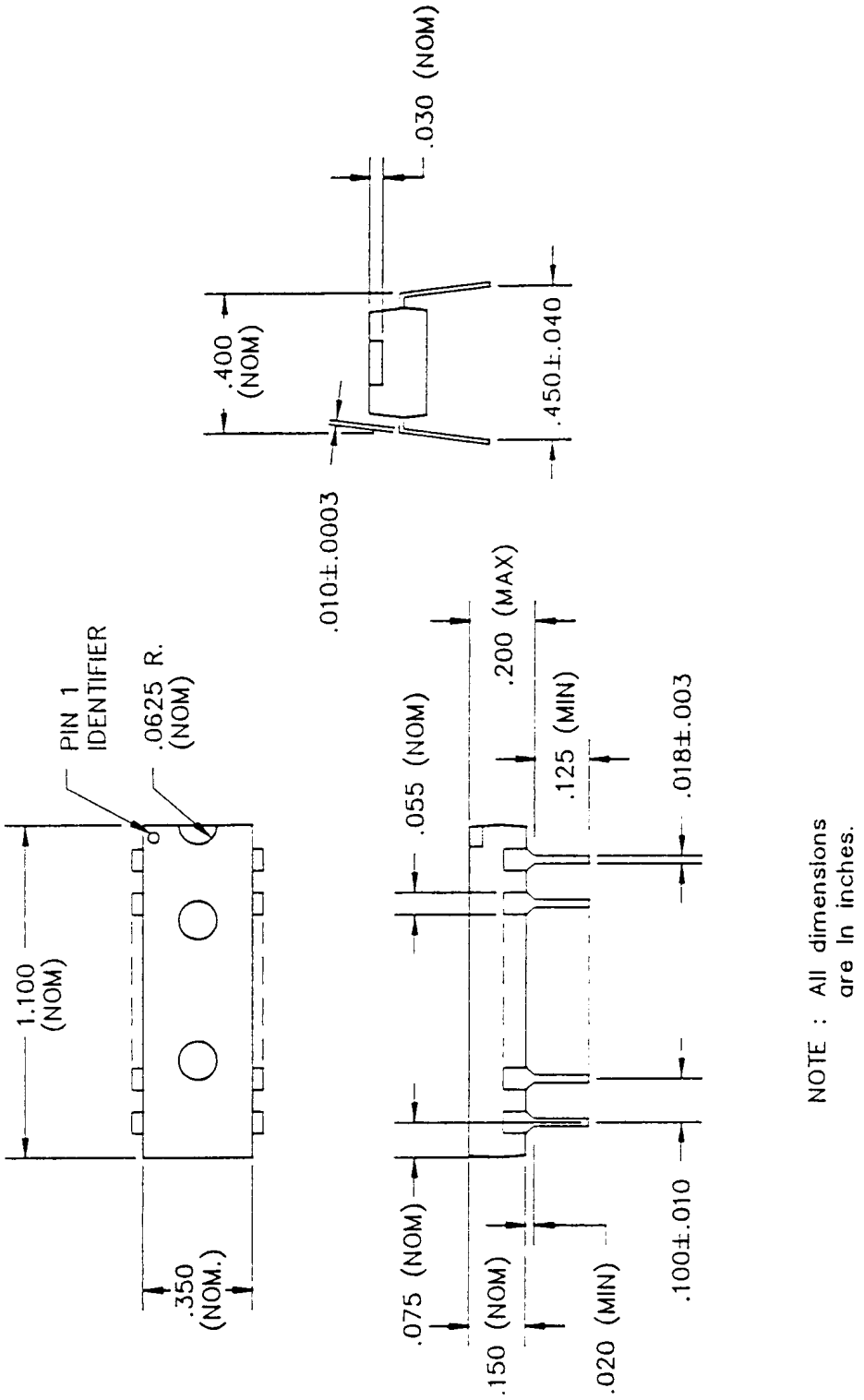
The Signal Quality Error (SQE) test is performed only if the -HBEN input is low. Otherwise, no collision signal is generated at the end of each transmission.

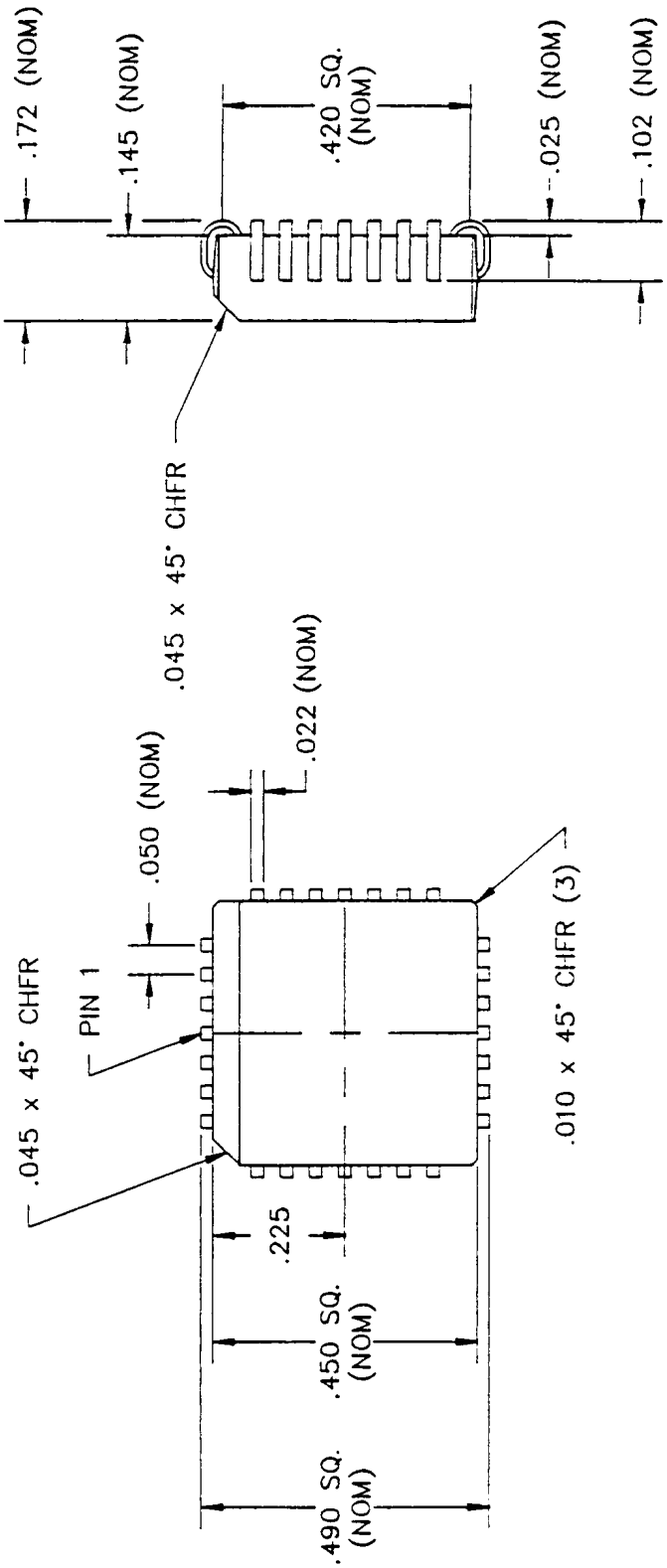
WATCHDOG TIMER

The watchdog timer function prevents a broken transmitter from transmitting continually (jabbering) and corrupting the LAN. An internal 26 ms timer is reset whenever the AUI squelch goes active. If the timer expires and the squelch is still active, the NCR92C02A enters its jabber state until the squelch goes inactive again.

When the NCR92C02A is in its jabber state, the DOE, DOA, and DOB outputs are disabled and the collision presence signal is continually generated on CD, CXA, and CXB. The DTA, DTB, DDA, and DDB twisted pair outputs are disabled except when used to generate link beat test pulses. If no link beat pulses are received, the NCR92C02A will enter its link fail state. The NCR92C02A exits its jabber state only when the AUI squelch has been inactive for at least 0.42 seconds.

MECHANICAL SPECIFICATIONS





NOTE : All dimensions are in inches.

ORDERING INFORMATION

The NCR92C02A is available in a 28-pin Plastic Leaded Chip Carrier (PLCC) or a 22-pin Dual In-line Package (DIP). Use the following part numbers to order the desired package.

Package Type	Part Number
28-pin PLCC	NCR92C02APP
22-pin DIP	NCR92C02APD

BACKGROUND INFORMATION

Additional information can be found in the following documents:

1. Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD), ANSI/IEEE Standard 802.3-1985, Institute of Electrical and Electronic Engineers, New York.
2. Information Processing Systems - Local Area Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Access Method and Physical Layer Specifications, ISO International Standard 8802-3:1989, Institute of Electrical and Electronic Engineers, New York.
3. Twisted Pair Medium Attachment Unit and Baseband Medium, Type 10BASE-T, IEEE Preliminary Standard P802.3I/D6, Draft F, March, 1989, Institute of Electrical and Electronic engineers, New York.
4. *10BASE-T Primer.* NCR Communication Products, Release 1.0 NCR Corporation, Dayton, Ohio, U.S.A. September, 1990.

ELECTRICAL SPECIFICATIONS

Absolute Maximums

Symbol	Parameter	Minimum	Maximum	Units
T_A	Operating Temperature	0	70	°C
T_S	Storage Temperature	−55	150	°C
V_{DD}	Supply Voltage	−0.5	7.0	V
V_{IN}	Input Voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
T_L	Lead Temperature (Soldering 10 seconds maximum)		250	°C

DC Characteristics

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units
V_{IL}	Low Input Voltage	V_{SS} − 0.5	0.8	Volts
V_{IH}	High Input Voltage	2.0	V_{DD} + 0.5	Volts
V_{OL}	Low Output Voltage: DTA and DTB (IOL = 32 mA) DDA and DDB (IOL = 32 mA) LINK, DOA, DOB (IOL = 24 mA) CXA, CXB (IOL = 24 mA) all other outputs (IOL = 4 mA)		0.45 0.45 0.40 0.40 0.40	Volts
V_{OH}	High Output Voltage: DTA and DTB (IOH = −32 mA) DDA and DDB (IOH = −32 mA) LINK, DOA,DOB (IOH = −12 mA) CXA, CXB (IOH = −12 mA) all other outputs (IOH = −4 mA)	4.43 4.43 4.0 4.0 4.0		Volts
I_{OL}	Low Output Current: DTA, DTB, DDA, and DDB LINK, DOA, DOB, CXA, CXB all other outputs		32 24 4	mA
I_{OH}	High Output Current: DTA, DTB, DDA, DDB LINK, DOA, DOB, CXA, CXB all other outputs		32 12 2	mA
R_{OL}	Output Source Resistance: DTA and DTB (current sink) DDA and DDB		12.5 12.5	Ω
R_{OH}	Output Source Resistance: DTA and DTB (current source) DDA and DDB		12.5 12.5	Ω
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		12.5	pF

AC Characteristics

Twisted Pair Output Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
1	Clock period (+/– 0.01%)	9		50		ns
2	CK to DTA delay	9			30	ns
3	DTA to DTB skew	9	–2		2	ns
4	DTA to DDA delay	9	47		53	ns
5	CK to DDA delay	9			30	ns
6	DDA to DDB skew	9	–2		2	ns
7	DTB to DDB delay	9	47		53	ns

Receive Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
8	TPD pulse high (short bits)	10	36		64	ns
8	TPD pulse high (long bits)	10	86		114	ns
9	TPD pulse low (short bits)	10	36		64	ns
9	TPD pulse low (long bits)	10	86		114	ns
10	TPD high to TPC high delay	10			20	ns
11	TPC low before TPD low delay	10			20	ns
12	TPC pulse high	10	8		184	ns
13	TPC pulse low	10	8		184	ns
14	TPC high to DOE turn on	10			500	ns
15	TPC high to DOA – unsquelch	10			500	ns
16	TPD to DOA delay	10			25	ns

Receive Start of Idle (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
17	TPD pulse high – SOI	11	225			ns
18	TPC pulse high – SOI	11	185			ns
19	TPC high to DOE turn off	11			500	ns
20	DOA pulse high – SOI	11	225		350	ns

Transmit Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
21	AUID setup to CK high	12	10			ns
22	AUID hold from CK high	12	10			ns
23	AUID pulse low (short bits)	12	36		64	ns
23	AUID pulse low (long bits)	12	86		114	ns
24	AUID pulse high (short bits)	12	36		64	ns
24	AUID pulse high (long bits)	12	86		114	ns
25	AUID high to AUIC high delay	12			20	ns
26	AUIC low before AUID low delay	12			20	ns
27	AUIC pulse low	12	8			ns
28	AUIC pulse high	12	8			ns
29	AUIC to DOE turn on	12	50		110	ns
30	AUIC to DTA delay – unsquelch	12	100		200	ns
31	AUID to DOA delay – AUI loopback	12			100	ns

Transmit Start of Idle (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
32	AUID pulse high – SOI	13	200			ns
33	AUIC pulse high – SOI	13	200			ns
34	AUIC high to DOE turn off	13			500	ns
35	DTA pulse high – SOI	13	250		350	ns

Collision Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
36	TPC high to CD – collision	14			900	ns
37	TPC high to CD – end of collision	15			900	ns
38	AUIC to CD delay – collision detection	16			900	ns
39	AUIC to CD delay – end of collision	17			900	ns

Link Test Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
40	DTA link pulse width	18		100		ns
41	DDA, DDB link pulse width	18		50		ns
42	Duration between transmitted link pulses	18	8	13	24	ms
43	Duration between received link pulses	18	6.5		105	ms

SQE Test Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
44	AUIC to CD delay	19	600		1600	ns
45	CD pulse high	19	500		1500	ns

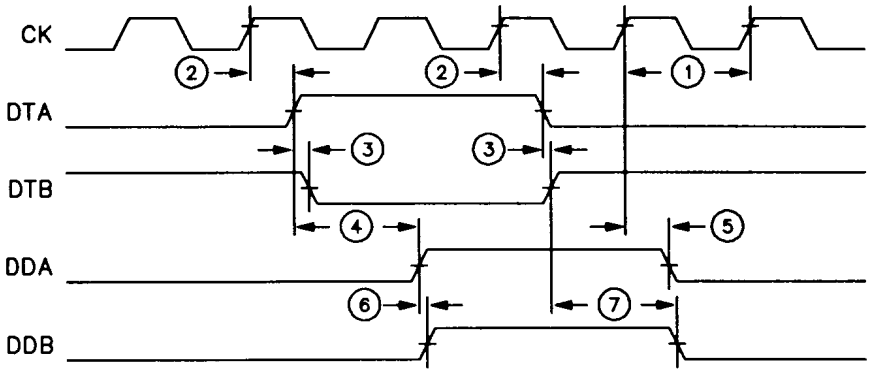


Figure 9 Twisted Pair Output Timing

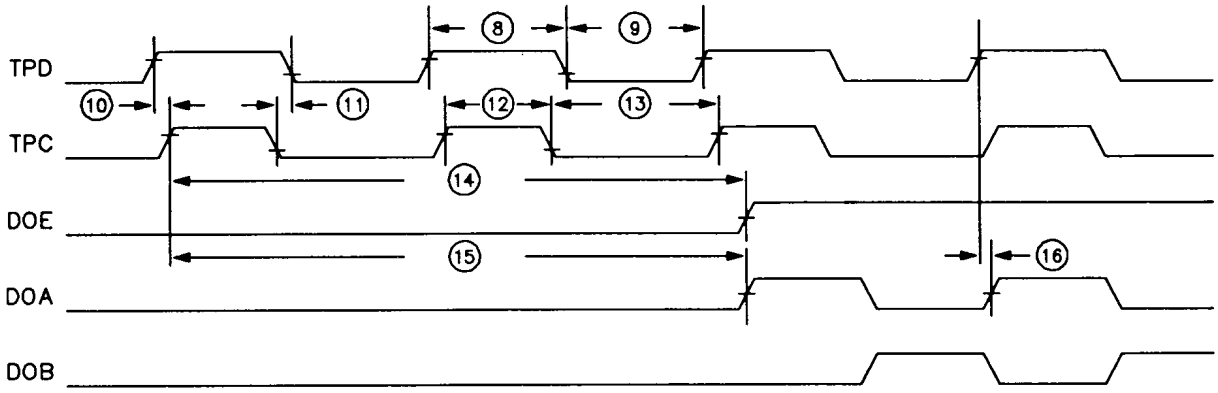


Figure 10 Receive Timing

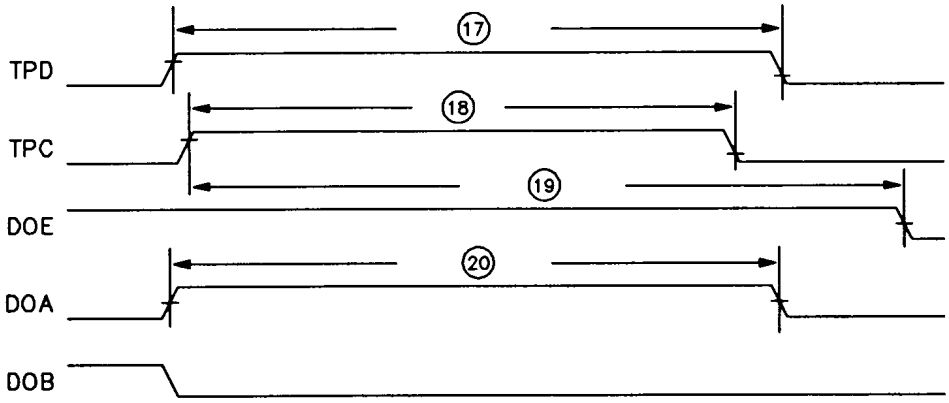


Figure 11 Receive Start of Idle

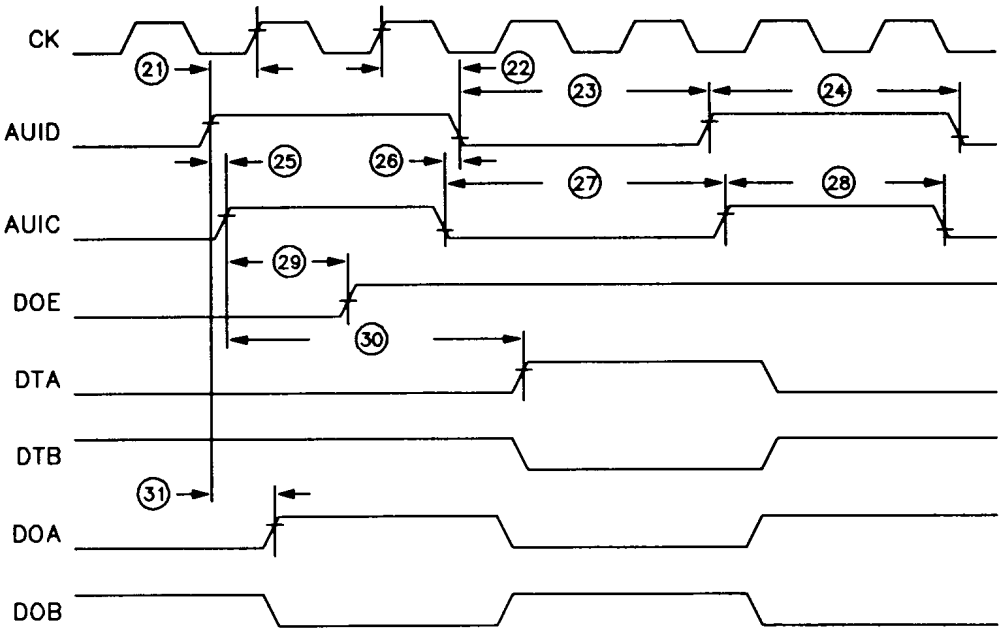


Figure 12 Transmit Timing

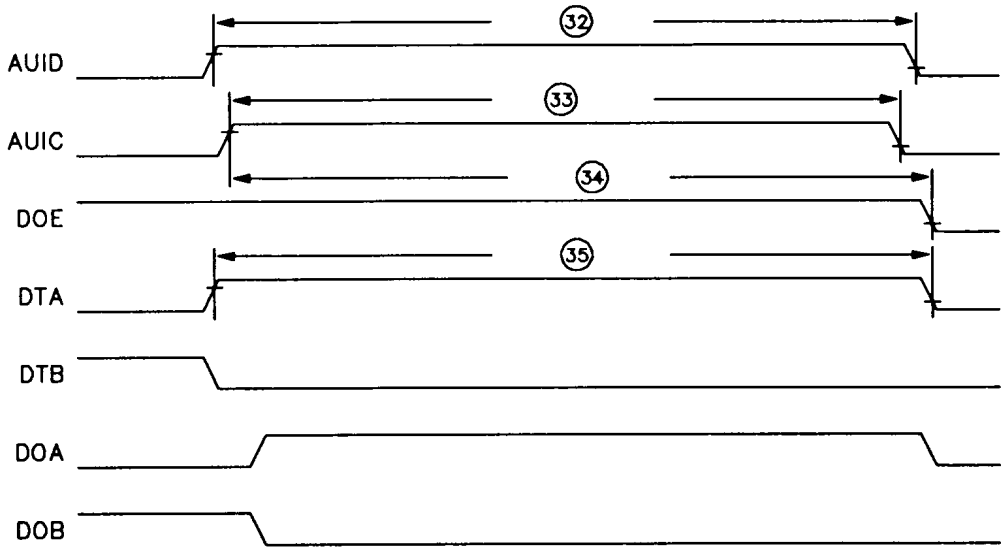


Figure 13 Transmit Start of Idle

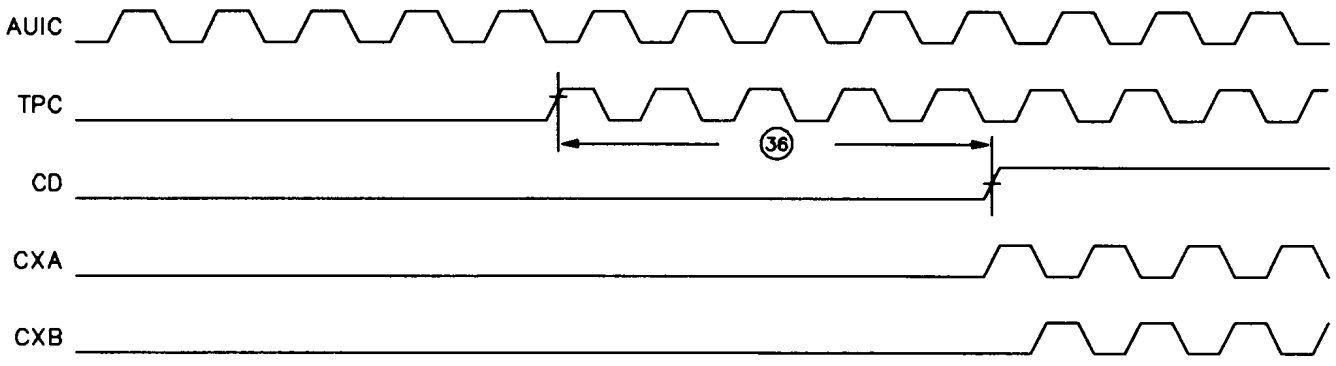


Figure 14 Twisted Pair Collision Detection

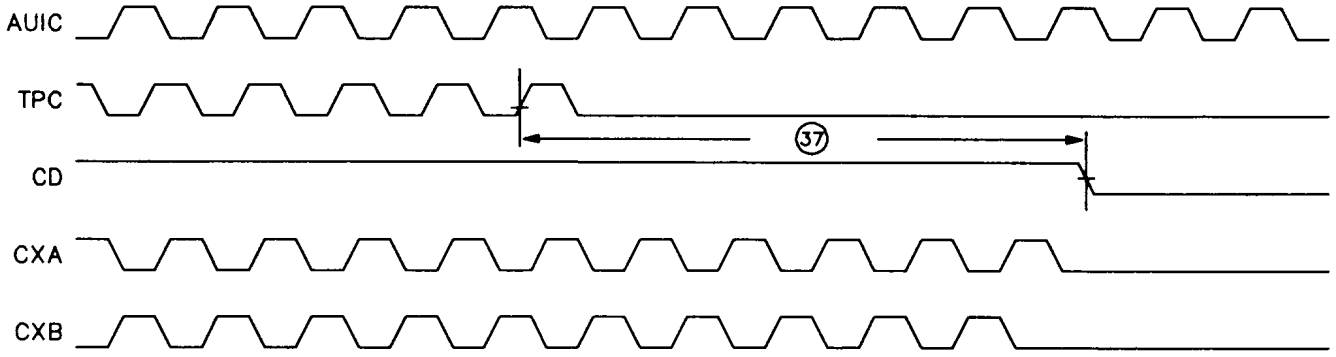


Figure 15 Twisted Pair End of Collision

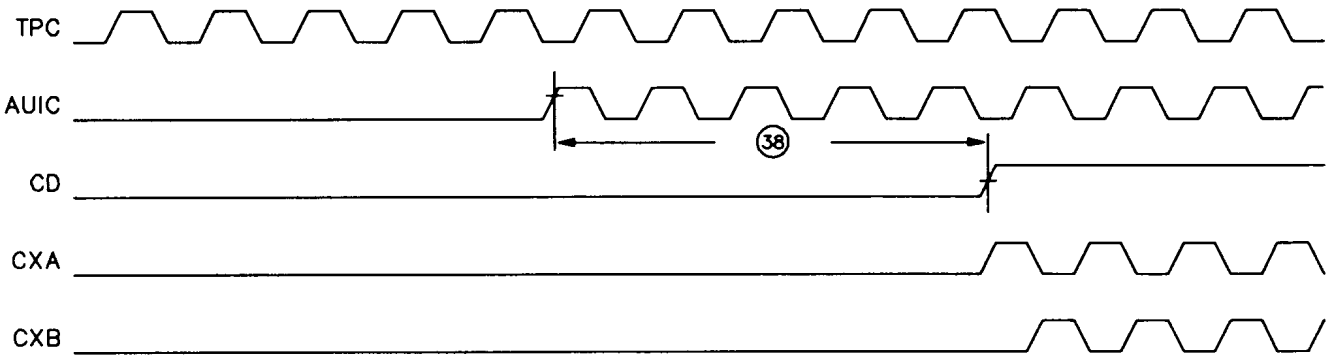


Figure 16 AUI Collision Detection

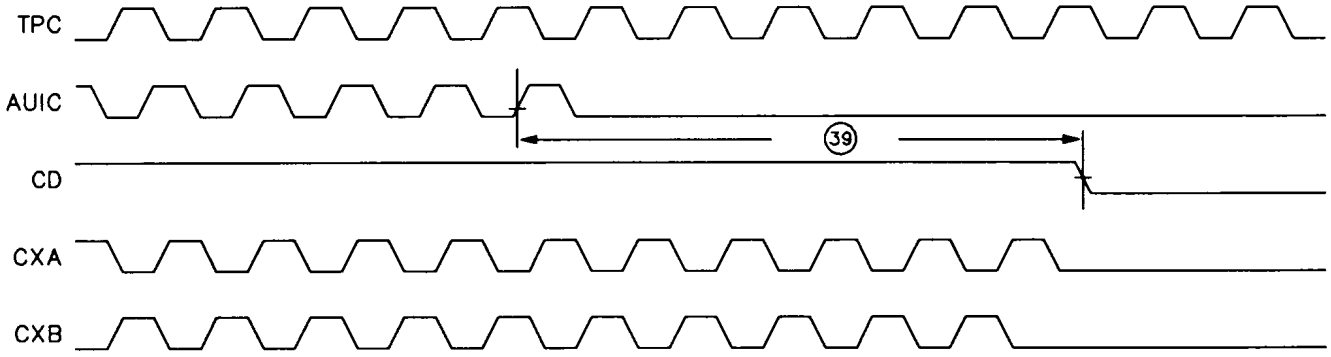


Figure 17 AUI End of Collision

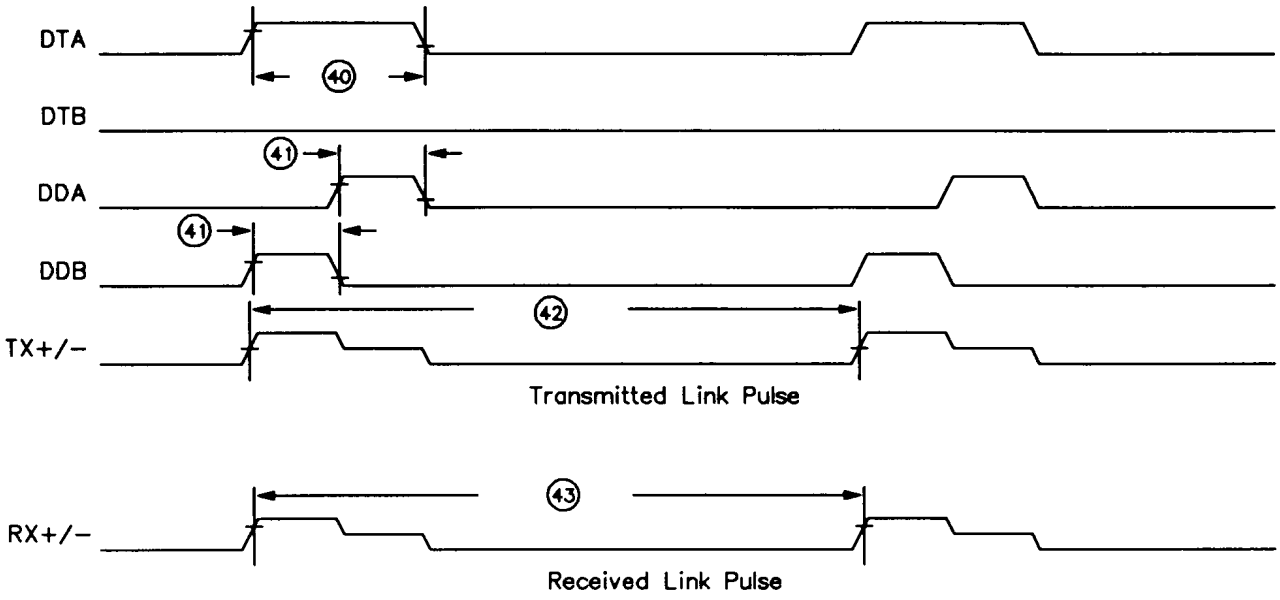


Figure 18 Link Test Timing

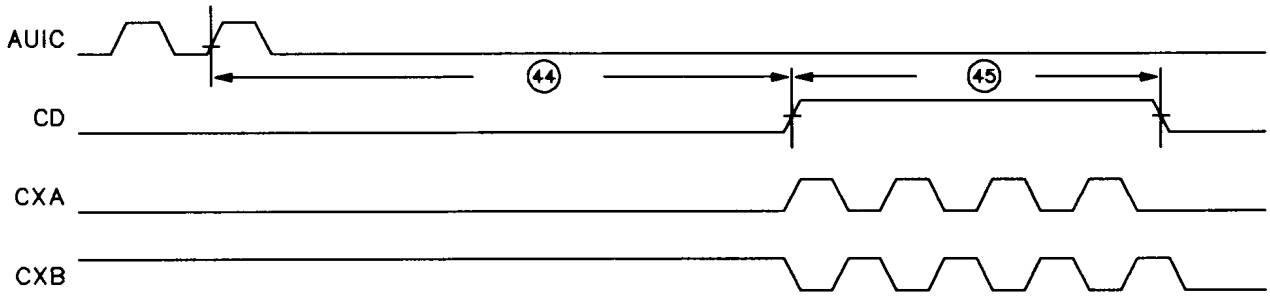


Figure 19 SQE Test Timing

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