

Dual NPN-PNP complementary bipolar transistor

Features

- High gain
- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count

Applications

- Push-pull or Totem-Pole configuration
- MOSFET and IGBT gate driving
- Motor, relay and solenoid driving

Description

The STS05DTP03 is a hybrid dual NPN-PNP complementary power bipolar transistor manufactured by using the latest low voltage planar technology. The STS05DTP03 is housed in dual island SO-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in Push-Pull or Totem Pole configuration as post IGBTs and MOSFETs driver.

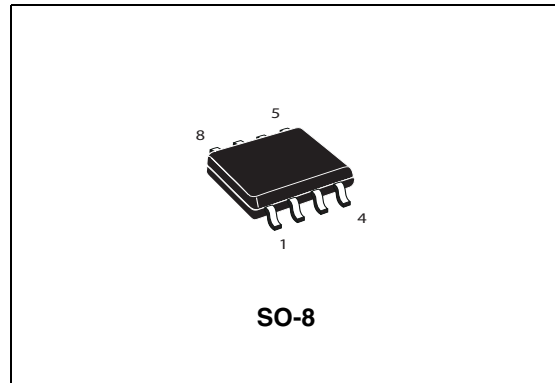


Figure 1. Internal schematic diagram

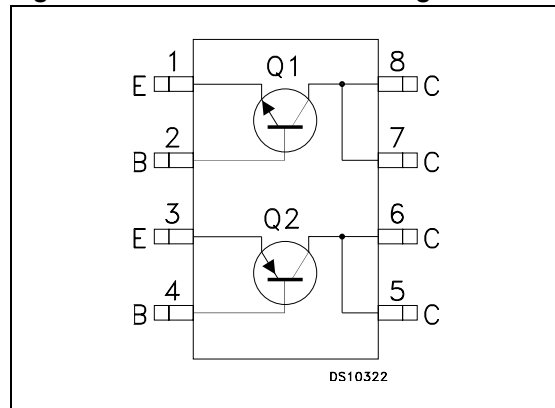


Table 1. Device summary

Order code	Marking	Package	Packaging
STS05DTP03	S05DTP03	SO-8	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		NPN	PNP	
V_{CBO}	Collector-base voltage ($I_E = 0$)	45	-45	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	30	-30	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	6	-6	V
I_C	Collector current	5	-5	A
I_{CM}	Collector peak current ($t_p < 5$ ms)	10	-10	A
I_B	Base current	1	-1	A
I_{BM}	Base peak current ($t_p < 1$ ms)	2	-2	A
P_{TOT}	Total dissipation at $T_{amb} = 25$ °C single operation	2		W
P_{TOT}	Total dissipation at $T_{amb} = 25$ °C couple operation	1.6		W
T_{stg}	Storage temperature	-65 to 150		°C
T_J	Max. operating junction temperature	150		

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient (single operation)	62.5	°C/W
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient (dual operation)	78	°C/W

1. When mounted on 1inch² pad 2oz. copper, $t < 10$ sec

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$; unless otherwise specified)

Table 4. Q1-NPN electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current ($I_E = 0$)	$V_{CB} = 30\text{ V}$			10	μA
I_{CEO}	Collector cut-off current ($I_B = 0$)	$V_{CE} = 30\text{ V}$			1	μA
I_{EBO}	Emitter cut-off current ($I_B = 0$)	$V_{EB} = 6\text{ V}$			10	μA
$V_{(BR)CEO}^{(1)}$	Collector-emitter breakdown voltage ($I_B = 0$)	$I_C = 10\text{ mA}$	30			V
$V_{CE(sat)}^{(1)}$	Collector-emitter saturation voltage	$I_C = 1\text{ A}$ $I_B = 10\text{ mA}$ $I_C = 3\text{ A}$ $I_B = 100\text{ mA}$ $I_C = 5\text{ A}$ $I_B = 250\text{ mA}$			0.25 0.7 0.7	V V V
$V_{BE(sat)}^{(1)}$	Base-emitter saturation voltage	$I_C = 1\text{ A}$ $I_B = 10\text{ mA}$			1.0	V
$h_{FE}^{(1)}$	DC current gain	$I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 3\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 5\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 10\text{ A}$ $V_{CE} = 2\text{ V}$	100 100 80	140 100 40	300	

1. Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$

Table 5. Q2-PNP electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current ($I_E = 0$)	$V_{CB} = -30$ V			-10	μ A
I_{CEO}	Collector cut-off current ($I_B = 0$)	$V_{CE} = -30$ V			-1	μ A
I_{EBO}	Emitter cut-off current ($I_B = 0$)	$V_{EB} = -6$ V			-10	μ A
$V_{(BR)CEO}^{(1)}$	Collector-emitter breakdown voltage ($I_B = 0$)	$I_C = -10$ mA	-30			V
$V_{CE(sat)}^{(1)}$	Collector-emitter saturation voltage	$I_C = -1$ A $I_B = -10$ mA $I_C = -3$ A $I_B = -100$ mA $I_C = -5$ A $I_B = -250$ mA			-0.25 -0.7 -0.7	V V V
$V_{BE(sat)}^{(1)}$	Base-emitter saturation voltage	$I_C = -1$ A $I_B = -10$ mA			-1.0	V
$h_{FE}^{(1)}$	DC current gain	$I_C = -1$ A $V_{CE} = -2$ V $I_C = -3$ A $V_{CE} = -2$ V $I_C = -5$ A $V_{CE} = -2$ V $I_C = -10$ A $V_{CE} = -2$ V	100 100 80 40	140 100 40	300	

1. Pulsed duration = 300 μ s, duty cycle \leq 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. DC current gain Q1 NPN transistor Figure 3. DC current gain Q1 NPN transistor

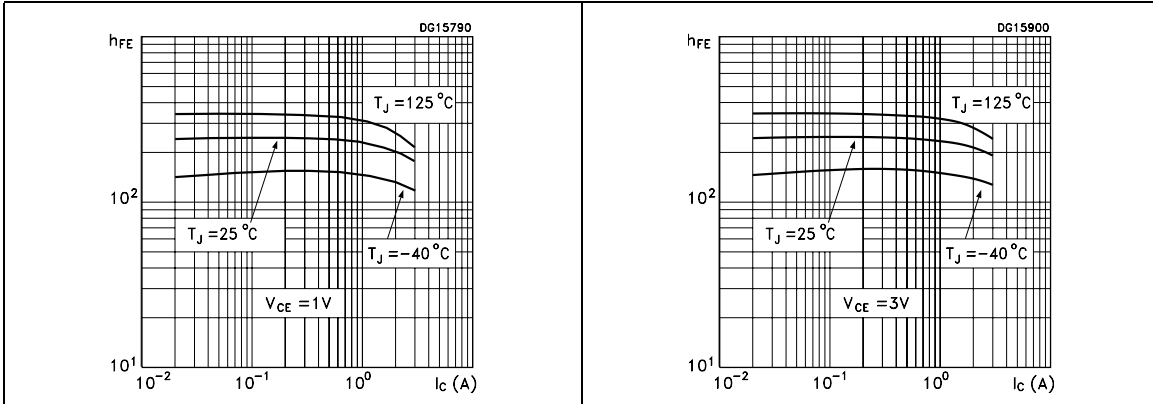


Figure 4. Collector-emitter saturation voltage Q1 NPN transistor

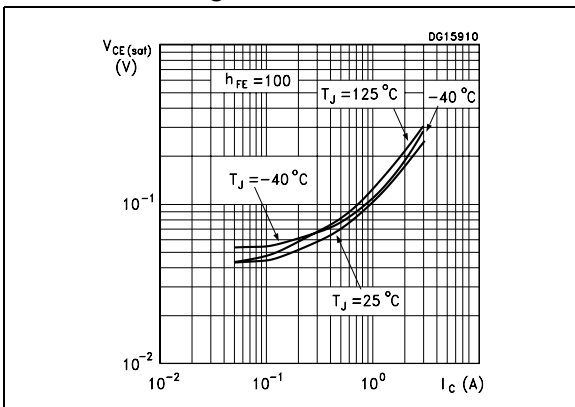


Figure 5. Base-emitter saturation voltage Q1 NPN transistor

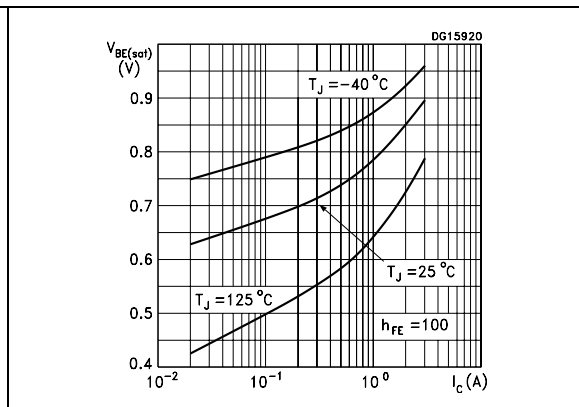


Figure 6. Switching time resistive load Q1 NPN transistor

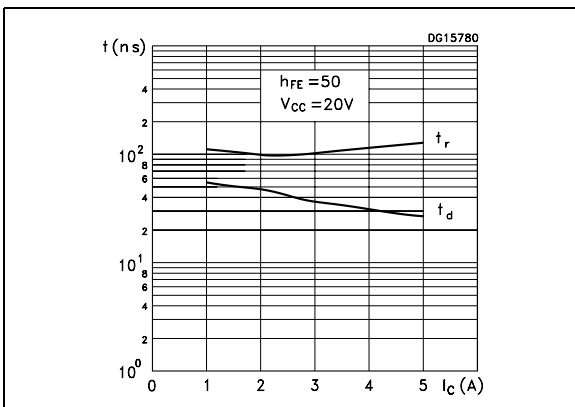


Figure 7. Switching time resistive load Q1 NPN transistor

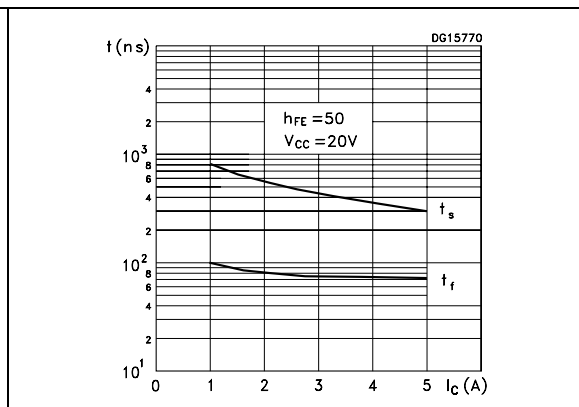


Figure 8. DC current gain Q2 PNP transistor Figure 9. DC current gain Q2 PNP transistor

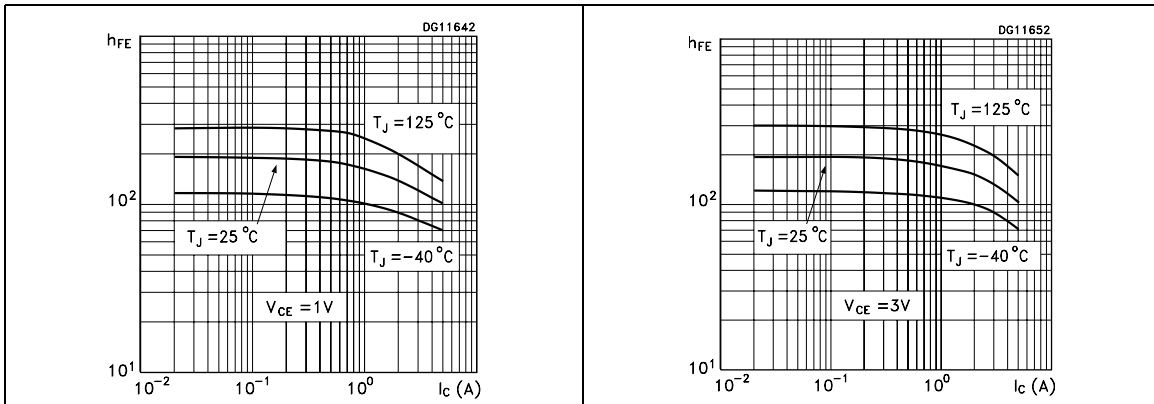


Figure 10. Collector-emitter saturation voltage Q2 PNP transistor

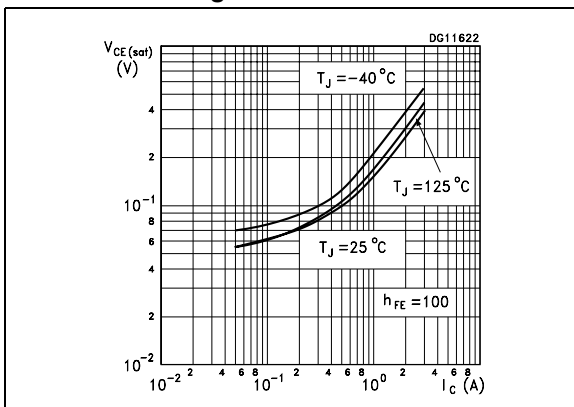


Figure 11. Base-emitter saturation voltage Q2 PNP transistor

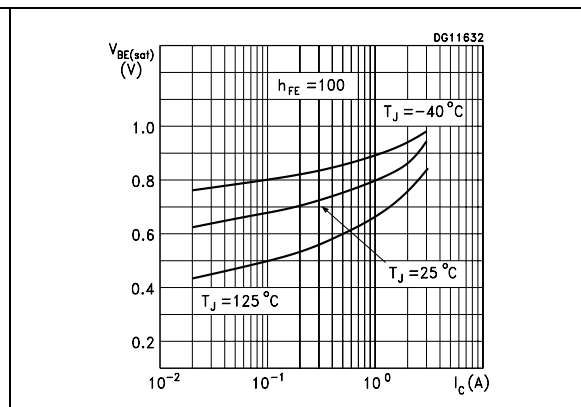


Figure 12. Switching time resistive load Q2 PNP transistor

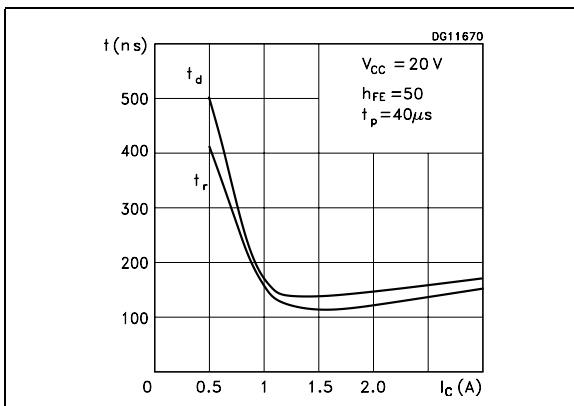
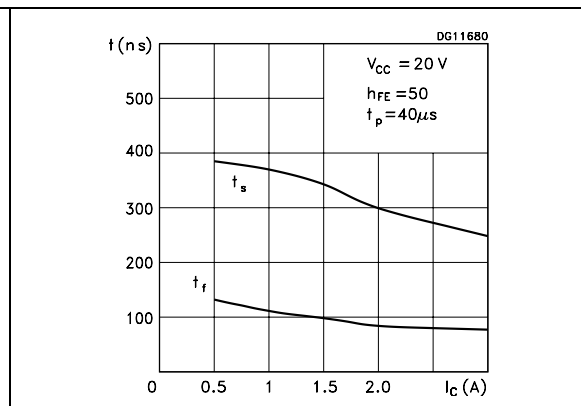


Figure 13. Switching time resistive load Q2 PNP transistor

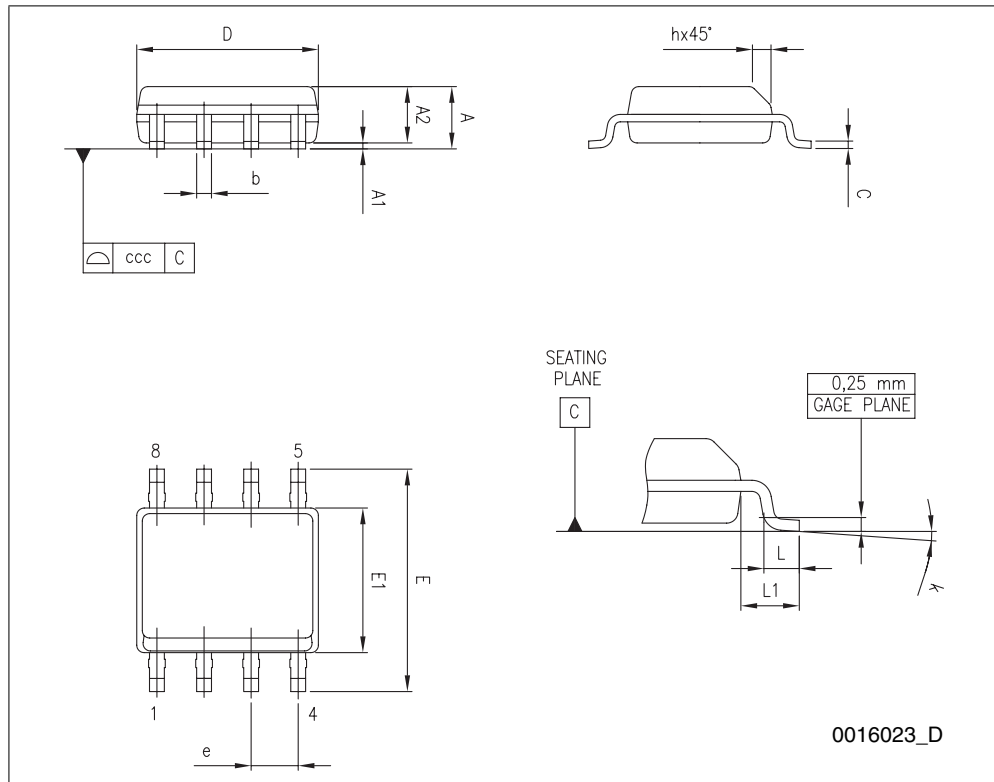


3 Package mechanical data

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ECOPACK is an ST trademark

SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10



4 Revision history

Table 6. Document revision history

Date	Revision	Changes
19-Mar-2009	1	First release

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