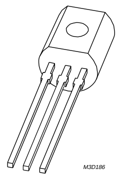


BT1306-400D/600D

Logic level triac

Rev. 01 — 19 February 2004 **Product data**

1. Product profile

1.1 Description

Logic level sensitive gate triac intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

1.2 Features

- Sensitive gate in all four quadrants
- Low cost package.

1.3 Applications

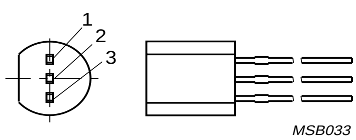
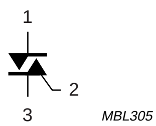
- General purpose bidirectional switching
- Phase control applications
- Solid state relays
- Low power AC fan speed controllers.

1.4 Quick reference data

- $V_{DRM} \leq 600$ V (BT1306-600D)
- $V_{DRM} \leq 400$ V (BT1306-400D)
- $I_{TSM} \leq 8$ A
- $I_{T(RMS)} \leq 0.6$ A.

2. Pinning information

Table 1: Pinning - SOT54 (TO-92), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	main terminal 2		
2	gate		
3	main terminal 1		
		SOT54 (TO-92)	

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BT1306-600D	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT1306-400D	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	BT1306-600D	25 °C ≤ T_j ≤ 125 °C	-	600	V
	BT1306-400D		-	400	V
$I_{T(RMS)}$	on-state current (RMS value)	full sine wave; T_{lead} ≤ 65 °C; Figure 1 and 2	-	0.6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; T_j = 25 °C prior to surge; Figure 3 and 4			
		t = 20 ms	-	8	A
		t = 16.7 ms	-	8.8	A
I^2t	I^2t for fusing	t = 10 ms	-	0.32	A^2s
dI_T/dt	repetitive rate of rise of on-state current after triggering	I_{TM} = 1 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs			
		T2+ G+	-	50	A/µs
		T2+ G–	-	50	A/µs
		T2– G–	-	50	A/µs
		T2– G+	-	10	A/µs
I_{GM}	gate current (peak value)	t = 2 µs max	-	1	A
V_{GM}	gate voltage (peak value)		-	5	V
P_{GM}	gate power (peak value)		-	5	W
$P_{G(AV)}$	average gate power	t = 2 µs max; T_{case} ≤ 80 °C	-	0.1	W
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		–40	+125	°C

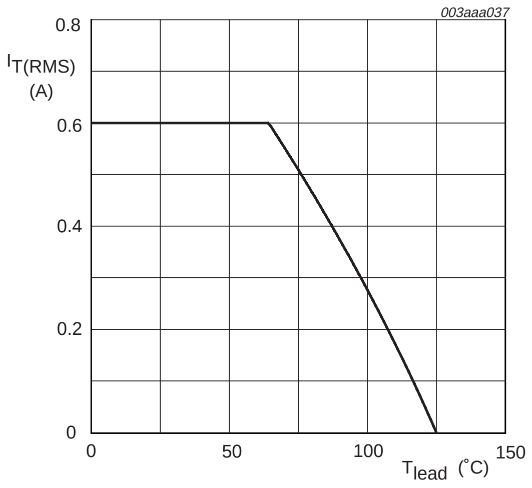
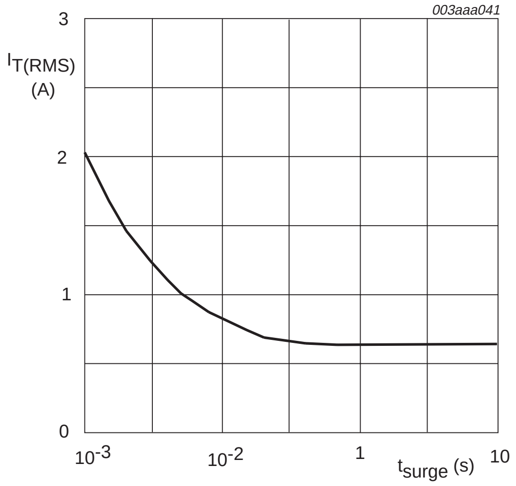


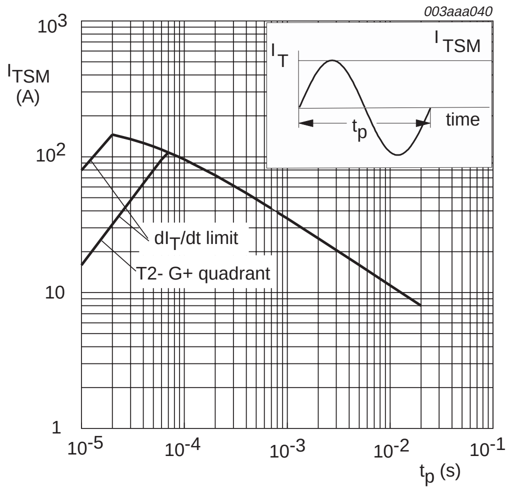
Fig 1. Maximum permissible on-state current (RMS value) as a function of lead temperature.



f = 50 Hz

$T_{lead} \leq 65$ °C

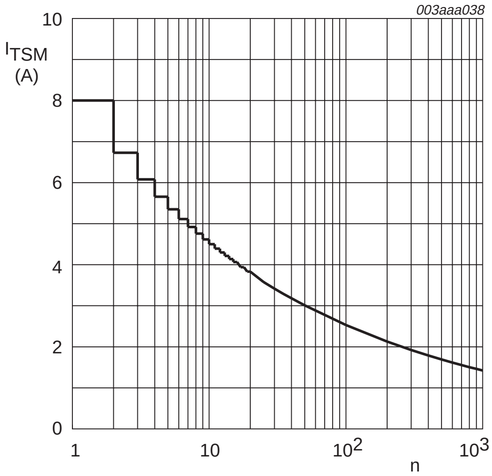
Fig 2. Maximum permissible repetitive on-state current (RMS value) as a function of surge duration for sinusoidal currents.



$t_p \leq 20$ ms

initial $T_j \leq 25$ °C

Fig 3. Maximum permissible non-repetitive peak on-state current as a function of pulse width for sinusoidal currents.



n = number of cycles

f = 50 Hz

initial $T_j \leq 25$ °C

Fig 4. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
		half cycle			80	
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; lead length = 4 mm; Figure 5	-	150	-	K/W

5.1 Transient thermal impedance

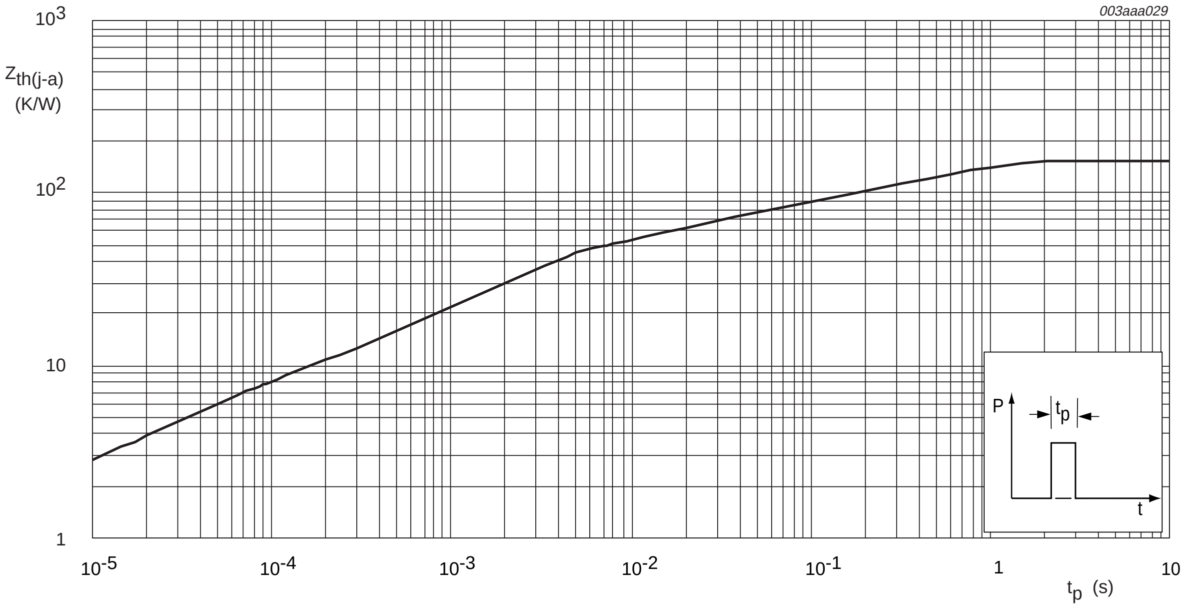


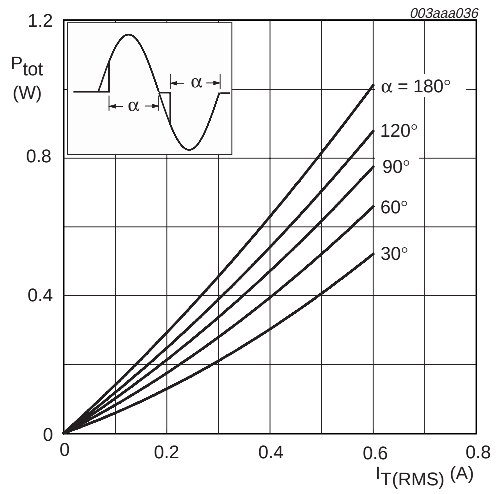
Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values.

6. Characteristics

Table 5: Characteristics

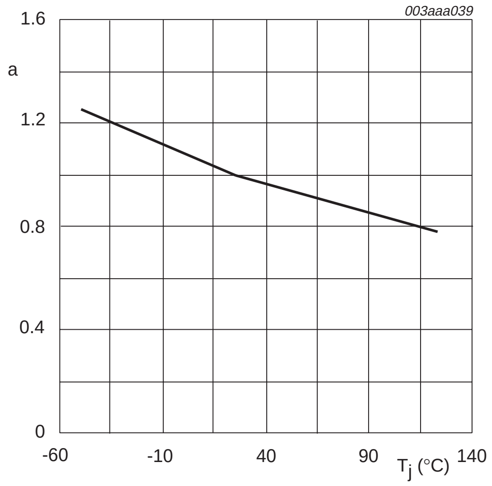
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; Figure 8				
		T2+ G+	-	1	5	mA
		T2+ G–	-	2	5	mA
		T2– G–	-	2	5	mA
		T2– G+	-	4	7	mA
I_L	latching current	V_D = 12 V; I_T = 0.1 A; Figure 9				
		T2+ G+	-	1	10	mA
		T2+ G–	-	5	10	mA
		T2– G–	-	1	10	mA
		T2– G+	-	2	10	mA
I_H	holding current	V_D = 12 V; I_{GT} = 0.1 A; Figure 10	-	1	10	mA
V_T	on-state voltage	I_T = 0.85 A; Figure 11	-	1.4	1.9	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; Figure 7	-	0.9	2	V
		$V_D = V_{DRM}$; I_T = 0.1 A; T_j = 110 °C	0.1	0.7	-	V
I_D	off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 110 °C	-	3	100	µA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	V_D = 67% of $V_{DM(max)}$; T_{case} = 110 °C; exponential waveform; gate open circuit; Figure 12	30	45	-	V/µs
dV_{com}/dt	critical rate of rise of commutation voltage	V_D = rated V_{DM}; T_{case} = 50 °C; I_{TM} = 0.84 A; commutating dI/dt = 0.3 A/ms	-	5	-	V/µs
t_{gt}	gate controlled turn-on time	I_{TM} = 1.0 A; $V_D = V_{DRM(max)}$; I_G = 25 mA; dI_G/dt = 5 A/µs	-	2	-	µs



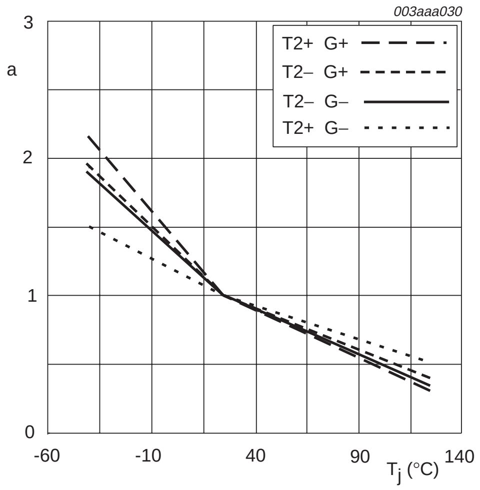
α = conduction angle

Fig 6. On-state dissipation as a function of on-state current (RMS value); maximum values.



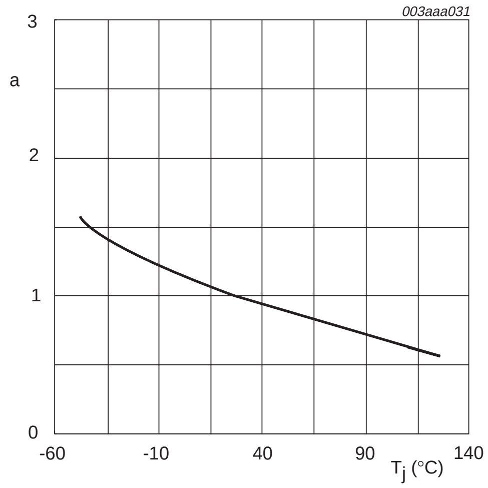
$$a = \frac{V_{GT(T_j)}}{V_{GT(25°C)}}$$

Fig 7. Normalized gate trigger voltage as a function of junction temperature; typical values.



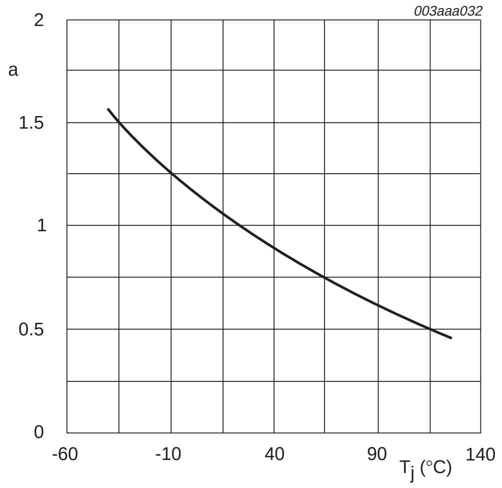
$$a = \frac{I_{GT(T_j)}}{I_{GT(25°C)}}$$

Fig 8. Normalized gate trigger current as a function of junction temperature; typical values.



$$a = \frac{I_{L(T_j)}}{I_{L(25°C)}}$$

Fig 9. Normalized latching current as a function of junction temperature; typical values.



$$a = \frac{I_{H(T_j)}}{I_{H(25°C)}}$$

Fig 10. Normalized holding current as a function of junction temperature; typical values

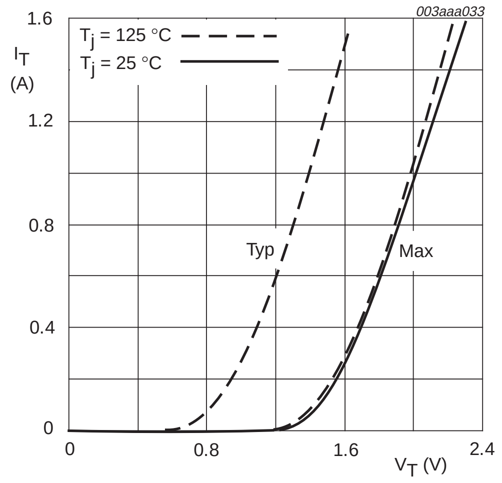


Fig 11. On-state current as a function of on-state voltage; typical and maximum values.

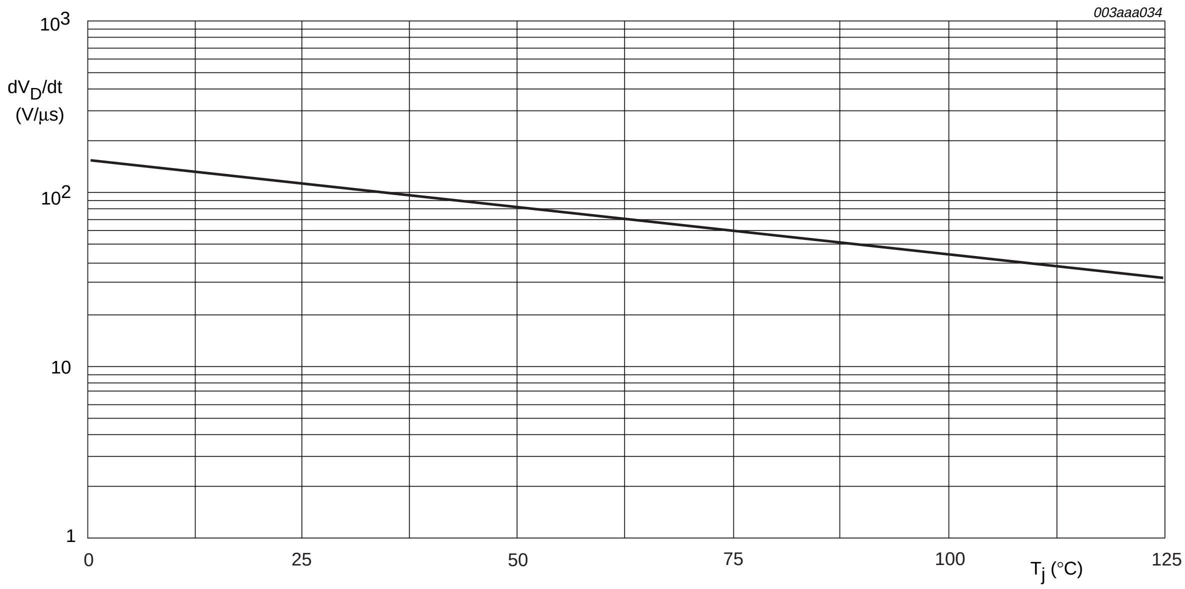
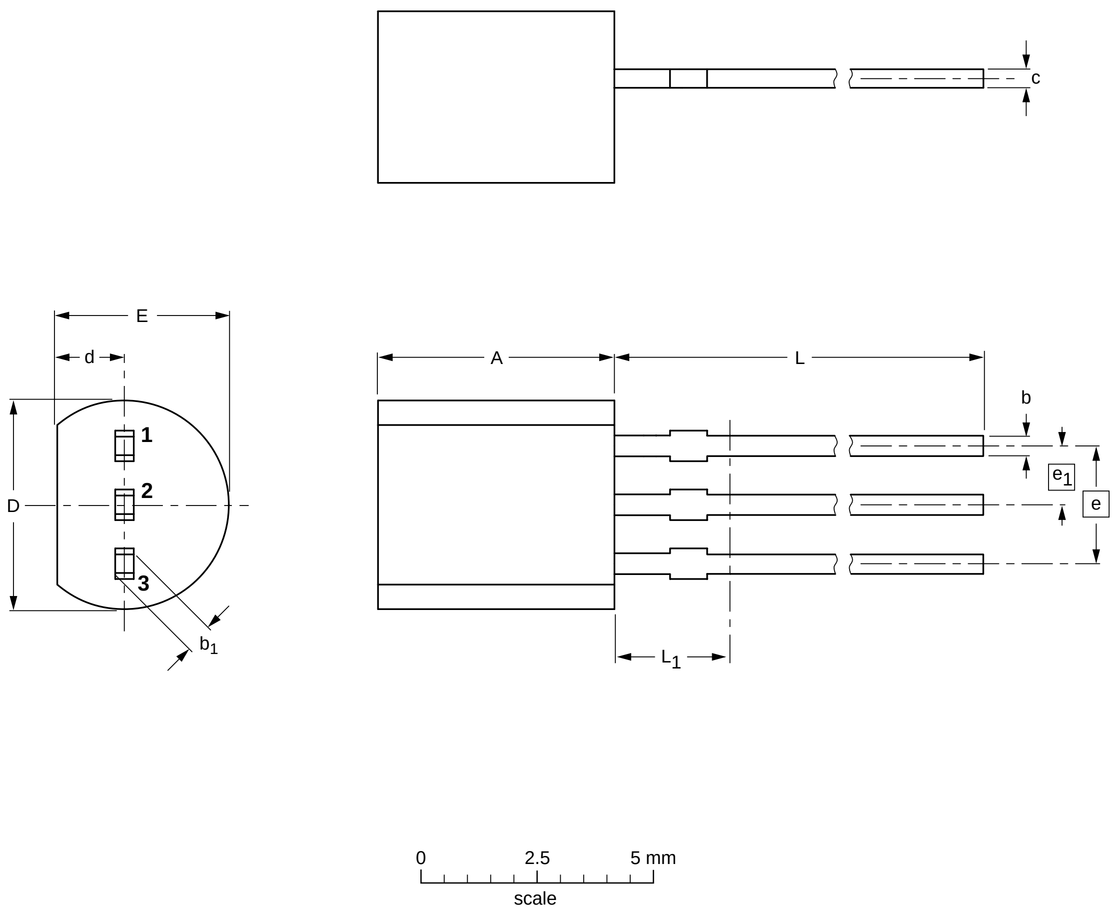


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values.

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Fig 13. SOT54 (TO-92).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040219	-	Product data (9397 750 12593)

9. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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