Si840x

Bidirectional I²C Isolators with Unidirectional Digital Channels

Features

- Independent, bidirectional SDA and SCL isolation channels
  - Open drain outputs with 35 mA sink current
  - Supports I²C clocks up to 1.7 MHz
- Unidirectional isolation channels support additional system signals (Si8405)
- Wide 3.0 to 5.0 V logic level compatibility
- UL, CSA, VDE recognition (pending)
- Operating temperature range –40 to +125 °C max
- Compact SO-8 and SO-16 narrow-body packages
- RoHS compliant

Applications

- Isolated I²C buses
- Power over Ethernet
- Motor Control Systems
- Hot-swap applications
- Intelligent Power systems
- Isolated SMPS systems with PMBus interfaces

Description

The Si840x series of isolators are single-package galvanic isolation solutions for I²C and SMBus serial port applications. These products are based on Silicon Labs proprietary RF isolation technology and offer shorter propagation delays, lower power consumption, smaller installed size, and more stable operation with temperature and age versus opto couplers or other digital isolators.

All devices in this family include hot-swap, bidirectional SDA and SCL isolation channels with open-drain, 35 mA sink capability that operate to a maximum frequency of 1.7 MHz. The 8-pin version (Si8400) supports bidirectional SDA and SCL isolation, while the 16-pin version (Si8405) features two unidirectional isolation channels to support additional system signals, such as an interrupt or reset. All versions contain protection circuits to guard against data errors when an unpowered device is inserted into a powered system.

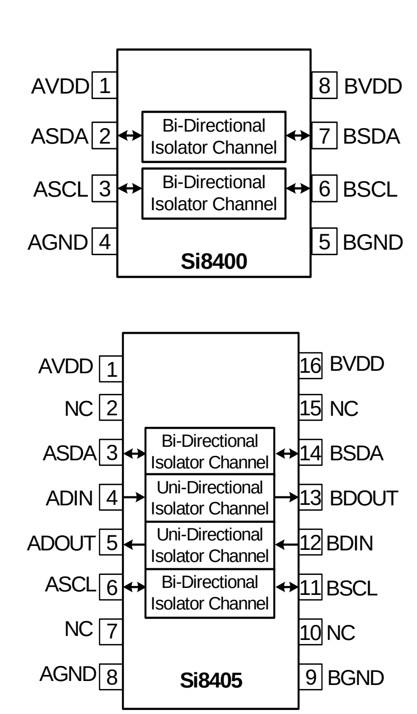
Small size, low installed cost, low power consumption, and short propagation delays make the Si840x family the optimum solution for isolating I²C and SMBus serial ports.

Safety Regulatory Approval

- UL 1577 recognized
  - 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950 approved
- VDE certification conformity*
  - IEC 60747-5-2 (VDE0884 Part 2)

***Note:** Pending. Regulatory information applies to 2.5 kV_{RMS} rated devices.

Pin Assignments



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3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
AVDD current 5 V	Idda	All I^2C inputs low	—	6	10	mA
BVDD current 5 V	Iddb	AVDD = 5 V	—	6	10	mA
AVDD current 3.3 V	Idda	BVDD = 5 V	—	6	10	mA
BVDD current 3.3 V	Iddb	AVDD = 3.3 V	—	6	10	mA
		BVDD = 3.3 V				
SCL and SDA Logic High Leakage	Isdaa, Isdab Iscla, Isclb	SDAA, SCLA = VSSA SDAB, SCLB = VSSB	—	2	10	µA
Logic Levels Side A						
Logic Input Threshold[3]	I^2CV_T (Side A)		510	—	760	mV
Logic Low Output Voltages	I^2CV_{OL} (Side A)	ISDAA = ISCLA = 2.5 mA	680	—	900	mV
		ISDAA = ISCLA = 0.5 mA	610	—	850	mV
Input/Output Logic Low Level Difference[4]	$I^2C\Delta V$ (Side A)		50	—	—	mV
Logic Levels Side B						
Logic Low Input Voltage	I^2CV_{IL} (Side B)		—	—	0.8	V
Logic High Input Voltage	I^2CV_{IH} (Side B)		2.0	—	—	V
Logic Low Output Voltage	I^2CV_{OL} (Side B)	ISCLB = 35 mA	—	—	400	mV
AC Specifications (measured at 1.40 V unless otherwise specified)						
Maximum I^2C bus Frequency	Fmax		—		1.7	MHz
Propagation Delay	Tphab	No bus capacitance	—	25	—	ns
5 V Operation	Tplab	R1 = 1400	—	36	—	ns
Side A to side B rising[5]	Tphba	R2 = 499	—	18	—	ns
Side A to side B falling[5]	Tplba	See Figure 2	—	15	—	ns
Side B to side A rising						
Side B to side A falling						
3.3 V Operation	Tphab		—	28	—	ns
Side A to side B rising[5]	Tplab	R1 = 806	—	34	—	ns
Side A to side B falling[5]	Tphba	R2 = 499	—	20	—	ns
Side B to side A rising	Tplba		—	16	—	ns
Side B to side A falling						

Notes:

1. Does not include current consumed by an isolated digital channel.
2. All voltages are relative to respective ground.
3. V_{IL} < 0.51 V, V_{IH} > 0.760 V.
4. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
5. Side A measured at 0.6 V.

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Table 1. Si840x Electrical Characteristics for Bidirectional I^2C Channels[1,2] (Continued)
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse width distortion 5 V Side A low to Side B low[5] Side B low to Side A low 3.3 V Side A low to Side B low[5] Side B low to Side A low	 PWDAB PWDBA PWDAB PWDBA	No bus capacitance, R1 = 1400 R2 = 499 See Figure 2 R1 = 806 R2 = 499	 — — — —	 –12 1 –8 4	 — — — —	 ns ns ns ns
Pin capacitance SDAA, SCLA, SDAB, SDBB	CA CB		— —	10 10	— —	pF pF

Notes:
1. Does not include current consumed by an isolated digital channel.
2. All voltages are relative to respective ground.
3. V_{IL} < 0.51 V, V_{IH} > 0.760 V.
4. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
5. Side A measured at 0.6 V.

Table 2. Electrical Characteristics for Unidirectional Non-I²C Digital Channels

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	AVDD, BVDD –0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O	V_{DD} = 5 V, 25 °C	—	50	—	Ω
DC Supply Current (All inputs 0 V or at Supply)[2]						
Si8405 AVDD		All inputs 0 DC	—	2	4	mA
Si8405 BVDD		All inputs 0 DC	—	2	4	mA
Si8405 AVDD		All inputs 1 DC	—	3	6	mA
Si8405 BVDD		All inputs 1 DC	—	3	6	mA
10 Mbps Supply Current (All inputs = 500 kHz square wave, C3 = 15 pF on all outputs)[2]						
Si8405 AVDD			—	3	5	mA
Si8405 BVDD			—	3	5	mA
Timing Characteristics						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	40	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	20	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	—	12	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	20	ns
Channel-Channel Skew	t_{PSK}		—	—	10	ns
Output Rise Time	t_r	C_3 = 15 pF See Figure 1 and Figure 2	—	2	4	ns
Output Fall Time	t_f	C_3 = 15 pF See Figure 1 and Figure 2	—	2	4	ns

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.
2. Does not include current for I²C channels. Assumes all isolated digital inputs are at same logic state.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Table 3. Electrical Characteristics for All I²C and Non-I²C Channels
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDD Undervoltage Threshold	VDDUV+	AVDD, BVDD rising	—	2.3	—	V
VDD Negative-going Lockout Hysteresis	VDDH–	AVDD, BVDD falling	—	75	—	mV
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	30	—	kV/µs
Shut Down Time from UVLO	t_{SD}		—	3	—	µs
Start-up Time*	t_{START}		—	15	40	µs
***Note:** Start-up time is the time period from the application of power to valid data at the output.						

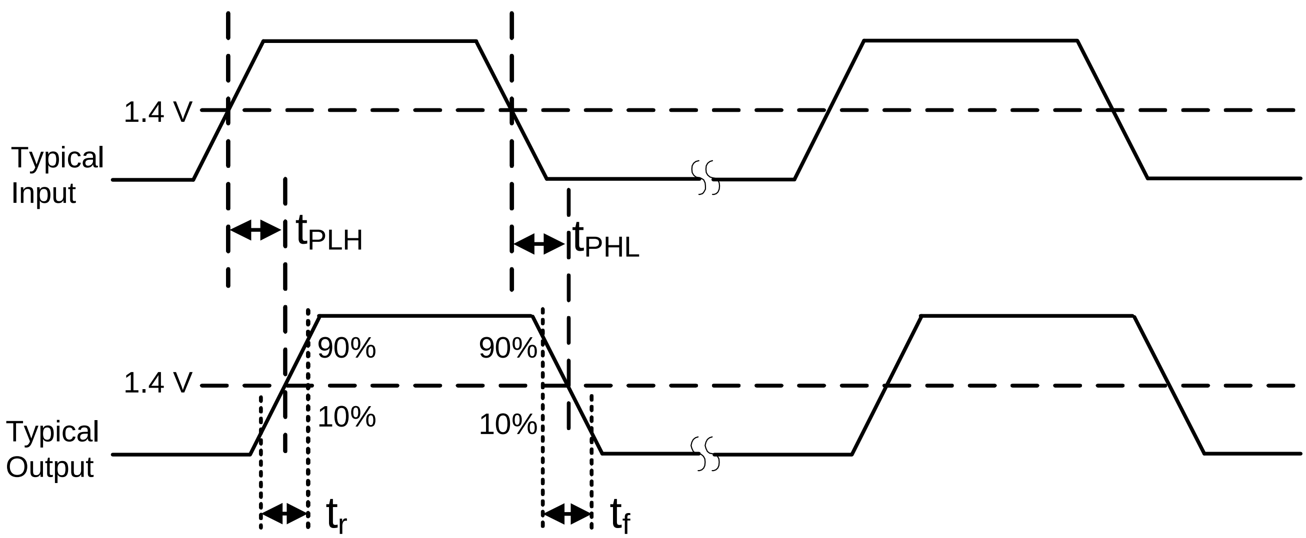

Figure 1. Propagation Delay Timing (Non-I²C Channels)

1.1. Test Circuits

Figure 2 depicts the timing test diagram.

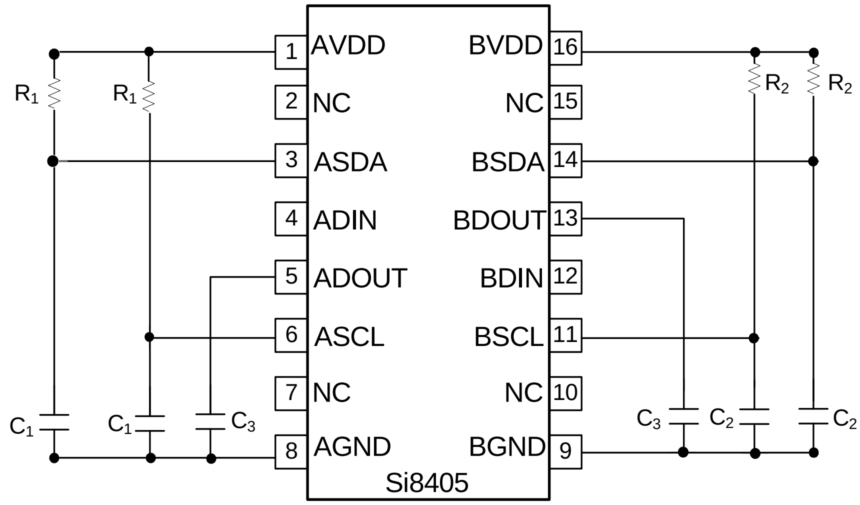

Figure 2. Simplified Timing Test Diagram

1.2. Typical Performance Characteristics

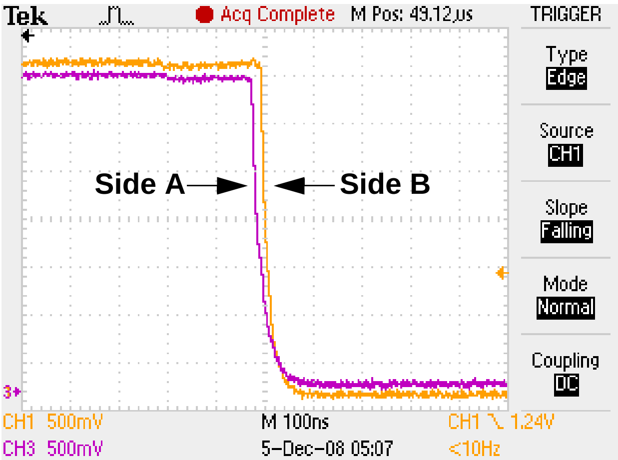

Figure 3. I^{2}C Side A Pulling Down (1100 Ω Pull-Up)

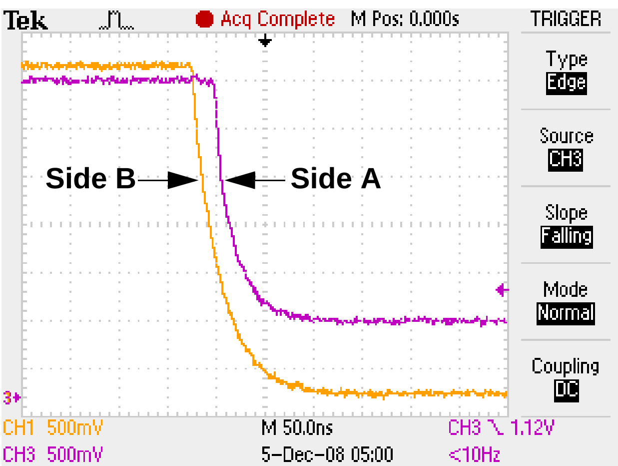

Figure 4. I^{2}C Side B Pulling Down

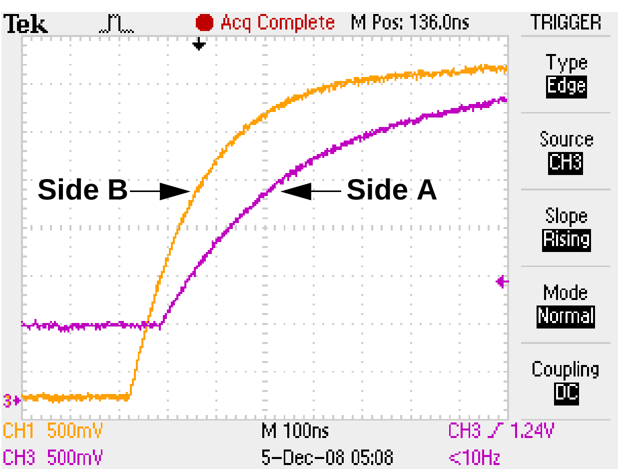

Figure 5. I^{2}C Side B Pulling Up, Side A Following

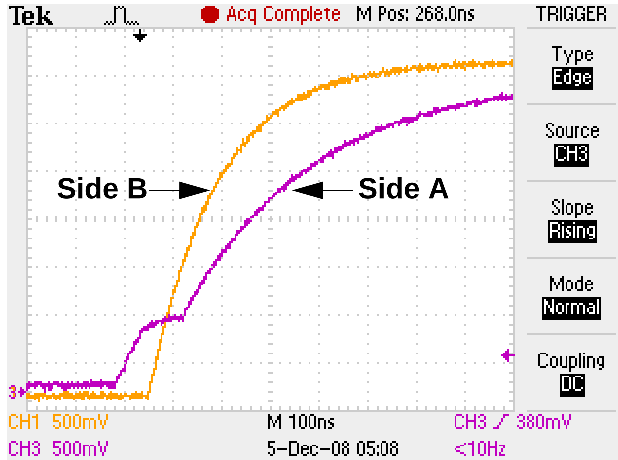

Figure 6. I^{2}C Side A Pulling Up, Side B Following

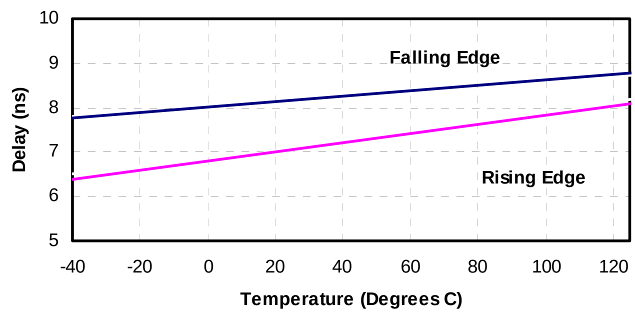

Figure 7. Non I^{2}C Channel Propagation Delay vs. Temperature

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Supply Voltage	V_{DD}	–0.5	—	5.75	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive (non-I^2C channels)	I_O	—	—	±10	mA
Side A output current drive (I^2C channels)	I_O	—	—	±15	mA
Side B output current drive (I^2C channels)	I_O	—	—	±75	mA
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.

Table 5. Regulatory Information[1]

CSA
The Si840x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE[2]
The Si840x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si840x is certified under UL1577 component recognition program. For more details, see File E257455.

Notes:

1. All 2.5 kV_{RMS} rated devices are production tested to ≥3.0 kV_{RMS} for 1 sec. For more information, see "8.Ordering Guide" on page 25.
2. Pending.

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Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-8	**NB SOIC-16**	
Minimum Air Gap (Clearance)	L(1O1)		3.9 min	3.9 min	mm
Minimum External Tracking (Creepage)	L(1O2)		3.9 min	3.9 min	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	>175	V
Resistance (Input-Output)[1]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1	2	pF
Input Capacitance[2]	C_I		4.0	4.0	pF

Notes:

1. To determine resistance and capacitance, the Si840x, SO-16, is converted into a 2-terminal device. Pins 1–8 (1-4, SO-8) are shorted together to form the first terminal and pins 9–16 (5–8, SO-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 7. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic Isolation Group	Material Group	IIIa
Installation Classification	Rated Mains Voltages $\leq$ 150 V_{RMS}	I-IV
	Rated Mains Voltages $\leq$ 300 V_{RMS}	I-III
	Rated Mains Voltages $\leq$ 400 V_{RMS}	I-II

Table 8. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	896	V peak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** The Si840x is suitable for basic electrical isolation within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si840x provides a climate classification of 40/125/21.

Table 9. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
Case Temperature	T_S		150	150	°C
Safety Input Current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), 140 °C/W (NB SOIC-8) AVDD, BVDD = 5.5 V, T_J = 150 °C, T_A = 25 °C	160	210	mA
Device Power Dissipation[2]	P_D		220	275	W

Notes:

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 8 and Figure 9.
2. The Si840x is tested with AVDD, BVDD = 5.5 V; T_J = 150 ºC; C_1, C_2 = 0.1 µF; C_3 = 15 pF; R1, R2 = 3kΩ; input 1 MHz 50% duty cycle square wave.

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		140	105	°C/W

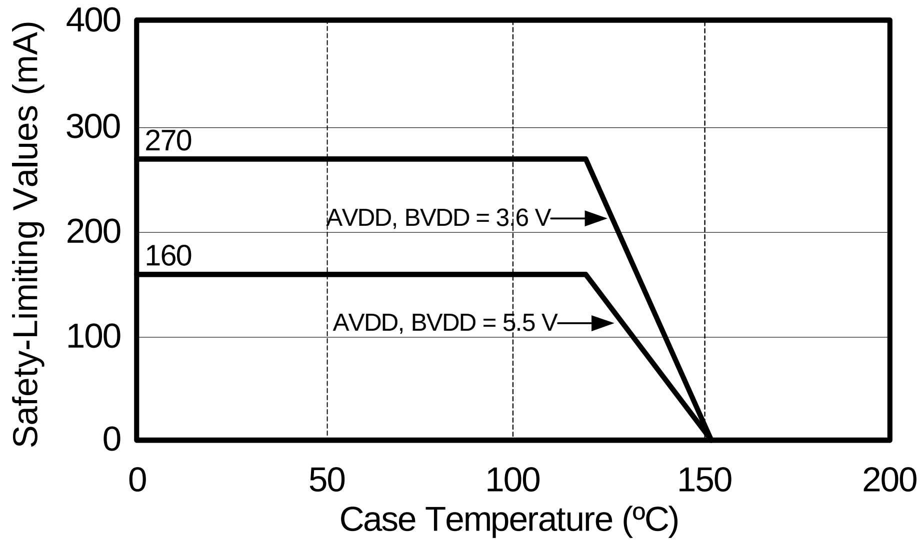

Figure 8. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

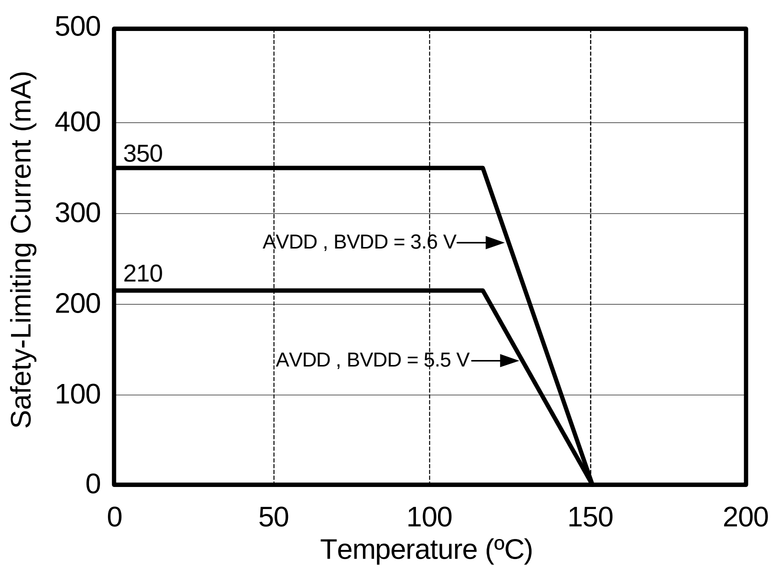

Figure 9. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Overview

2.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single unidirectional Si84xx channel is shown in Figure 10.

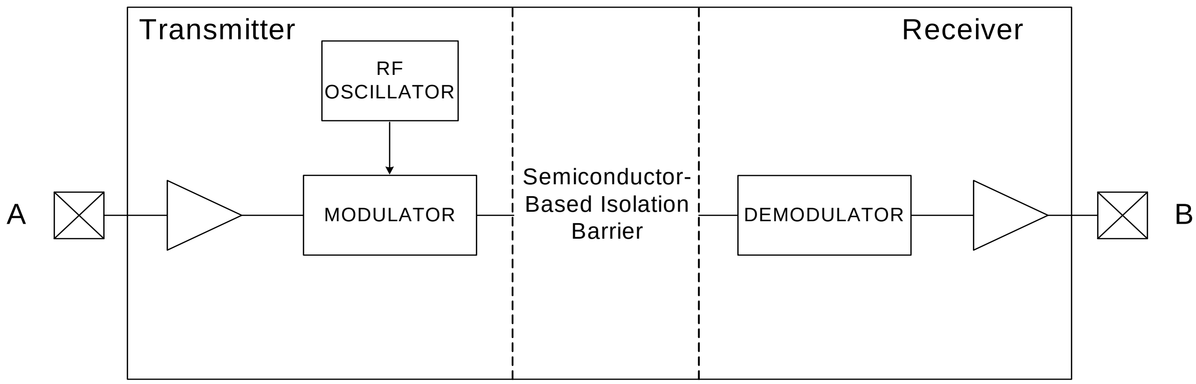

Figure 10. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 11 for more details.

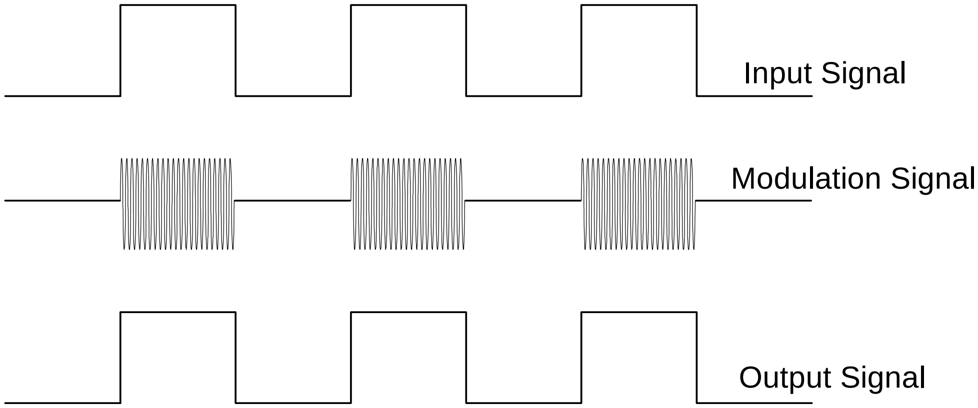

Figure 11. Modulation Scheme

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 12, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 11 to determine outputs when power supply (VDD) is not present.

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own under voltage lockout monitors. The Si840x Side A enters UVLO when AVDD < V_{AUVH}–, and exits UVLO when AVDD > AVDDUV+. Side B operates the same as Side A with respect to its BVDD supply. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when AVDD falls below AVDDUV– and exits UVLO when AVDDA rises above $AVDD_{UV+}$.

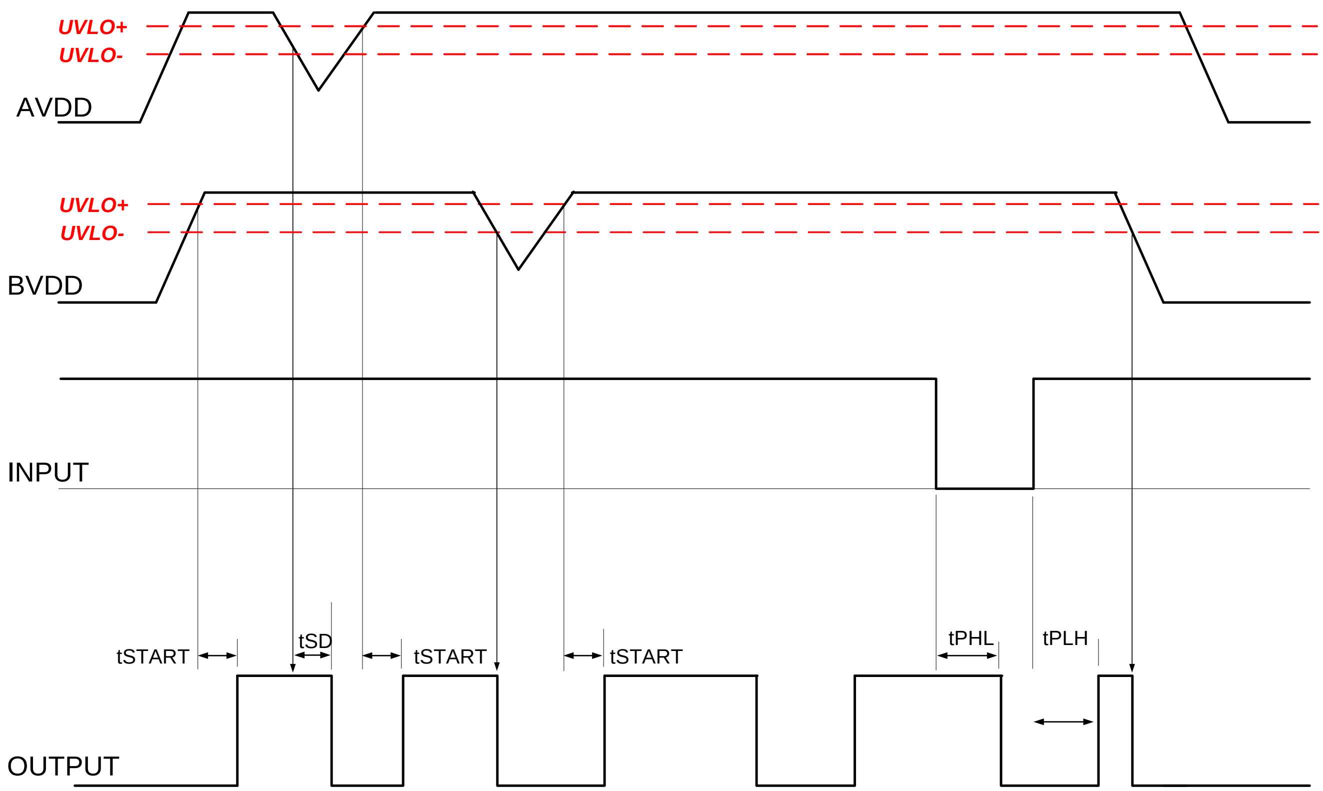

Figure 12. Device Behavior during Normal Operation

3.3. Input and Output Characteristics for Non-I²C Digital Channels

The Si84xx inputs and outputs are standard CMOS drivers/receivers. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces. Table 11 details powered and unpowered operation of the Si84xx's non-I²C digital channels.

Table 11. Si84xx Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 3.0 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.

4. Layout Recommendations

Dielectric isolation is a set of specifications produced by safety regulatory agencies from around the world, which describes the physical construction of electrical equipment that derives power from high-voltage power systems, such as 100–240 V_{AC} systems or industrial power. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user-touchable surfaces of the product. For the IEC relating to products deriving their power from the 220–240 V power grids, the test voltage is 2500 V_{AC} (or 3750 V_{DC}, the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the shortest distance through air that an arc may travel.

Figure 13 illustrates the accepted method of providing the proper creepage distance along the surface. For a 120 V_{AC} application, this distance is 3.2 mm, and the narrow-body SOIC package can be used. For a 220–240 V_{AC} application, this distance is 6.4 mm, and a wide-body SOIC package must be used. There must be no copper traces within this 3.2 or 6.4 mm exclusion area, and the surface should have a conformal coating, such as solder resist. The digital isolator chip must straddle this exclusion area.

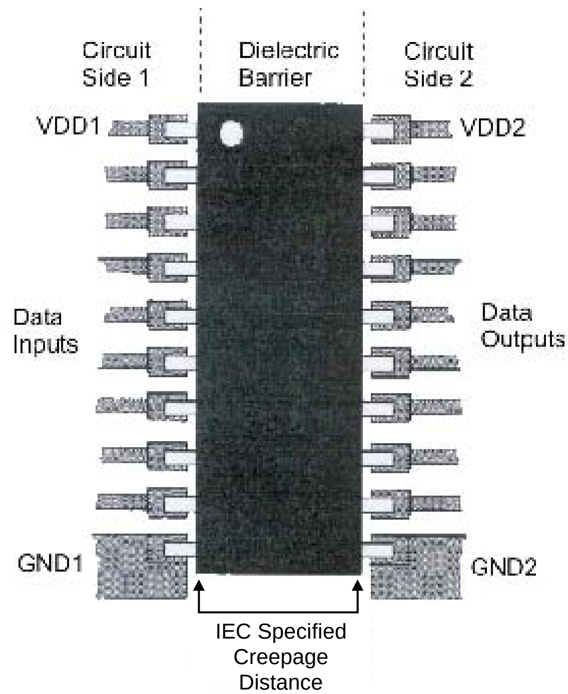

Figure 13. Creepage Distance

4.1. Supply Bypass

The Si84xx families require a 1 µF bypass capacitor between AVDD and AGND and BVDD and BGND. The capacitor should be placed as close as possible to the package. See "6.Errata and Design Migration Guidelines" on page 22 for more details.

4.2. RF Radiated Emissions

The Si84xx families use an RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si84xx evaluation board passes FCC Class B (Part 15) requirements. Table 12 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions, where all inputs tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 12. Radiated Emissions

Frequency (MHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
712	29	37	–8
1424	39	54	–15
2136	42	54	–12
2848	43	54	–11
4272	44	54	–10
4984	44	54	–10
5696	44	54	–10

4.3. RF, Magnetic, and Common Mode Transient Immunity

The Si84xx families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 30 kV/µs (typical). During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si84xx families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 14, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si840x digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si84xx devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.

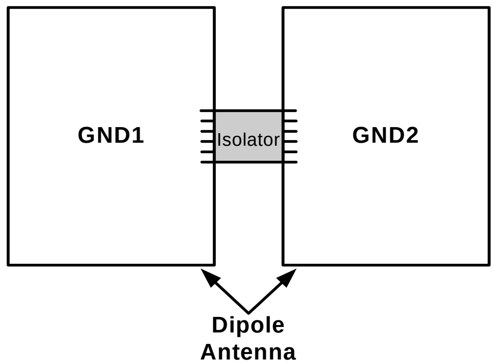

Figure 14. Dipole Antenna

5. Typical Application Overview

5.1. I^2C Background

In many applications, I^2C, SMBus, and PMBus interfaces require galvanic isolation for safety or ground loop elimination. For example, Power over Ethernet (PoE) applications typically use an I^2C interface for communication between the PoE power sourcing device (PSE), and the earth ground referenced system controller. Galvanic isolation is required both by standard and also as a practical matter to prevent ground loops in Ethernet connected equipment.

The physical interface consists of two wires: serial data (SDA) and serial clock (SCL). These wires are connected to open collector drivers that serve as both inputs and outputs. At first glance, it appears that SDA and SCL can be isolated simply by placing two unidirectional isolators in parallel, and in opposite directions. However, this technique creates feedback that latches the bus line low when a logic low asserted by either master or slave. This problem can be remedied by adding anti-latch circuits, but results in a larger and more expensive solution. The Si840x products offer a single-chip, anti-latch solution to the problem of isolating I^2C/SMBus applications and require no external components except the I^2C/SMBus pull-up resistors. In addition, they provide isolation to a maximum of 2.5 kV_{RMS}, support I^2C clock stretching, and operate to a maximum I^2C bus speed of 1.7 Mbps.

5.2. I^2C Isolator Operation

Without anti-latch protection, bidirectional I^2C isolators latch when an isolator output logic low propagates back through an adjacent isolator channel creating a stable latched low condition on both sides. Anti-latch protection is typically added to one side of the isolator to avoid this condition (the "A" side for the Si8400/05).

The following examples illustrate typical circuit configurations using the Si8405.

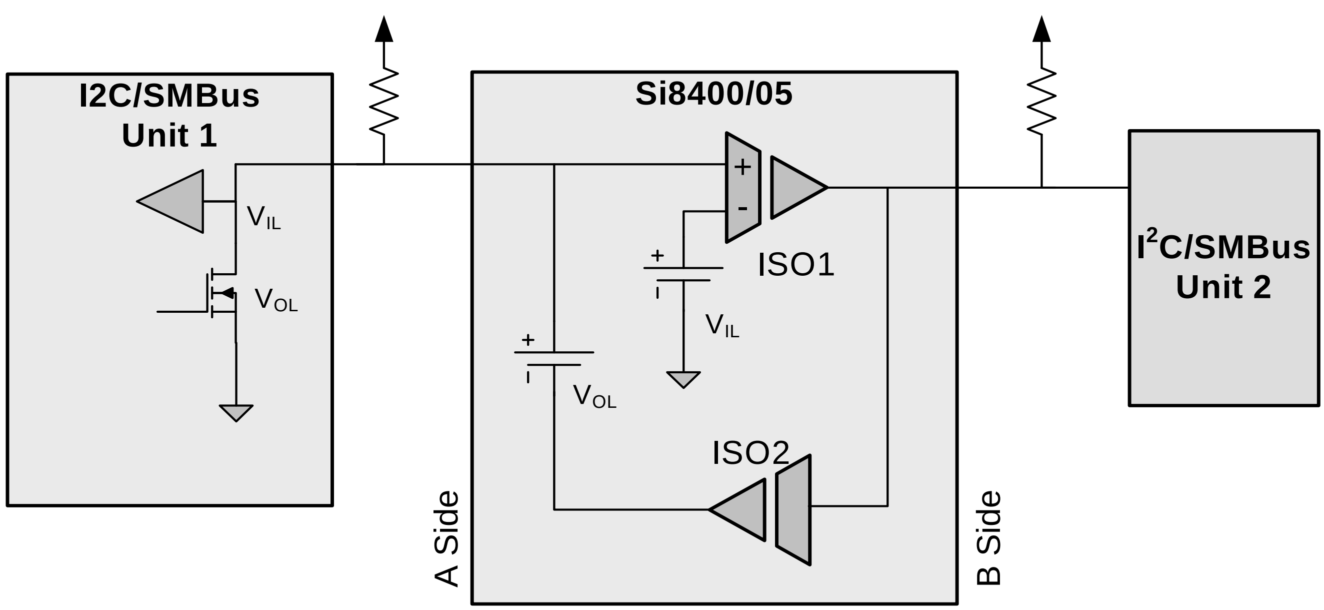

Figure 15. Isolated Bus Overview

The "A side" output low (V_{OL}) and input low (V_{IL}) levels are designed such that the isolator V_{OL} is greater than the isolator V_{IL} to prevent the latch condition.

5.3. I^2C Isolator Design Constraints

Table 13 lists the design constraints.

Table 13. Design Constraints

Design Constraint	Data Sheet Values	Effect of Bus Pull-up Strength and Temperature
To prevent the latch condition, the isolator output low level must be greater than the isolator input high level.	Isolator V_{OL} 0.8 V typical Isolator V_{IL} 0.6 V typical Input/Output Logic Low Level Difference ΔVSDA1, ΔVSCL1 = 50 mV minimum	This is normally guaranteed by the isolator data sheet. However, if the pull up strength is too weak, the output low voltage will fall and can get too close to the input low logic level. These track over temperature.
The bus output low must be less than the isolator input low logic level.	Bus V_{OL} = 0.4 V maximum Isolator V_{IL} = 0.545 V minimum	If the pull up strength is too large, the devices on the bus might not pull the voltage below the input low range. These have opposite temperature coefficients. Worst case is hot temperature.
The isolator output low must be greater than the bus input low.	Bus V_{IL} 0.3 x V_{DD} = 1.0 V minimum for V_{DD} = 3.3 V Isolator V_{OL} = 0.9 V maximum	If the pull up strength is too large, the isolator might not pull below the bus input low voltage. Si8400/05 Vol: –1.8 mV/C CMOS buffer: –0.6 mV/C This provides some temperature tracking, but worst case is cold temperature.

5.4. I^2C Isolator Design Considerations

The first step in applying an I^2C isolator is to choose which side of the bus will be connected to the isolator A side. Ideally, it should be the side which:

1. Is compatible with the range of bus pull up specified by the manufacturer. For example, the Si8400/05 isolators are normally used with a pull up of 0.5 mA to 3 mA.
2. Has the highest input low level for devices on the bus. Some devices may specify an input low of 0.8 V and other devices might require an input low of 0.3 x Vdd. Assuming a 3.3 V minimum power supply, the side with an input low of 0.3 x Vdd is the better side because this side has an input low level of 1.0 V.
3. Have devices on the bus that can pull down below the isolator input low level. For example, the Si840x input level is 0.545 V. As most CMOS devices can pull to within 0.4 V of GND this is generally not an issue.
4. Has the lowest noise. Due to the special logic levels, noise margins can be as low as 50 mV.

Although I^2C isolators typically have an output low of 0.9 V, it is still possible to connect the isolator A side to a bus having a standard TTL logic low level of 0.8 V. In this case, use the lowest recommended bus pull-up. In this case, the Si8400/05 input low level will be reduced from 0.9 V maximum to 0.83 V maximum. It is important to take into account the input level negative temperature coefficient to ensure adequate noise margin. For example, if the bus device is specified for a maximum input low level of 0.8 V at 85 °C, the typical –0.6 mV/C temperature coefficient means that at –40 °C the input level will be 0.875 V minimum. This results in a noise margin of 45 mV.

Figure 16 illustrates a typical circuit configuration using the Si8405.

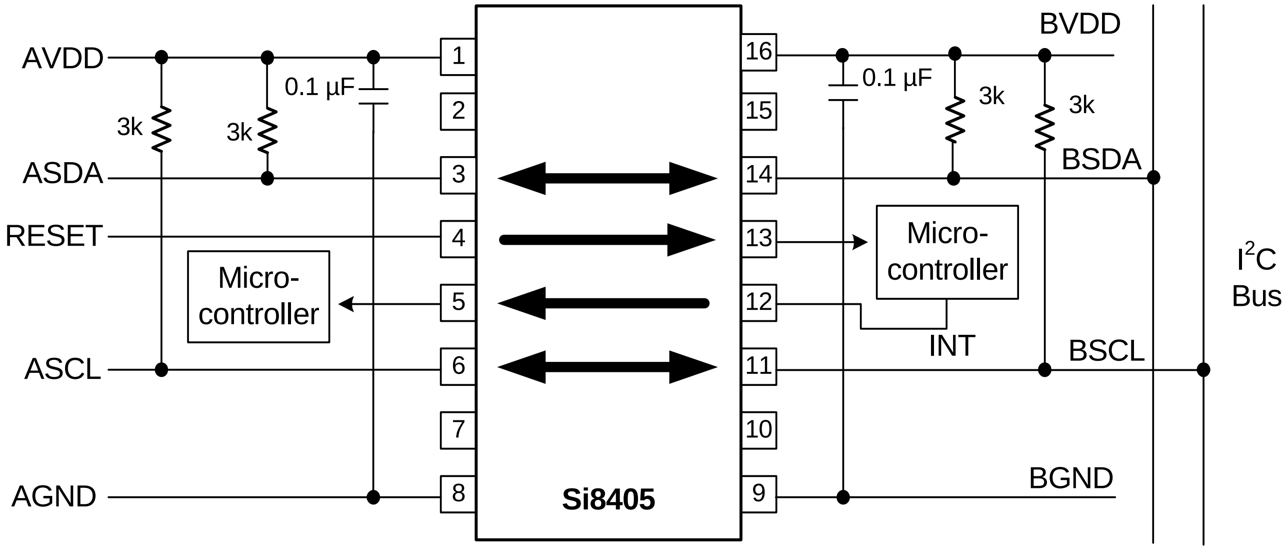

Figure 16. Typical Application Diagram

6. Errata and Design Migration Guidelines

When using the new ISOpro products, or when migrating from Silicon Labs' legacy isolators, designers must consider and adhere to the following requirements.

6.1. Power Supply Bypass Capacitors

When using the ISOpro isolators with power supplies $\geq$ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a $\geq$ 4.5 V supply). Although rise time is power supply dependent, $\geq$ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

6.1.1. Resolution

This issue will be eliminated in a future revision of the device. Refer to "8.Ordering Guide" on page 25 for current ordering information.

7. Pin Descriptions

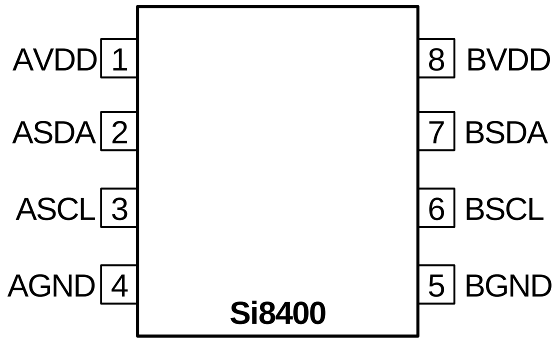

Table 14. Si8400 in SO-8 Package

Pin	Name	Description
1	AVDD	Side A power supply terminal; connect to a source of 3.0 to 5.5 V.
2	ASDA	Side A data input or output.
3	ASCL	Side A clock input or output.
4	AGND	Side A ground terminal.
5	BGND	Side B ground terminal.
6	BSCL	Side B clock input or output.
7	BSDA	Side B data input or output.
8	BVDD	Side B power supply terminal; connect to a source of 3.0 to 5.5 V.

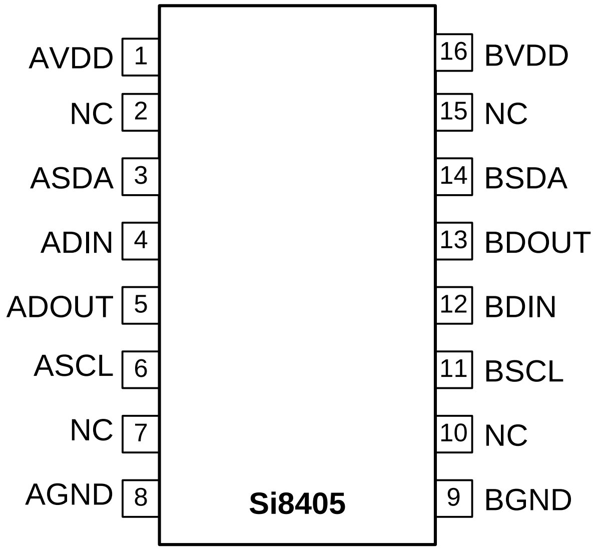

Table 15. Si8405 in Narrow-Body SO-16 Package

Pin	Name	Description
1	AVDD	Side A Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.
2	NC	No connection.
3	ASDA	Side A Data Input or Output.
4	ADIN	Side A Digital Input (non I^2C).
5	ADOUT	Side A Digital Output (non I^2C).
6	ASCL	Side A Clock Input or Output.
7	NC	No connection.
8	AGND	Side A Ground Terminal.
9	BGND	Side B Ground Terminal.
10	NC	No connection.
11	BSCL	Side B Clock Input or Output.
12	BDIN	Side B Digital Input (non I^2C).
13	BDOUT	Side B Digital Output (non I^2C).
14	BSDA	Side B Data Input or Output.
15	NC	No connection.
16	BVDD	Side B Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.

8. Ordering Guide

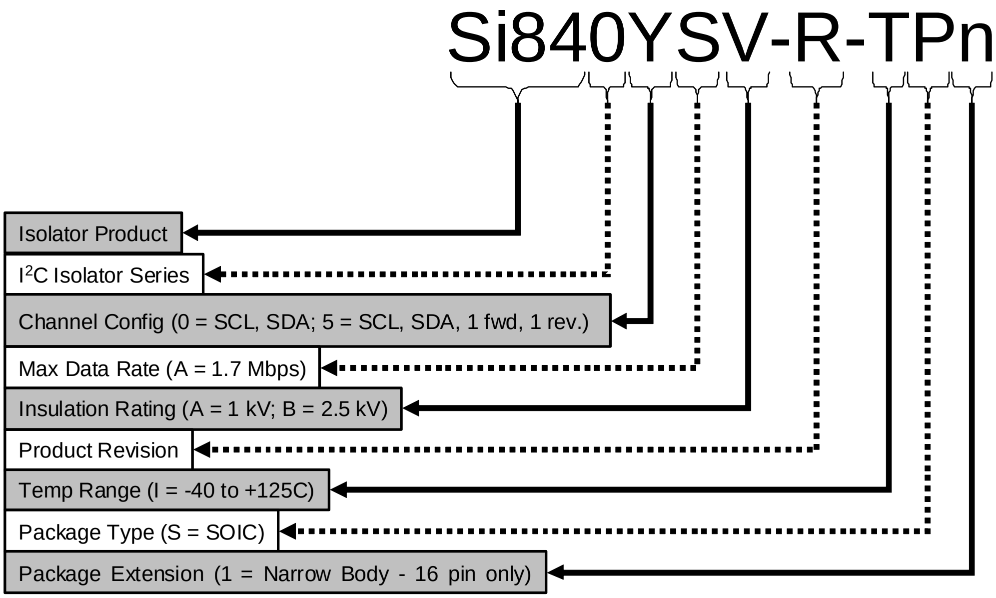

Figure 17. Naming Convention

Table 16. Ordering Guide

Ordering Part Number	Number of Bidirectional I^{2}C Channels	Max I^{2}C Bus Speed (MHz)	Number of Unidirectional Channels	Max Data Rate of Non-I^{2}C Unidirectional Channels (Mbps)	Isolation Ratings	Temp Range (°C)	Package
Si8400AA-A-IS	2	1.7	0	—	1 kV_{RMS}	–40 to 125	NB SOIC-8
Si8400AB-A-IS	2	1.7	0	—	2.5 kV_{RMS}	–40 to 125	NB SOIC-8
Si8405AA-A-IS1	2	1.7	1 forward 1 reverse	10	1 kV_{RMS}	–40 to 125	NB SOIC-16
Si8405AB-A-IS1	2	1.7	1 forward 1 reverse	10	2.5 kV_{RMS}	–40 to 125	NB SOIC-16

9. Package Outline: 8-Pin Narrow Body SOIC

Figure 18 illustrates the package details for the Si840x in an 8-pin SOIC (SO-8). Table 17 lists the values for the dimensions shown in the illustration. All packages are Pb-free and RoHS compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry classification and peak solder temperature.

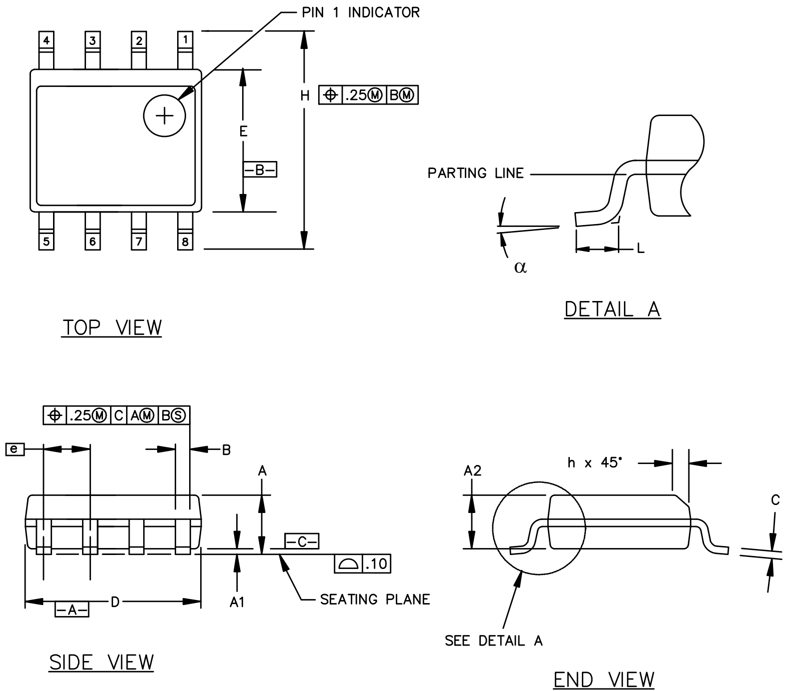

Figure 18. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 17. Package Diagram Dimensions

Symbol	Millimeters	
	Min	**Max**
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

10. Landing Pattern: 8-Pin Narrow Body SOIC

Figure 19 illustrates the recommended landing pattern details for the Si840x in an 8-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

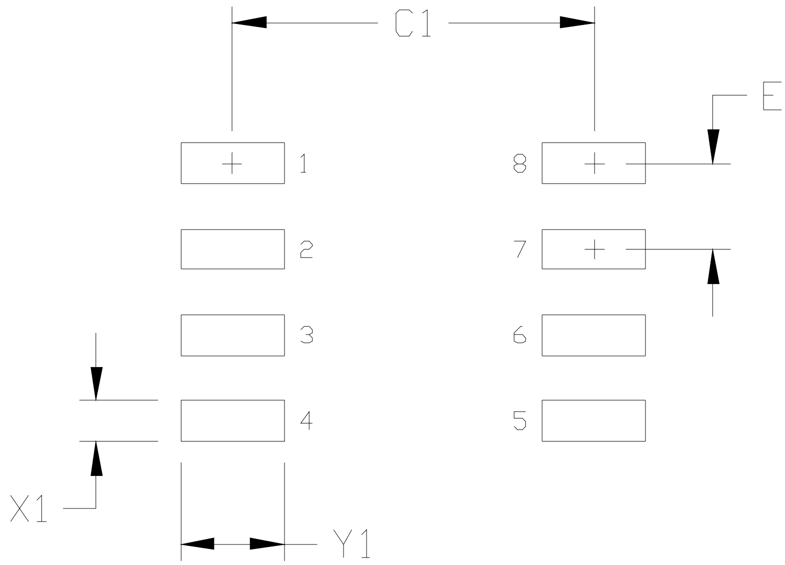

Figure 19. PCB Landing Pattern: 8-Pin Narrow Body SOIC

Table 18. PCM Landing Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Package Outline: 16-Pin Narrow Body SOIC

Figure 20 illustrates the package details for the Si840x in a 16-pin narrow-body SOIC (SO-16). Table 19 lists the values for the dimensions shown in the illustration. All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry classification and peak solder temperature.

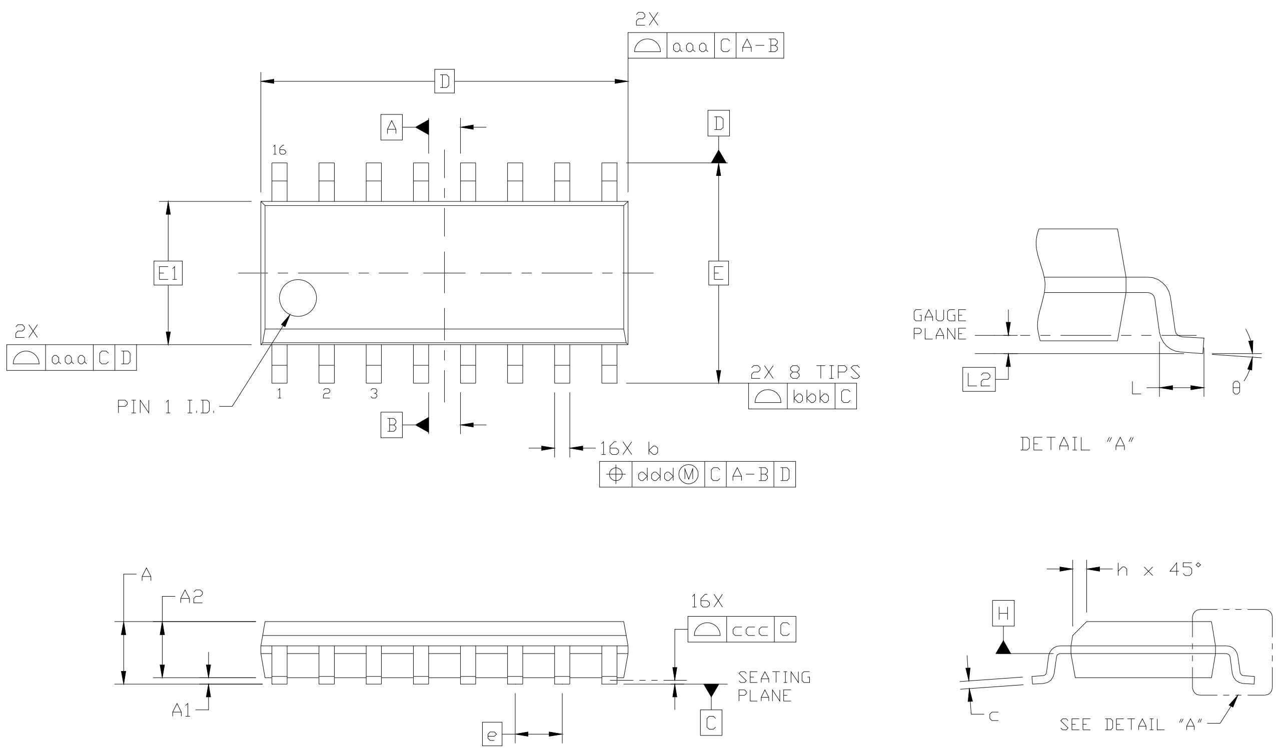

Figure 20. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 19. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27

Table 19. Package Diagram Dimensions (Continued)

Dimension	Min	Max
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Landing Pattern: 16-Pin Narrow Body SOIC

Figure 21 illustrates the recommended landing pattern details for the Si840x in a 16-pin narrow-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

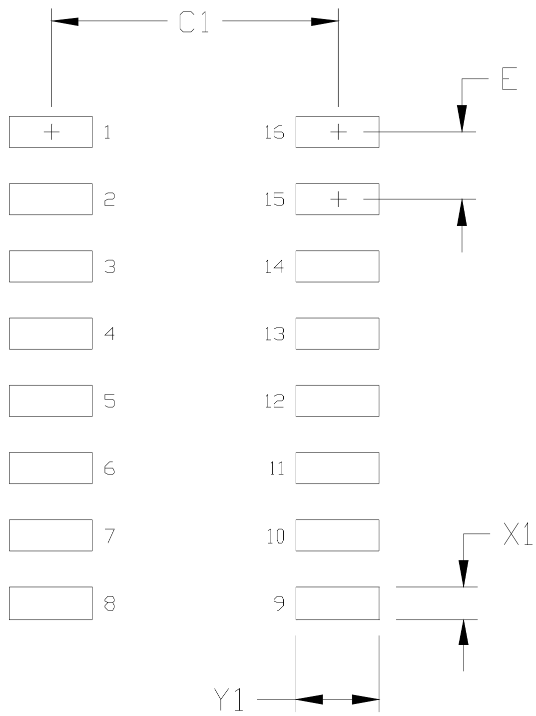

Figure 21. 16-Pin Narrow Body SOIC PCB Landing Pattern

Table 20. 16-Pin Narrow Body SOIC Landing Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

13. Top Marking: 8-Pin Narrow Body SOIC

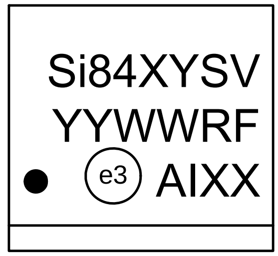

Figure 22. 8-Pin Narrow Body SOIC Top Marking

Table 21. 8-Pin Narrow Body SOIC Top Marking Table

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator I^2C Product Series: ■ XY = Channel Configuration • 00 = Bidirectional SCL and SDA channels ■ S = Speed Grade • A = 1.7 Mbps ■ V = Isolation rating • A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Work week	Assigned by assembly contractor. Corresponds to the year and work week of the mold date.
	R = Product Rev F = Wafer Fab	First two characters of the manufacturing code from Assembly.
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	“e3” Pb-Free Symbol
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code from assembly.

14. Top Marking: 16-Pin Narrow Body SOIC

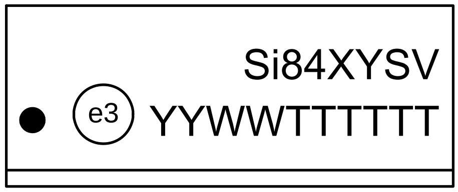

Figure 23. 16-Pin Narrow Body SOIC Top Marking

Table 22. 16-Pin Narrow Body SOIC Top Marking Table

Line 1 Marking:	Base Part Number Ordering Options	Si84 = Isolator product series ■ XY = Channel Configuration • 05 = Bidirectional SCL, SDA; 1- forward and 1-reverse unidirectional channel ■ S = Speed Grade • A = 1.7 Mbps ■ V = Isolation rating • A = 1 kV; B = 2.5 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	"e3" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	"e3" Pb-Free Symbol.

NOTES:

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