0.5 AND 4.0 A ISODRIVERS

Features

- Two completely isolated drivers in one package
  - 2.5 kV_{RMS} output-to-input differential voltage
  - 600 VDC peak driver-to-driver differential voltage
  - HS/LS and dual LS versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2), 4.0 A peak output (Si8233/4/5)
- Independent HS and LS inputs or PWM input versions
- Common-mode transient immunity >35 kV/µs
- Overlap protection and programmable dead time (Si8230/1/3/4)
- Operating temperature range –40 to +125 °C
- UL/VDE/CSA approval (pending)

Applications

- Power delivery systems
- Motor control systems
- Lighting control systems
- Plasma displays

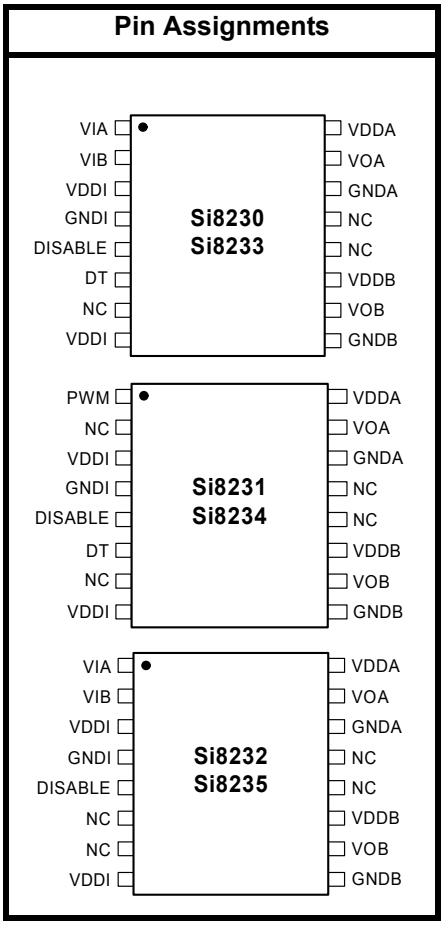
Description

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, and the Si8232/5 are dual low-side drivers. Versions with peak output currents of 0.5 A (Si8230/1/2) and 4.0 A (Si8233/4/5) are available. All drivers operate with a maximum supply voltage of 24 V.

These drivers utilize Silicon Labs' proprietary silicon isolation technology, which provides 600 V dc (2.5 kV_{acRMS}) withstand voltage per UL1577, and fast 50 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs are available in individual control input (Si8230/2/3/5) or PWM input (Si8231/4) configurations.

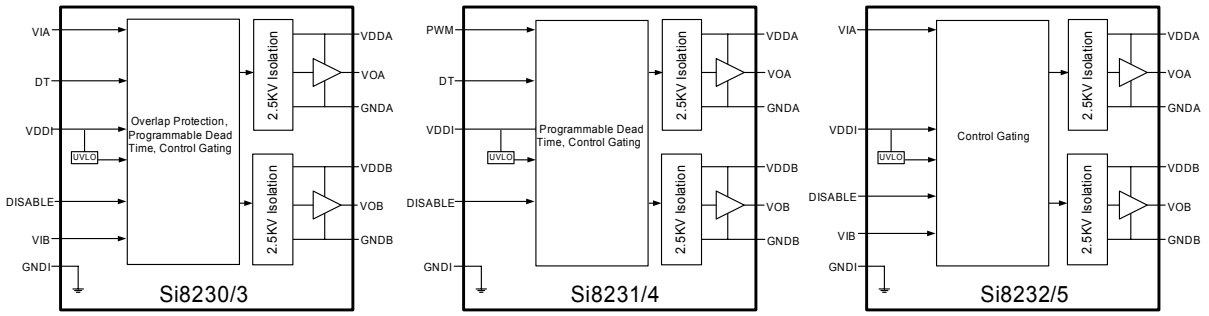
High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

Pin Assignments



Patents pending

Block Diagrams



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1. Top-Level Block Diagrams

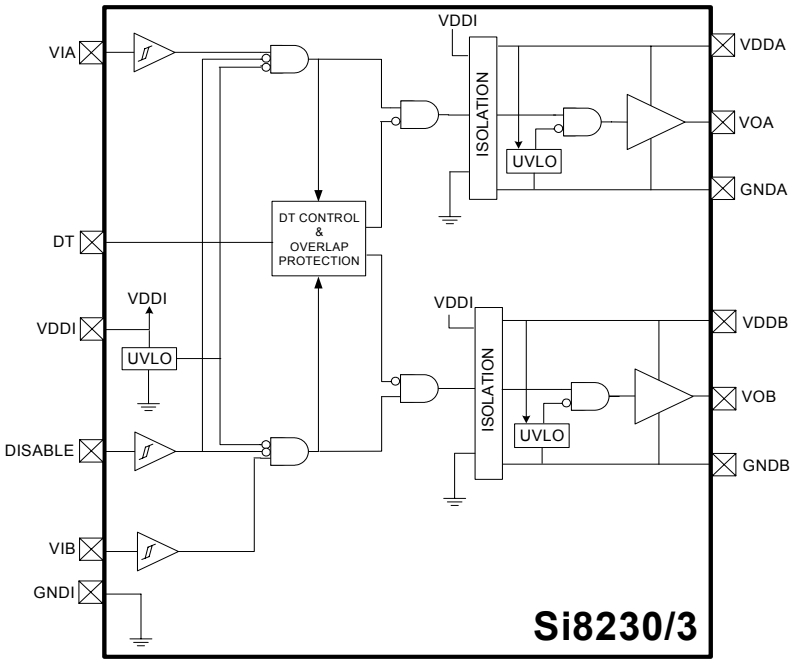


Figure 1. Si8230/3 Two-Input High-Side/Low-Side Isolated Drivers

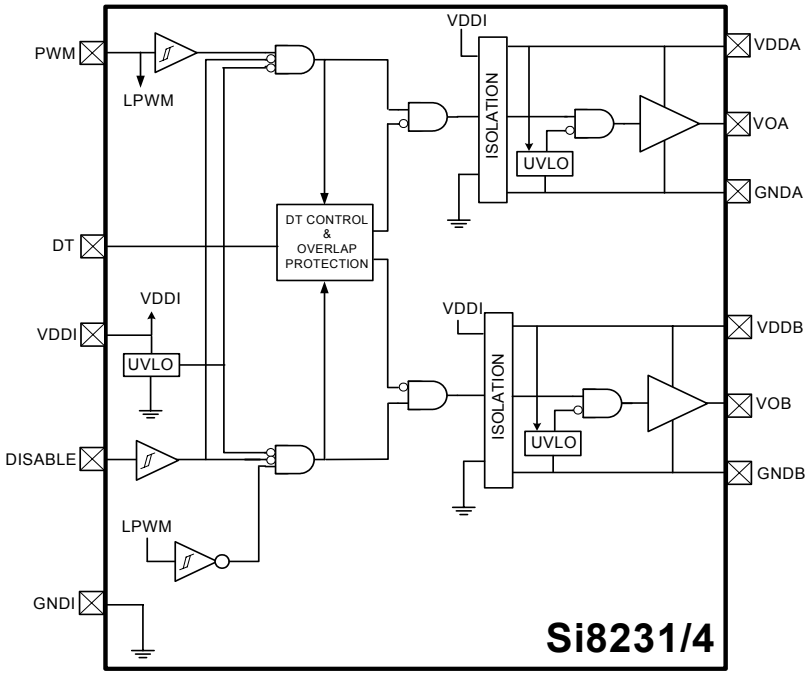


Figure 2. Si8231/4 Single-Input High-Side/Low-Side Isolated Drivers

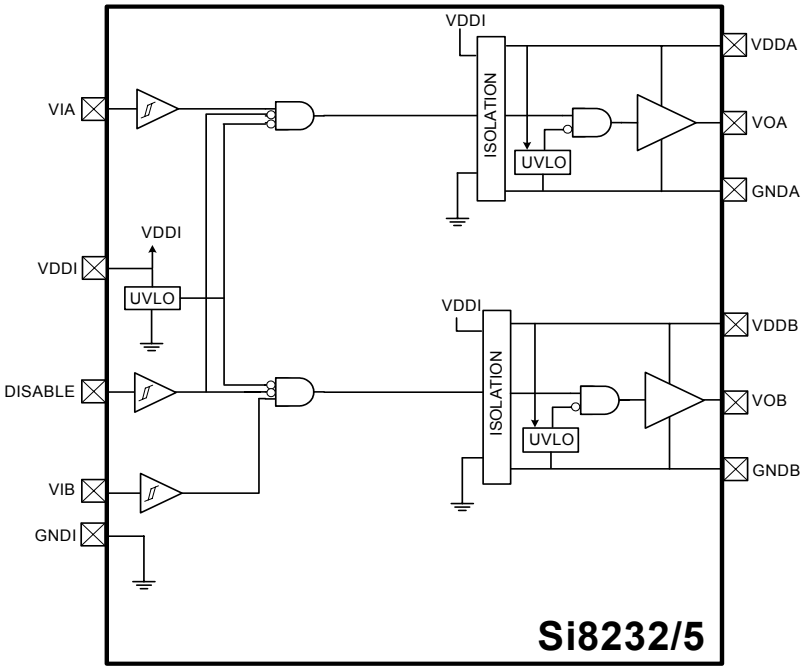


Figure 3. Si8232/5 Dual Low-Side Isolated Drivers

2. Pin Descriptions

Table 1. Si8230/3 Two-Input HS/LS Isolated Driver

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 7 ns dead time when connected to VDDI or left open (see "5.7.Programmable Dead Time and Overlap Protection" on page 16).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 10 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 10 to 24 V.

Table 2. Si8231/4 PWM Input HS/LS Isolated Driver

Pin	Name	Description
1	PWM	PWM input
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 7 ns dead time when connected to VDDI or left open (see "5.7.Programmable Dead Time and Overlap Protection" on page 16).
7	NC	No connection.

Table 2. Si8231/4 PWM Input HS/LS Isolated Driver (Continued)

8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for VOB driver output.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 10 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 10 to 24 V.

Table 3. Si8232/5 Dual LS Isolated Driver

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	NC	No connection.
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for VOB driver output.
10	VOB	Driver B output.
11	VDDB	Driver output VOB power supply voltage terminal; connect to a source of 10 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver B output.
16	VDDA	Driver A power supply voltage terminal; connect to a source of 10 to 24 V.

3. Electrical Specifications

Table 4. Electrical Characteristics

4.5 V < VDDI< 5.5 V, VDDA = VDDB = 12 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Specifications						
Input-side power supply voltage	VDDI		4.5	—	5.5	V
Driver supply voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB	10	—	24	V
Input supply quiescent current	IDDI(Q)		—	—	11	mA
Output supply quiescent current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input supply active current	IDDI	PWM freq = 500 kHz	—	11	—	mA
Input pin leakage current	IIA, IIB, IPWM, IDISABLE		–10	—	+10	µA dc
Logic HIGH input threshold	VIH		2.0	—	—	V
Logic LOW input threshold	VIL		—	—	0.8	V
Logic HIGH output voltage	VOAH, VOBH	IOA, IOB = –1 mA	VDDA – 0.04	—	—	V
Logic LOW output voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output short-circuit pulsed sink current	IOA(SCL), IOB(SCL)	Si8230/1/2, Figure 4	—	0.5	—	A
		Si8233/4/5, Figure 4	—	4.0	—	
Output short-circuit pulsed source current	IOA(SCH), IOB(SCH)	Si8230/1/2, Figure 5	—	0.25	—	
		Si8233/4/5, Figure 5	—	2.0	—	
Output sink resistance	$R_{ON(SINK)}$	Si8230/1/2	—	5.0	—	Ω
		Si8233/4/5	—	1.0	—	
Output source resistance	$R_{ON(SOURCE)}$	Si8230/1/2	—	15	—	
		Si8233/4/5	—	2.7	—	
VDDI undervoltage threshold	VDDIUV+	VDDI rising	3.60	—	4.40	V
VDDI negative-going lockout hysteresis	VDDIH–	VDDI falling	—	300	—	mV

***Note:** T_{DD} is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).

Table 4. Electrical Characteristics (Continued)
4.5 V < VDDI< 5.5 V, VDDA = VDDB = 12 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDDA, VDDB positive-going undervoltage threshold	VDDAUV+, VDDBUV+	VDDA, VDDB rising	7.5	8.5	9.5	V
VDDA, VDDB negative-going undervoltage threshold	VDDAUVH–, VDDBUVH–	VDDA, VDDB falling	7.0	8.0	9.0	V
AC Specifications						
Propagation delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	—	50	ns
Minimum Overlap Time	TDD	DT = VDDI, Note*	—	–0.4	—	ns
Programmed Dead Time	DT	Fig 2.3, RDT = 100 k	—	1,000	—	ns
		Fig 2.3, RDT = 6 k	—	72	—	
Output rise and fall time	t_R,t_F	C_L = 200 pF (Si8230/1/2)	—	—	12	ns
		C_L = 200 pF (Si8233/4/5)	—	—	20	
Shutdown time from DISABLE true	tSD		—	—	50	ns
Restart time from DISABLE false	tRESTART		—	—	50	ns
Device start-up time	tSTART	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	2	µs

***Note:** T_{DD} is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).

3.1. Test Circuits

Figures 4 and 5 depict sink current and source current test circuits.

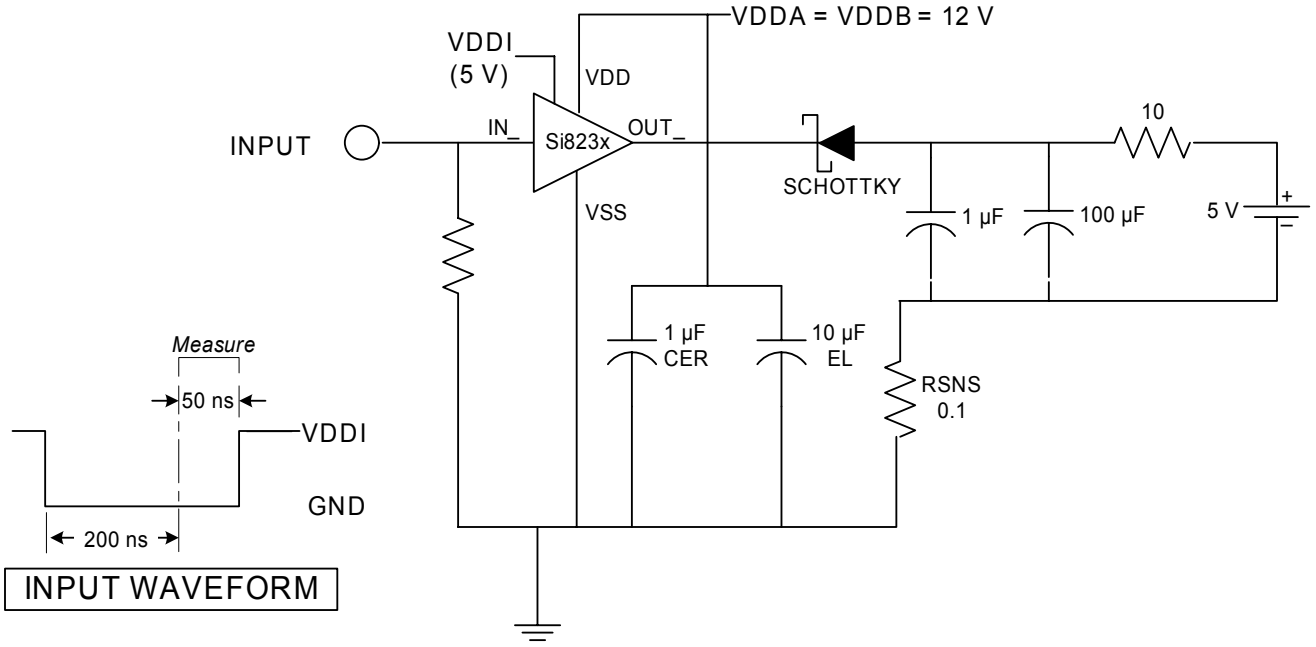


Figure 4. Sink Current Test Circuit

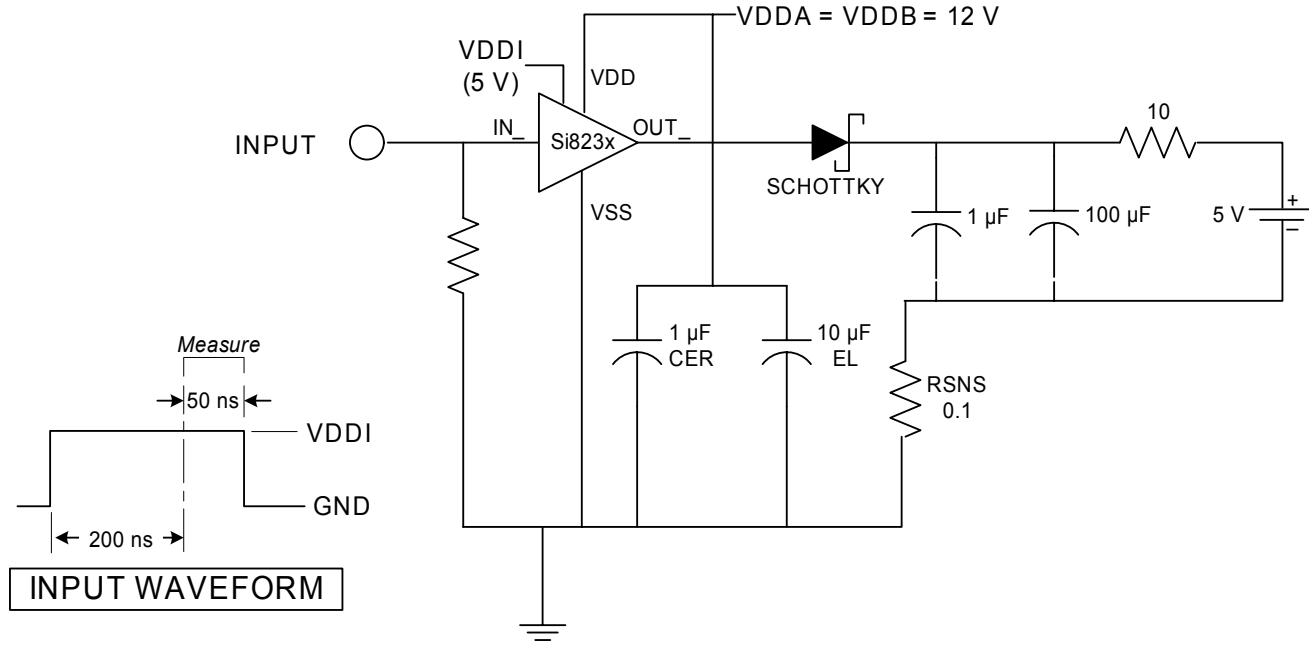


Figure 5. Source Current Test Circuit

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Storage temperature	T_{STG}	–65		+150	°C
Ambient temperature under bias	T_A	–40		+125	°C
Input-side supply voltage	V_{DDI}	–0.6		6.0	V
Driver-side supply voltage	V_{IA}, V_{IB}	–0.6		24	V
Voltage on any pin with respect to ground (not including IIN, IOUT)	V_{IN}	–0.5		VDD + 0.5	V
Lead solder temperature (10 sec.)	—	—	—	260	Degrees C
DC isolation (output to output)	—	—	—	1,000	VDC
DC isolation (input to output)	—	—	—	3,000	VDC

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Regulatory Information

UL
The Si823x is certified under UL1577 component recognition program to provide basic insulation to 2500 V_{RMS} (1 minute). It is production tested $\geq$ 3000 V_{RMS} for 1 second. For more details, see File E257455.

Table 7. Insulation and Safety-related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Minimum Air Gap (Clearance)	L(IO1)		7.7 min	mm
Minimum External Tracking (Creepage)	L(IO2)		8.1	mm
Minimum Internal Gap (Internal Clearance)			0.008 min	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the Si823x is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

4. Overview

The Si823x ISOdrivers are dual output drivers for isolated high-side/low-side and dual low-side gate drive applications. These products utilize Silicon Laboratories' proprietary silicon isolator technology, which enables fast propagation time while withstanding 600 V dc from the input to either output and between outputs. The operation of this isolator is analogous to that of an optocoupler, except that an RF carrier is modulated instead of light. This simple architecture provides a robust, isolated data path and requires no special considerations or initialization at start-up. As shown in Figure 6, an isolation channel consists of an RF transmitter and receiver separated by an RF transformer.

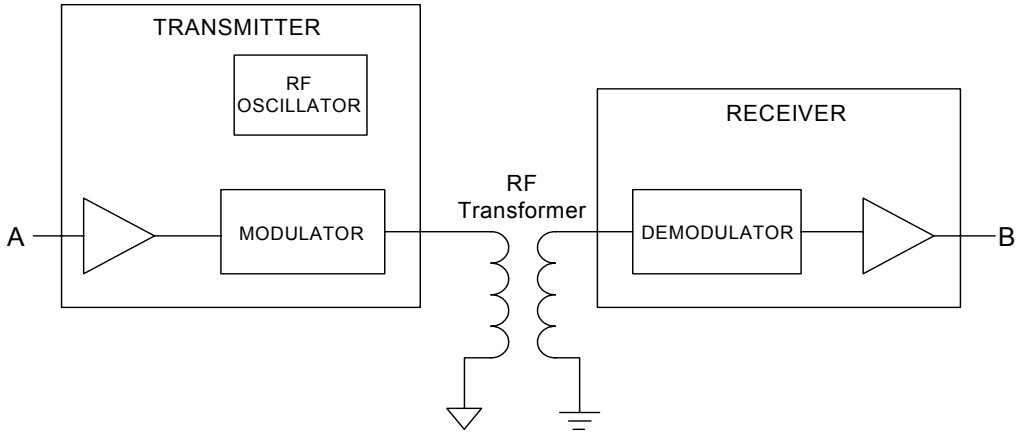


Figure 6. Isolator Operation

Input "A" turns the RF carrier on when high and off when low. The carrier is transmitted through the RF transformer to the output side demodulator, which consists of a receiver tuned to the carrier frequency. The demodulator asserts output "B" when sufficient in-band energy is detected. The driver output stage follows that of output B.

5. Application Information

The Si823x family of isolated drivers consists of high-side, low-side, and dual low-side driver configurations.

5.1. Products

Table 8 shows the configuration and functional overview for each product in this family.

Table 8. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-side/Low Side	✓	✓	VIA, VIB	0.5
Si8231	High-side/Low Side	✓	✓	PWM	0.5
Si8232	Dual Low Side	—	—	VIA, VIB	0.5
Si8233	High-side/Low Side	✓	✓	VIA, VIB	4.0
Si8234	High-side/Low Side	✓	✓	PWM	4.0
Si8235	Dual Low Side	—	—	VIA, VIB	4.0

5.2. Device Behavior

Table 9 contains truth tables for the Si8230/3, Si8231/4, and Si8232/5 families.

Table 9. Si823x Family Truth Table

Si8230/3 (High-Side/Low-Side) Truth Table				
VIA, VIB Inputs	**VDDI State**	**Disable**	**VOA/VOB Output**	**Notes**
H	Powered	L	H	Output transition occurs after internal dead time expires.
L	Powered	L	L	Output transition occurs after internal dead time expires.
X	Unpowered	X	L	Output returns to input state within 500 ns of VDDI power restoration.
X	Powered	H	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table				
PWM Input	**VDDI State**	**Disable**	**VOA/VOB Output**	**Notes**
H	Powered	L	H	Output transition occurs after internal dead time expires.
L	Powered	L	L	Output transition occurs after internal dead time expires.
X	Unpowered	X	L	Output returns to input state within 500 ns of VDDI power restoration.
X	Powered	H	L	Device is disabled.
Si8232/5 (Dual Low-Side) Truth Table				
VIA, VIB Inputs	**VDDI State**	**Disable**	**VOA/VOB Output**	**Notes**
H	Powered	L	H	Output transition occurs immediately (no internal dead time).
L	Powered	L	L	
X	Unpowered	X	L	Output returns to input state within 500 ns of VDDI power restoration.
X	Powered	H	L	Device is disabled.

5.3. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

5.4. Power Dissipation Considerations

Proper system design must assure that the Si823x operates within safe thermal limits across the entire load range. The Si823x total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load. Equation 1 shows total Si823x power dissipation. In a non-overlapping system, such as a high-side/low-side driver, n = 1. For a dual low-side driver with each driver having an independent load, n can have a maximum value of 2, corresponding to a 100% overlap between the two outputs.

$$P_D = V_{DDI}I_{DDI} + 2(V_{DDO}I_{QOUT} + C_{int}V_{DDO}^2F) + 2n(C_LV_{DDO}^2F)$$

where:

P_D is the total Si823x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{QOUT} is the driver die maximum bias current (5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

V_{DDI} is the input-side VDD supply voltage (4.5 to 5.5 V)

V_{DDO} is the driver-side supply voltage (10 to 24 V)

F is the switching frequency (Hz)

n is the overlap constant (max value = 2)

Equation 1.

The maximum power dissipation allowable for the Si823x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta ja}$$

where:

P_{Dmax} = Maximum Si823x power dissipation (W)

T_{jmax} = Si823x maximum junction temperature (145 °C)

T_A = Ambient temperature (°C)

θja = Si823x junction-to-air thermal resistance (105 °C/W)

F = Si823x switching frequency (Hz)

Equation 2.

Substituting values for PDMAX TjMAX, TA, and ja into Equation 2 results in a maximum allowable total power dissipation of 1.1 W. Maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 4 on page 8 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume VDDI = 5 V and VDDA = VDDB = 18 V.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 7.5 \times 10^{-11}$$

Equation 3.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 3.7 \times 10^{-10}$$

Equation 4.

Equation 1 and Equation 2 are graphed in Figure 7 where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.

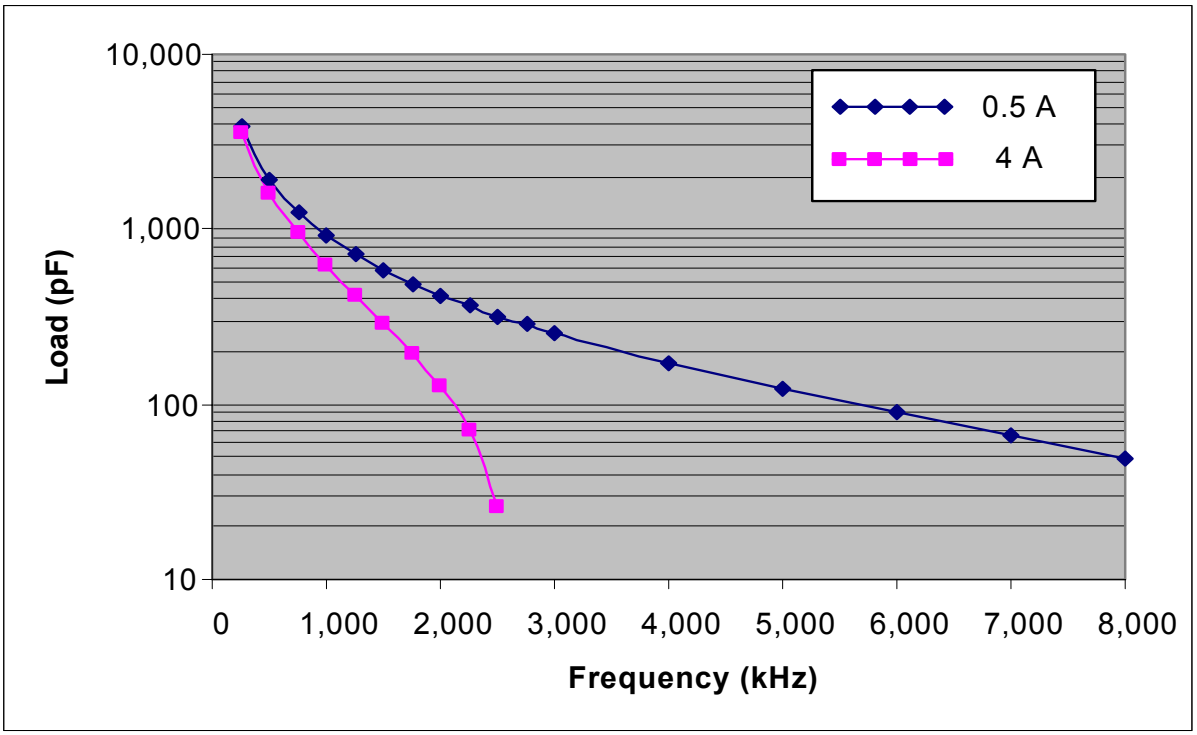


Figure 7. Max Load vs. Switching Frequency

5.5. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si823x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si823x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

5.6. Device Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 8, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

5.6.1. Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTARTUP. Following this, the outputs follow the states of inputs VIA and VIB.

5.6.2. Under Voltage Lockout (UVLO)

UVLO is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own under voltage lockout monitors.

The Si823x input side enters UVLO when VDDI $\leq V_{IUVH-}$, and exits UVLO when VDDI > VDD_{IUV+}. The driver outputs, VOA and VOB, remain low when the input side of the Si823x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below VDD_{AUV-} and exits UVLO when VDDA rises above VDD_{AUV+}.

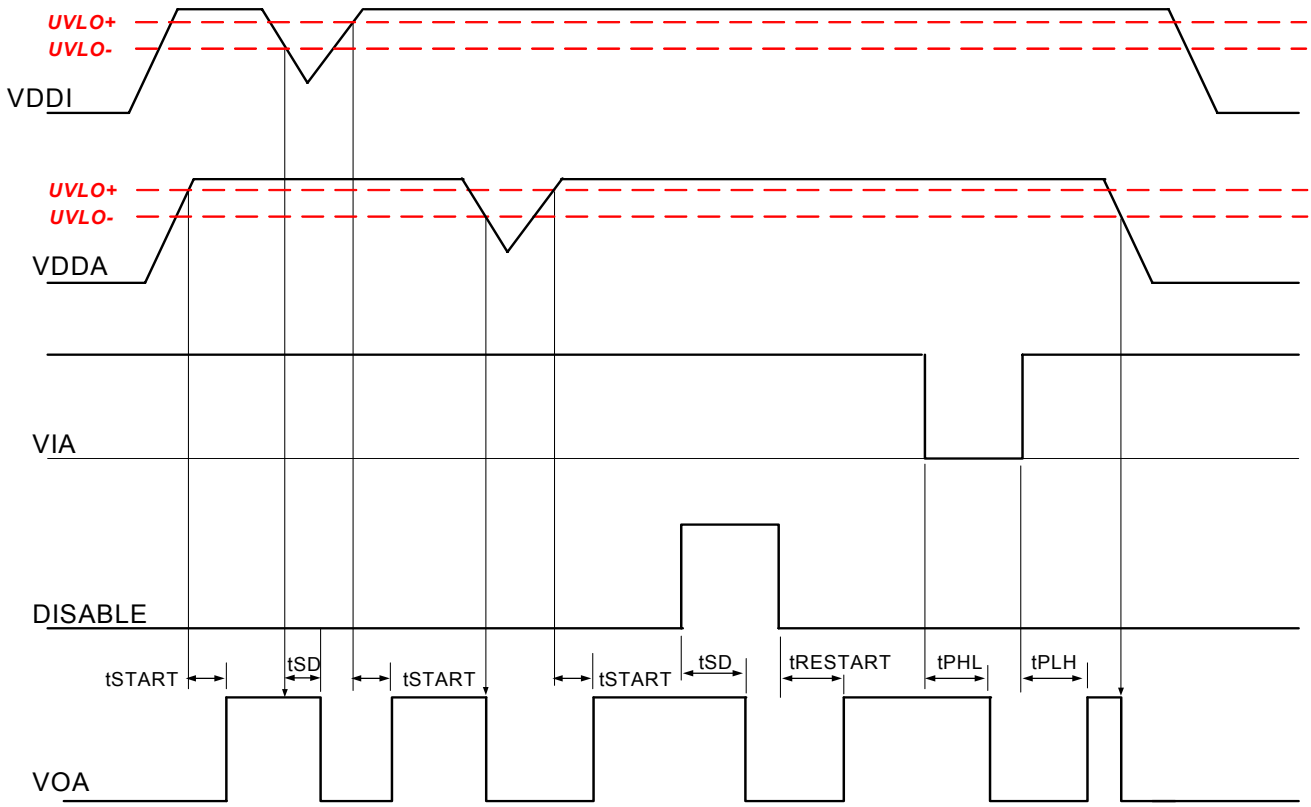


Figure 8. Device Behavior during Normal Operation and Shutdown

5.6.3. Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8231/4), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

5.6.4. Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after DISABLE = V_{IH} and resumes within tRESTART after DISABLE = V_{IL}. The DISABLE input has no effect if VDDI is below its UVLO level (i.e. VOA, VOB remain low).

5.7. Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8230/1/3/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB (Figure 2.3a). When enabled, dead time is present on all transitions, even after overlap recovery (Figure 2.3b). The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 5.

$$DT \approx 11 \times RDT$$

where:

DT= dead time (ns)

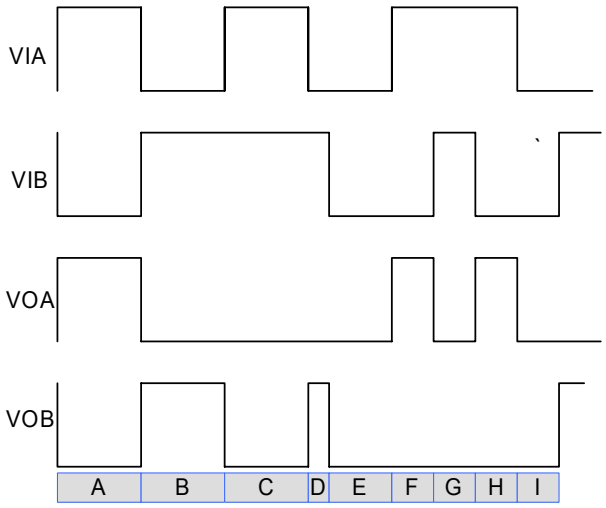
and

RDT= dead time programming resistor (kΩ)

Equation 5.

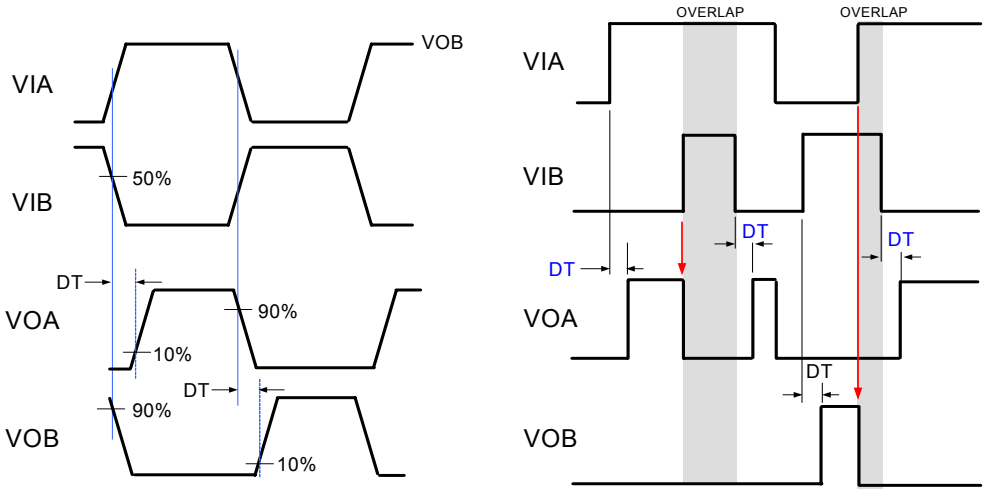
The device driving VIA and VIB should provide a minimum dead time of TDD to avoid activating overlap protection. Input/output timing waveforms for the two-input drivers are shown in Figure 8, and dead time waveforms are shown in Figure 9. If dead time programming is not used, it is strongly recommended that DT be connected to VDDI to avoid capacitive noise coupling; however, DT may also be left unconnected.

Note: If DT is left floating, there can be no DC leakage path between ground and DT. Avoid adding parasitic or component capacitance in parallel with RDT.



Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

Figure 8. Input/Output Waveforms for High Side/Low Side Two-Input Drivers



A. Typical Dead Time Operation

B. Dead Time Operation During Overlap

Figure 9. Dead Time Waveforms for High Side/Low Side Two-Input Drivers

6. Applications

The following examples illustrate typical circuit configurations using the Si823x.

6.1. High-Side/Low-Side Driver

Figure 10A shows the Si8230/3 controlled using the VIA and VIB input signals, and Figure 10B shows the Si8231/4 controlled by a single PWM signal.

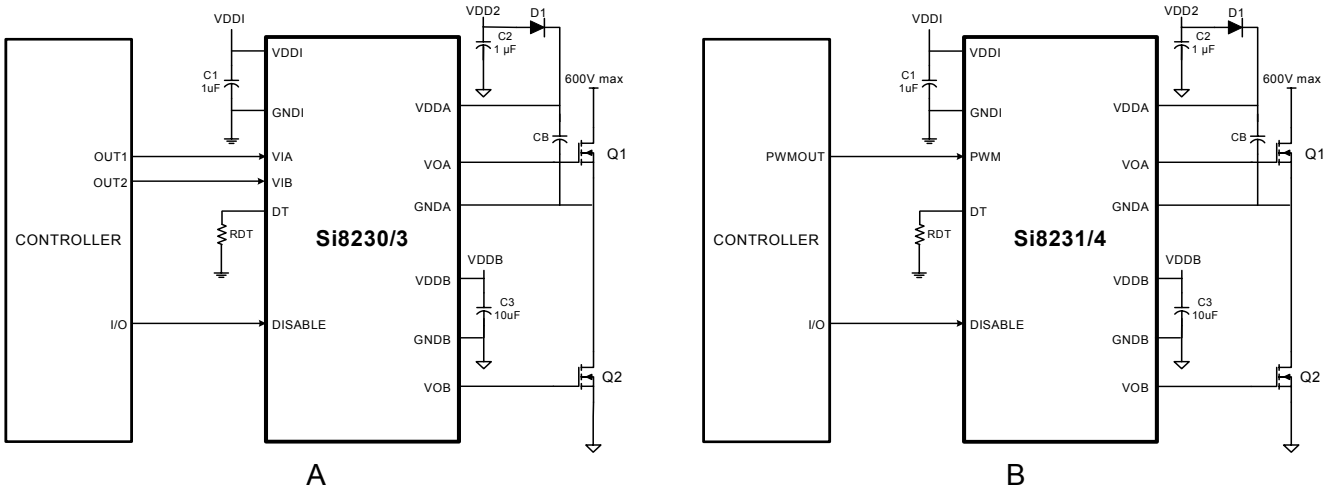


Figure 10. Si823x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 600 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si823x requires VDD in the range of 4.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 10 and 24 V. Also note that the bypass capacitors on the Si823x should be located as close to the chip as possible. Moreover, it is recommended that 0.1, 1, and 10 µF bypass capacitors be used to minimize high frequency and maximize performance.

6.2. Dual Low-Side Driver

Figure 11 shows the Si823x configured as a dual low-side driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 600 V dc between them.

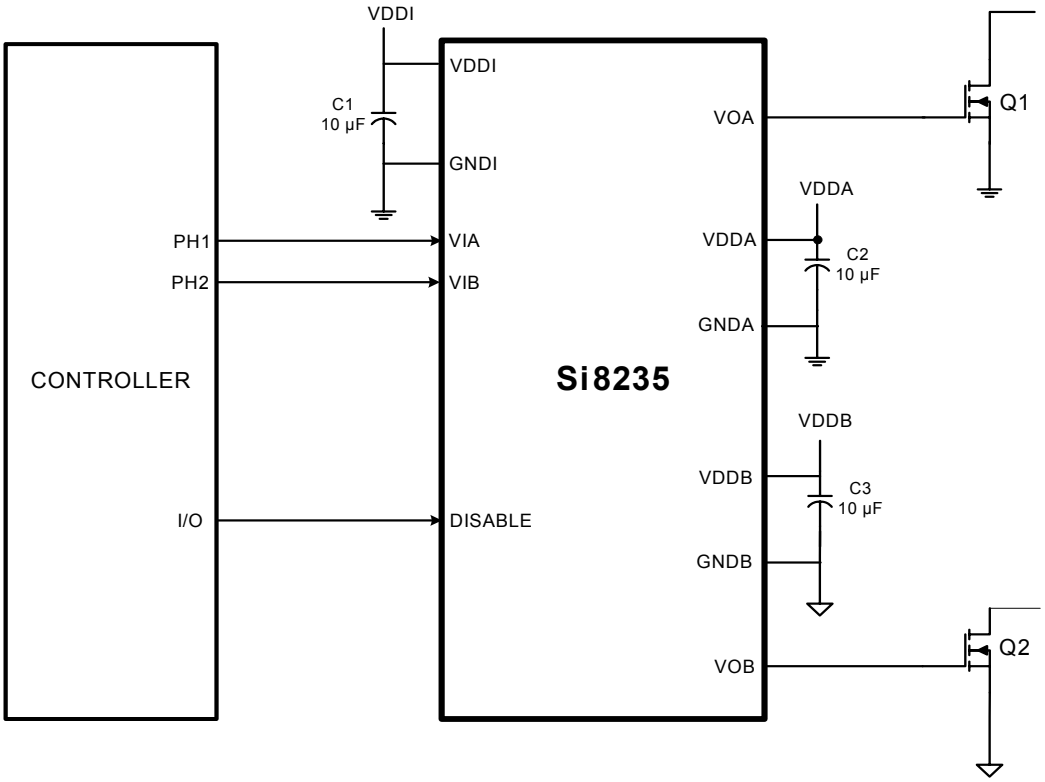


Figure 11. Si8235 in a Dual Low-Side Driver Application

7. Ordering Guide

Part Number	Inputs	Configuration	Peak Output Current (A)	Package	Temp Range (°C)
Si8230-A-IS	VIA, VIB	High Side/Low Side	0.5	16SO Wide	–40 to +125
Si8231-A-IS	PWM	High Side/Low Side			
Si8232-A-IS	VIA, VIB	Dual Low Side			
Si8233-B-IS	VIA, VIB	High Side/Low Side	4.0		
Si8234-B-IS	PWM	High Side/Low Side			
Si8235-B-IS	VIA, VIB	Dual Low Side			

8. Package Outline: Wide Body SOIC

Figure 12 illustrates the package details for the Quad-Channel Digital Isolator. Table 10 lists the values for the dimensions shown in the illustration. All packages are Pb-free and RoHS compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry classification and peak solder temperature.

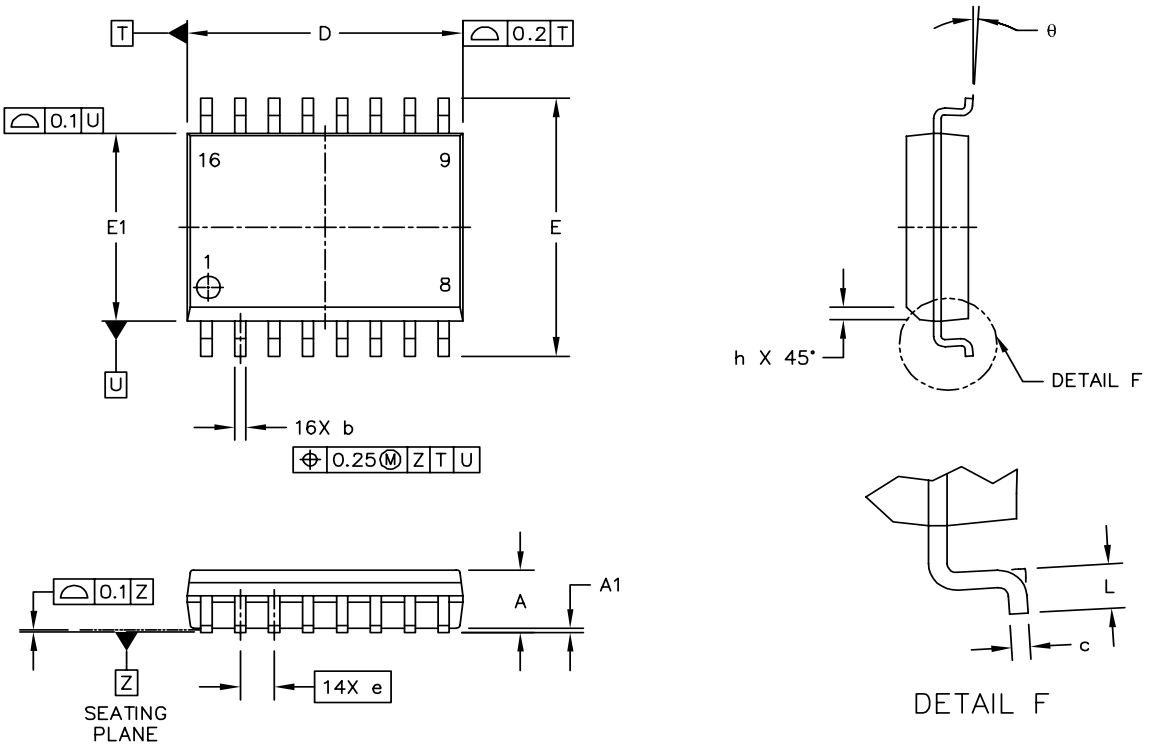


Figure 12. 16-Pin Wide Body SOIC

Table 10. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

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