N- and P-Channel
Enhancement-Mode Dual MOSFET

Features

► 500V breakdown voltage
► Independent N- and P-channels
► Electrically isolated N- and P-channels
► Low input capacitance
► Fast switching speeds
► Free from secondary breakdowns
► Low input and output leakage

Applications

► High voltage pulsers
► Amplifiers
► Buffers
► Piezoelectric transducer drivers
► General purpose line drivers

General Description

The Supertex TC1550 consists of a high voltage N-channel and P-channel MOSFET in an 8-Lead SOIC package. This is an enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.
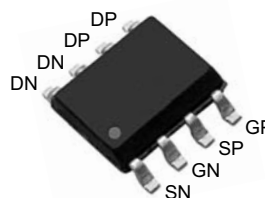
Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS}		$R_{DS(ON)}$ (Max)	
	8-Lead SOIC	N-Channel (V)	P-Channel (V)	N-Channel (Ω)	P-Channel (Ω)
TC1550	TC1550TG-G	500	-500	60	125

-G indicates package is RoHS compliant ('Green')

Pin Configuration
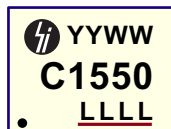
8-Lead SOIC (TG)
(top view)

DP, DP, DN, DN, GP, SP, GN, SN

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to + 150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Product Marking

YYWW
C1550
LLLL

YY = Year Sealed
WW = Week Sealed
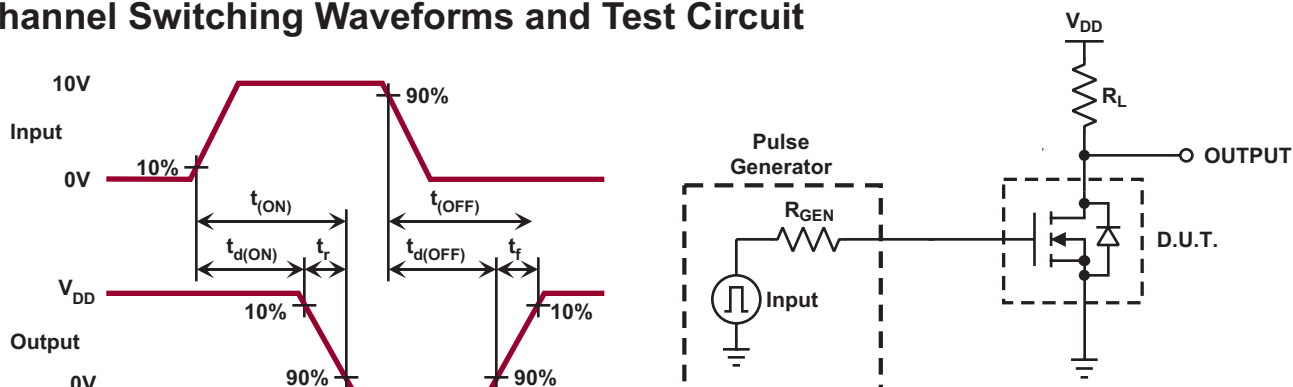L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC (TG)

N-Channel Electrical Characteristics *(T$_A$ = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV$_{DSS}$	Drain-to-source breakdown voltage	500	-	-	V	V$_{GS}$ = 0V, I$_D$ = 1.0mA
V$_{GS(th)}$	Gate threshold voltage	2.0	-	4.0	V	V$_{GS}$ = V$_{DS}$, I$_D$ =1.0mA
ΔV$_{GS(th)}$	Change in V$_{GS(th)}$ with temperature	-	-3.8	-5.0	mV/°C	V$_{GS}$ = V$_{DS}$, I$_D$ = 1.0mA
I$_{GSS}$	Gate body leakage current	-	-	100	nA	V$_{GS}$ = ±20V, V$_{DS}$ = 0V
I$_{DSS}$	Zero gate voltage drain current	-	-	10	μA	V$_{GS}$ = 0V, V$_{DS}$ = Max Rating
		-	-	1.0	mA	V$_{DS}$ = 0.8 Max Rating, V$_{GS}$ = 0V, T$_A$ = 125°C
I$_{D(ON)}$	On-state drain current	-	100	-	mA	V$_{GS}$ = 5.0V, V$_{DS}$ = 25V
		150	350	-		V$_{GS}$ = 10V, V$_{DS}$ = 25V
R$_{DS(ON)}$	Static drain-to-source on-state resistance	-	45	-	Ω	V$_{GS}$ = 5.0V, I$_D$ = 50mA
		-	40	60		V$_{GS}$ = 10V, I$_D$ = 50mA
ΔR$_{DS(ON)}$	Change in R$_{DS(ON)}$ with temperature	-	1.0	1.7	%/°C	V$_{GS}$ = 10V, I$_D$ = 50mA
G$_{FS}$	Forward transconductance	50	100	-	mmho	V$_{DS}$ = 25V, I$_D$ =50mA
C$_{ISS}$	Input capacitance	-	45	55	pF	V$_{GS}$ = 0V, V$_{DS}$ = 25V, f = 1.0MHz
C$_{OSS}$	Common source output capacitance	-	8.0	10		
C$_{RSS}$	Reverse transfer capacitance	-	2.0	5.0		
t$_{d(ON)}$	Turn-on delay time	-	-	10	ns	V$_{DD}$ = 25V, I$_D$ = 150mA, R$_{GEN}$ = 25Ω
t$_r$	Rise time	-	-	15		
t$_{d(OFF)}$	Turn-off delay time	-	-	10		
t$_f$	Fall time	-	-	10		
V$_{SD}$	Diode forward voltage drop	-	0.8	-	V	V$_{GS}$ = 0V, I$_{SD}$ = 500mA
t$_{rr}$	Reverse recovery time	-	300	-	ns	V$_{GS}$ = 0V, I$_{SD}$ = 500mA

Notes:
1. All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300μs pulse at 2% duty cycle.)
2. All AC parameters sample tested.

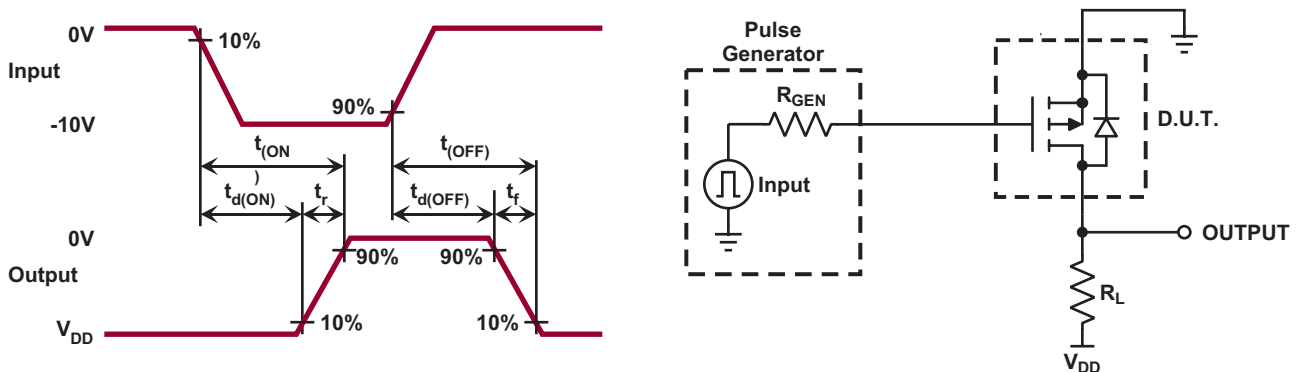# N-Channel Switching Waveforms and Test Circuit

Supertex inc. • 1235 Bordeaux Drive, Sunnyvale, CA 94089 • Tel: (408) 222-8888 • FAX: (408) 222-4895 • www.supertex.com

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P-Channel Electrical Characteristics *(T$_A$ = 25°C unless otherwise specified)*

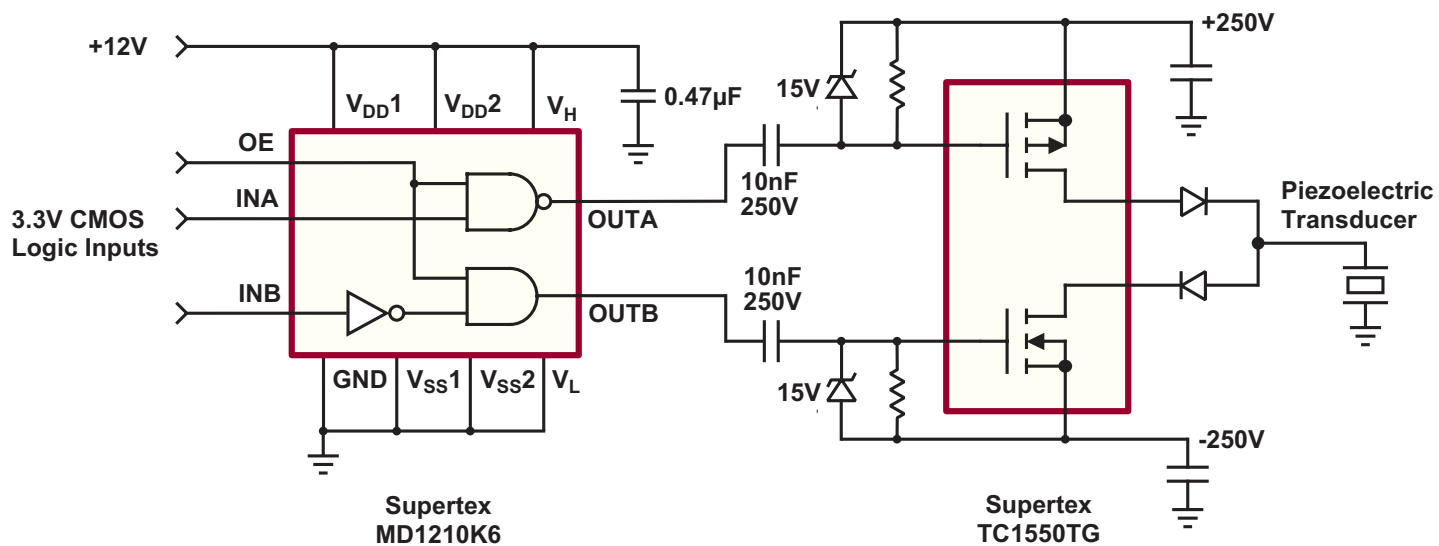| Sym	Parameter	Min	Typ	Max	Units	Conditions
BV$_{DSS}$	Drain-to-source breakdown voltage	-500	-	-	V	V$_{GS}$ = 0V, I$_D$ = -1.0mA
V$_{GS(th)}$	Gate threshold voltage	-2.0	-	-4.5	V	V$_{GS}$ = V$_{DS}$, I$_D$ = -1.0mA
ΔV$_{GS(th)}$	Change in V$_{GS(th)}$ with temperature	-	3.5	6.0	mV/°C	V$_{GS}$ = V$_{DS}$, I$_D$ = -1.0mA
I$_{GSS}$	Gate body leakage current	-	-	100	nA	V$_{GS}$ = ±20V, V$_{DS}$ = 0V
I$_{DSS}$	Zero gate voltage drain current	-	-	-10	µA	V$_{GS}$ = 0V, V$_{DS}$ = Max Rating
		-	-	-1.0	mA	V$_{DS}$ = 0.8 Max Rating, V$_{GS}$ = 0V, T$_A$ = 125°C
I$_{D(ON)}$	On-state drain current	-	-90	-	mA	V$_{GS}$ = -5.0V, V$_{DS}$ = -25V
		-100	-240	-		V$_{GS}$ = -10V, V$_{DS}$ = -25V
R$_{DS(ON)}$	Static drain-to-source on-state resistance	-	85	-	Ω	V$_{GS}$ = -5.0V, I$_D$ = -5.0mA
		-	80	125		V$_{GS}$ = -10V, I$_D$ = -10mA
ΔR$_{DS(ON)}$	Change in R$_{DS(ON)}$ with temperature	-	0.85	-	%/°C	V$_{GS}$ = -10V, I$_D$ = -10mA
G$_{FS}$	Forward transconductance	25	40	-	mmho	V$_{DS}$ = -25V, I$_D$ = -10mA
C$_{ISS}$	Input capacitance	-	40	70	pF	V$_{GS}$ = 0V, V$_{DS}$ = -25V, f = 1.0MHz
C$_{OSS}$	Common source output capacitance	-	10	20		
C$_{RSS}$	Reverse transfer capacitance	-	3.0	10		
t$_{d(ON)}$	Turn-on delay time	-	5.0	10	ns	V$_{DD}$ = -25V, I$_D$ = -100mA, R$_{GEN}$ = 25Ω
t$_r$	Rise time	-	8.0	10		
t$_{d(OFF)}$	Turn-off delay time	-	8.0	15		
t$_f$	Fall time	-	5.0	16		
V$_{SD}$	Diode forward voltage drop	-	-0.8	-1.5	V	V$_{GS}$ = 0V, I$_{SD}$ = -100mA
t$_{rr}$	Reverse recovery time	-	200	-	ns	V$_{GS}$ = 0V, I$_{SD}$ = -100mA

Notes:
1. All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse at 2% duty cycle.)
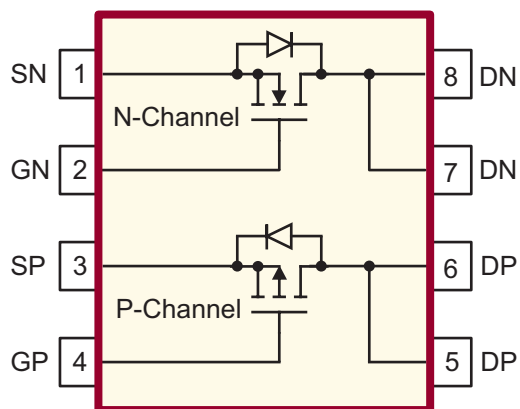2. All AC parameters sample tested.

P-Channel Switching Waveforms and Test Circuit
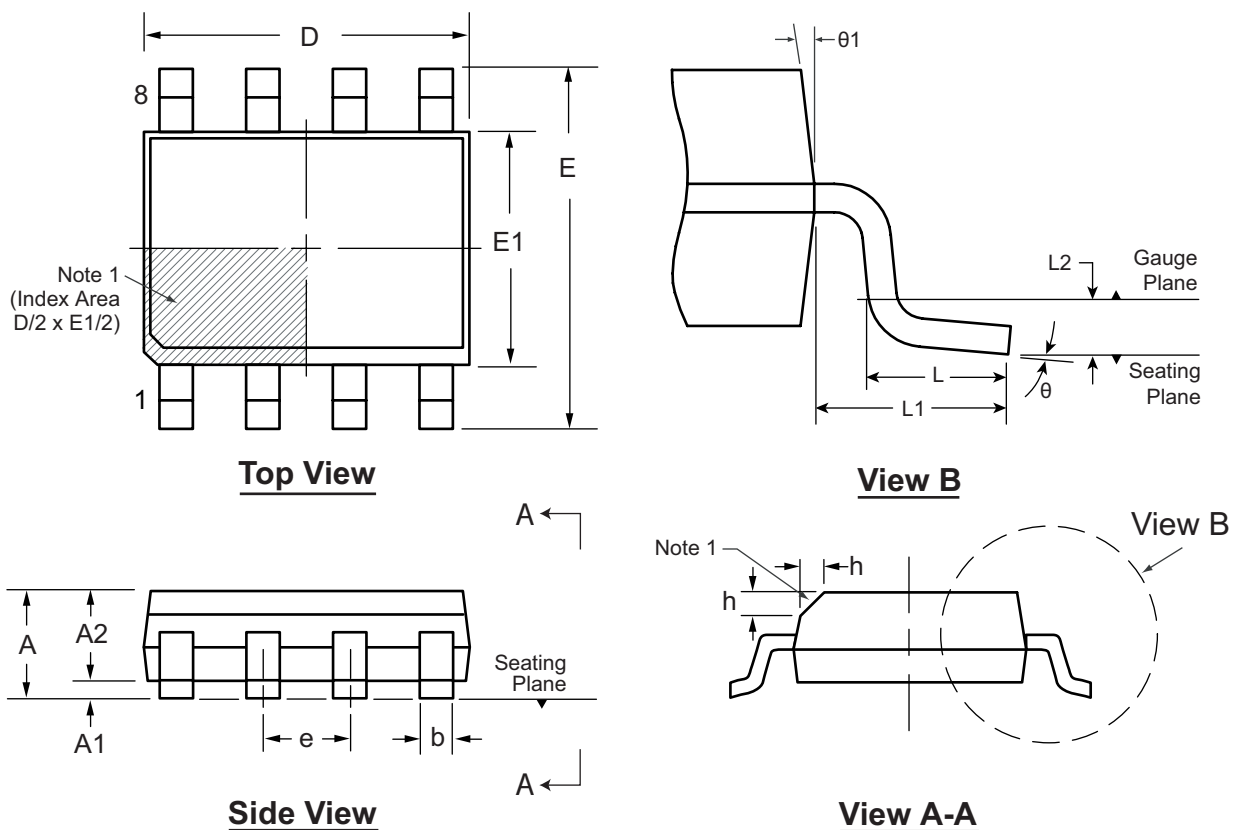
Typical Application Circuit

+12V

V_{DD}1   V_{DD}2   V_H   0.47µF

OE

3.3V CMOS
Logic Inputs

INA   OUTA

INB   OUTB

GND   V_{SS}1   V_{SS}2   V_L

**Supertex
MD1210K6**

10nF
250V

10nF
250V

15V

15V

+250V

-250V

**Piezoelectric
Transducer**

**Supertex
TC1550TG**

Block Diagram

SN	1		8	DN
N-Channel				
GN	2		7	DN
SP	3		6	DP
P-Channel				
GP	4		5	DP

8-Lead SOIC (Narrow Body) Package Outline (TG)
4.9x3.9mm body, 1.75mm height (max), 1.27mm pitch

Top View

View B

Side View

View A-A

Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35	0.10	1.25	0.31	4.80	5.80	3.80	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65	0.51	5.00	6.20	4.00		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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