TC4420M/TC4429M

6A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Will Withstand >1.5A Reverse Output Current
- Logic Input: Will Withstand Negative Swing Up To 5V
- ESD Protected: 4 kV
- Matched Rise and Fall Times:
  - 25 ns (2500 pF load)
- High Peak Output Current: 6A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability: 10,000 pF
- Short Delay Time: 55 ns (typ.)
- CMOS/TTL-Compatible Input
- Low Supply Current With Logic '1' Input:
  - 450 µA (typ.)
- Low Output Impedance: 2.5Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Wide Operating Temperature Range:
  - -55°C to +125°C
- See TC4420/TC4429 Data Sheet (DS21419) for additional temperature range and package offerings.

Applications

- Switch-mode Power Supplies
- Motor Controls
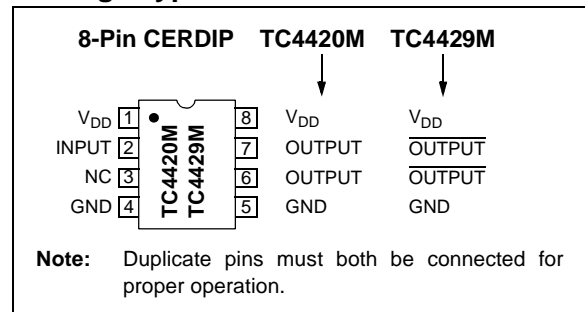- Pulse Transformer Driver
- Class D Switching Amplifiers

General Description

The TC4420M/TC4429M are 6A (peak), single-output MOSFET drivers. The TC4429M is an inverting driver (pin-compatible with the TC429M), while the TC4420M is a non-inverting driver. These drivers are fabricated in CMOS for lower power and more efficient operation versus bipolar drivers.

Both devices have TTL/CMOS-compatible inputs, which can be driven as high as V_{DD} + 0.3V or as low as -5V without upset or damage to the device. This eliminates the need for external level-shifting circuitry and its associated cost and size. The output swing is rail-to-rail, ensuring better drive voltage margin, especially during power-up/power-down sequencing. The propagational delay time is only 55 ns (typ.), while the output rise and fall times are only 25 ns (typ.) into 2500 pF across the usable power supply range.
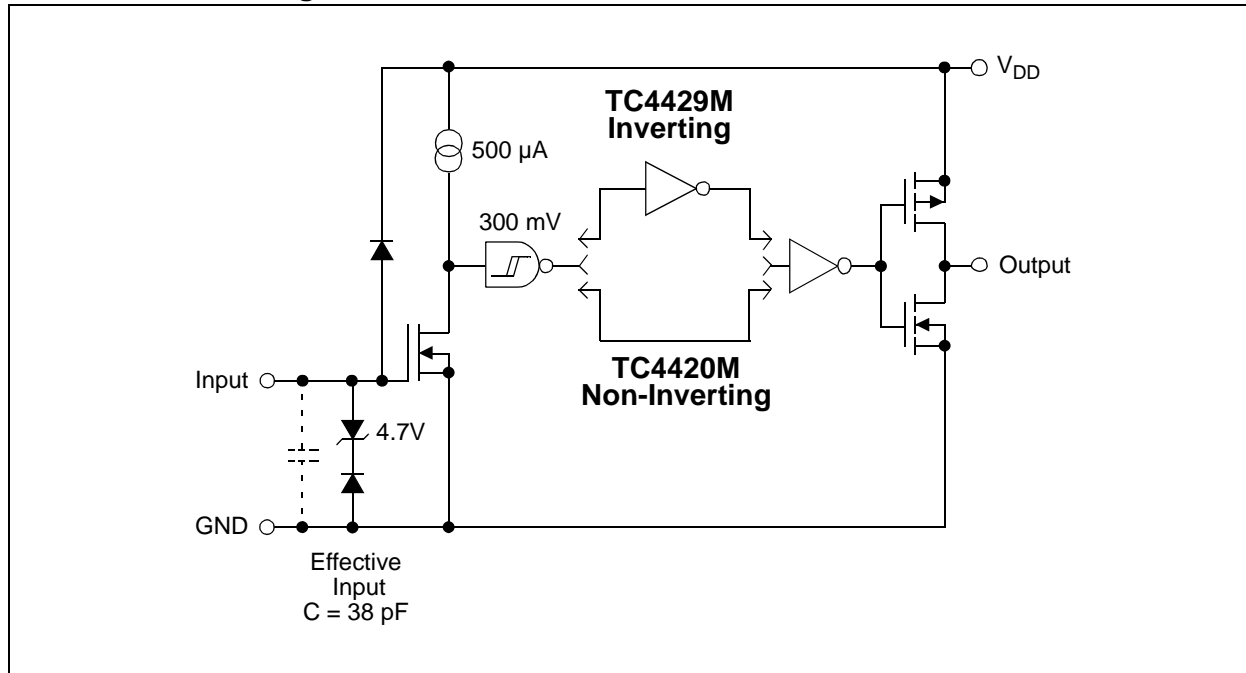
Unlike other drivers, the TC4420M/TC4429M are virtually latch-up proof. They replace three or more discrete components, saving PCB area and parts while improving overall system reliability.

Package Types:

8-Pin CERDIP   **TC4420M**   **TC4429M**

	TC4420M / TC4429M	TC4420M	TC4429M
V_{DD} 1		8 V_{DD}	V_{DD}
INPUT 2		7 OUTPUT	$\overline{OUTPUT}$
NC 3		6 OUTPUT	$\overline{OUTPUT}$
GND 4		5 GND	GND

Note: Duplicate pins must both be connected for proper operation.

TC4420M/TC4429M

Functional Block Diagram

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1.0   ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ....+20V
Input Voltage ....-5V to V_{DD} + 0.3V
Input Current ($V_{IN} > V_{DD}$)..................................50 mA

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.8	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Voltage Range	V_{IN}	- 5	—	V_{DD} + 0.3	V	
Input Current	I_{IN}	-10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	2.1	2.8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	1.5	2.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	6.0	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 1.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µs
Switching Time (Note 1)						
Rise Time	t_R	—	25	35	ns.	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	25	35	ns.	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	55	75	ns.	**Figure 4-1**
Delay Time	t_{D2}	—	55	75	ns.	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.45	1.5	mA	V_{IN} = 3V
		—	55	150	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1:   Switching times ensured by design.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.						
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Voltage Range	V_{IN}	-5	—	V_{DD} + 0.3	V	
Input Current	I_{IN}	-10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	2.3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	32	60	ns.	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	34	60	ns.	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	50	100	ns.	**Figure 4-1**
Delay Time	t_{D2}	—	65	100	ns.	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.45	3	mA	V_{IN} = 3V
		—	60	400	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V $\leq V_{DD} \leq$ 18V.						
Temperature Ranges						
Specified Temperature Range (M)	T_A	-55	—	+125	℃	
Maximum Junction Temperature	T_J	—	—	+150	℃	
Storage Temperature Range	T_A	-65	—	+150	℃	
Package Thermal Resistances						
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	°C/W	

2.0   TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V $\leq V_{DD} \leq$ 18V.
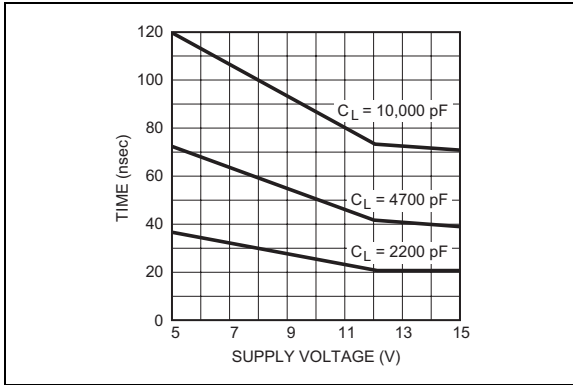
FIGURE 2-1:   *Rise Time vs. Supply Voltage.*
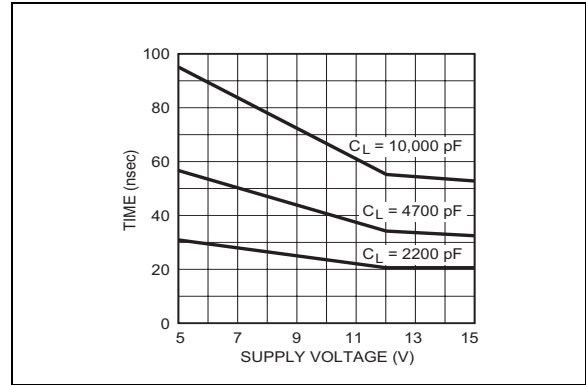
FIGURE 2-4:   *Fall Time vs. Supply Voltage.*
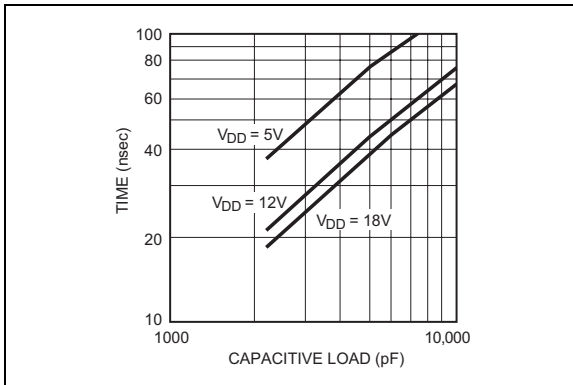
FIGURE 2-2:   *Rise Time vs. Capacitive Load.*
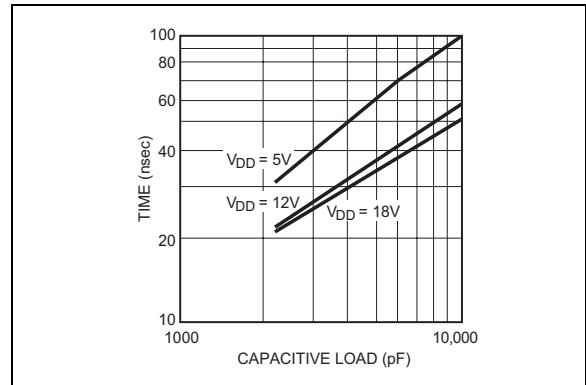
FIGURE 2-5:   *Fall Time vs. Capacitive Load.*
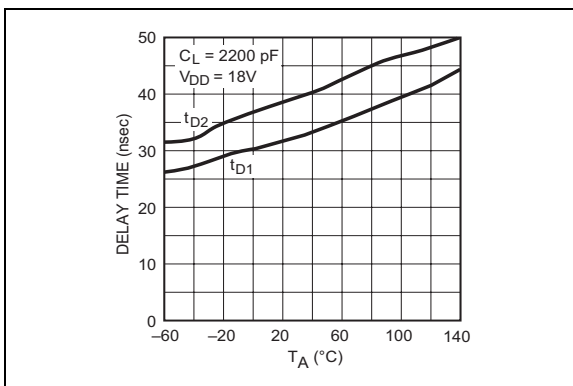
FIGURE 2-3:   *Propagation Delay Time vs. Temperature.*
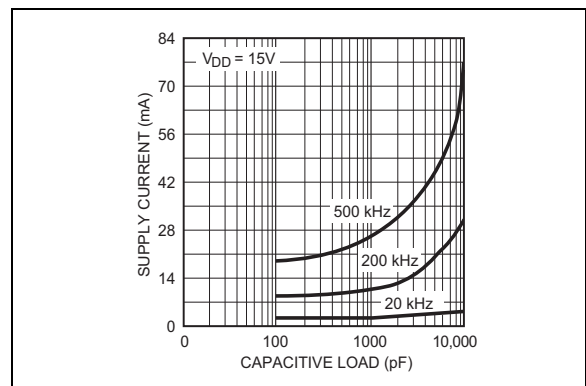
FIGURE 2-6:   *Supply Current vs. Capacitive Load.*

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TC4420M/TC4429M

Note: Unless otherwise indicated, T_A = +25℃ with 4.5V $\leq V_{DD} \leq$ 18V.
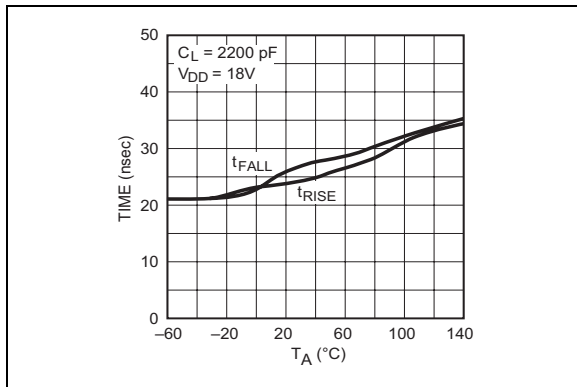
FIGURE 2-7: *Rise and Fall Times vs. Temperature.*

FIGURE 2-8: *Propagation Delay Time vs. Supply Voltage.*

FIGURE 2-9: *Supply Current vs. Frequency.*

FIGURE 2-10: *High-State Output Resistance vs. Supply Voltage.*

FIGURE 2-11: *Effect of Input Amplitude on Propagation Delay.*
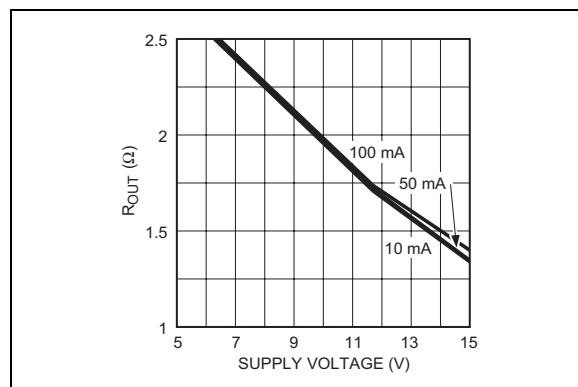
FIGURE 2-12: *Low-State Output Resistance vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25℃ with 4.5V $\le V_{DD} \le$ 18V.

* The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.
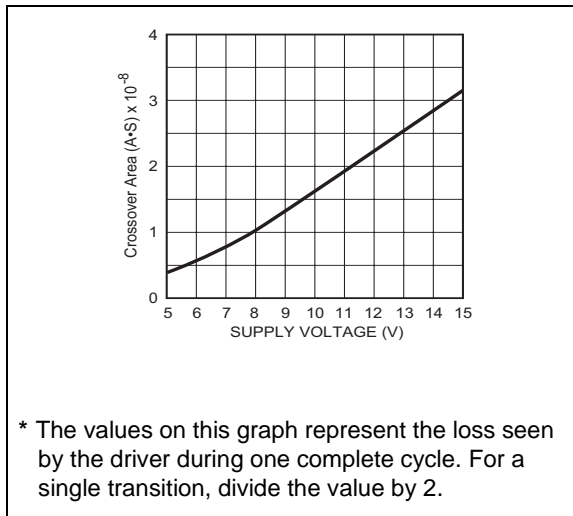
FIGURE 2-13: *Crossover Energy*.*

3.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1:   PIN FUNCTION TABLE

Pin No. 8-Pin CERDIP	Symbol	Description
1	V_{DD}	Supply input, 4.5V to 18V
2	INPUT	Control input, TTL/CMOS compatible input
3	NC	No Connection
4	GND	Ground
5	GND	Ground
6	OUTPUT	CMOS push-pull output
7	OUTPUT	CMOS push-pull output
8	V_{DD}	Supply input, 4.5V to 18V

3.1   Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pins. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

3.2   Control Input

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input circuitry of the TC4420M/TC4429M MOSFET driver also has a "speed-up" capacitor. This helps to decrease the propagation delay times of the driver. Because of this, input signals with slow rising or falling edges should not be used, as this can result in double-pulsing of the MOSFET driver output.

3.3   CMOS Push-Pull Output

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 6.0A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4   Ground

The ground pins are the return path for the bias current and the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.
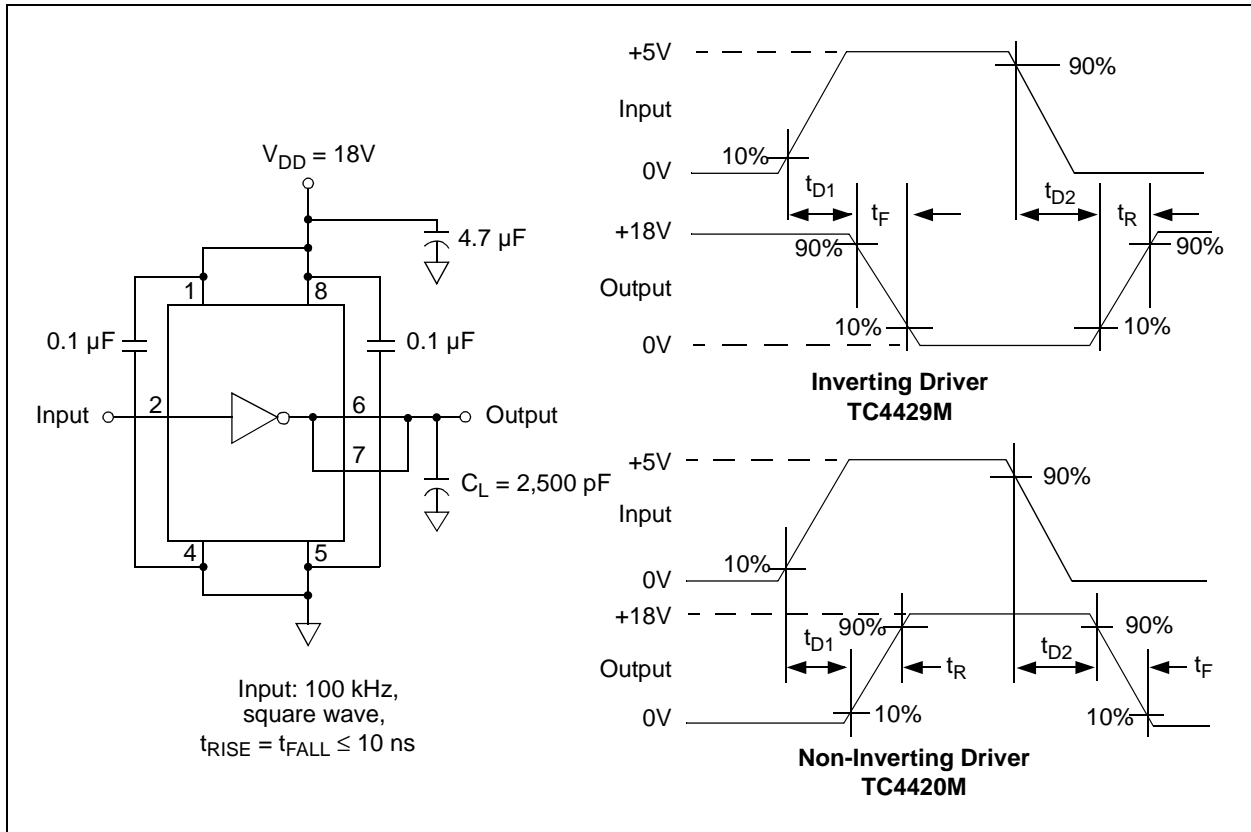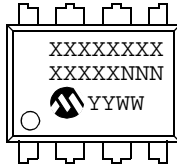
4.0   APPLICATIONS INFORMATION

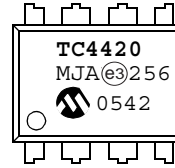*FIGURE 4-1:*   *Switching Time Test Circuits.*

TC4420M/TC4429M

5.0   PACKAGING INFORMATION

### 5.1   Package Marking Information

8-Lead CERDIP (300 mil)

```
XXXXXXXX
XXXXXNNN
(M)YYWW
```

Example:

```
TC4420
MJA(e3)256
(M)0542
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead Ceramic Dual In-line – 300 mil (CERDIP)
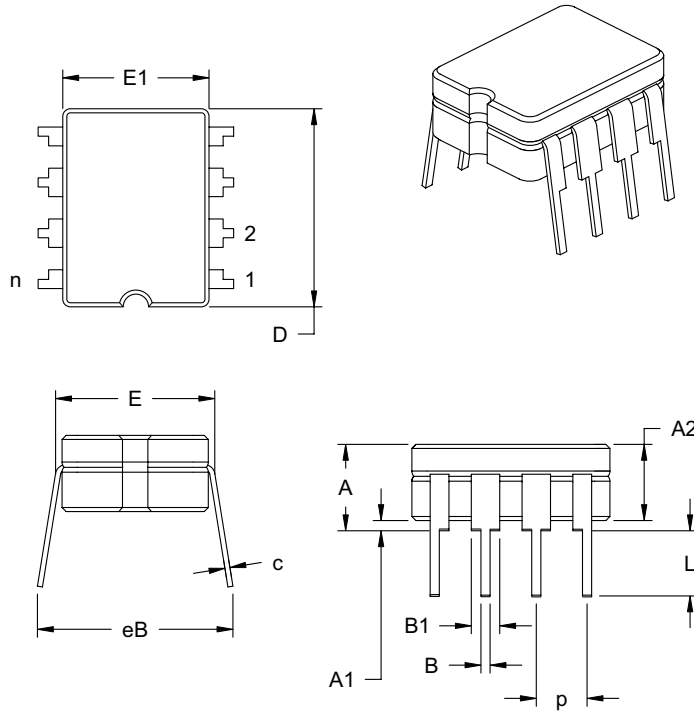
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2005)

• Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX
Device and Temperature Range	**Package**

Device and Temperature Range:	TC4420M: 6A High-Speed MOSFET Driver, Non-Inverting, -55°C to +125°C
	TC4429M: 6A High-Speed MOSFET Driver, Inverting, -55°C to +125°C
Package:	JA = Ceramic Dual In-line (300 mil Body), 8-lead

Examples:

a) TC4420MJA: 6A High-Speed MOSFET Driver, Non-inverting, 8LD CERDIP package.

a) TC4429MJA: 6A High-Speed MOSFET Driver, Inverting, 8LD CERDIP package.

NOTES:

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
=== ISO/TS 16949:2002 ===

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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