

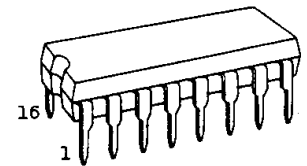
TC40174BP/TC40174BF HEX D-TYPE FLIP-FLOP

TC40174BP/TC40174BF contains six circuits of D type flip-flops having common clock terminal and clear terminal. The logical input applied to D_n input is transferred to Q_n output by the rising edge of CLOCK input.

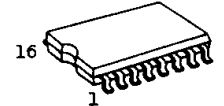
$\overline{\text{RESET}}$ input is active with "L" level. This has the same functions as TTL 54174/74174 and the pin assignment is also same.

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +20	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T _A	-40 ~ 85	°C
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10sec	

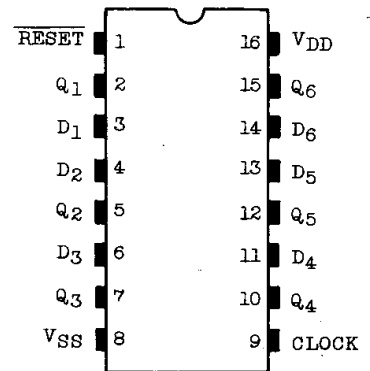


DIP 16 (3D16A-P)



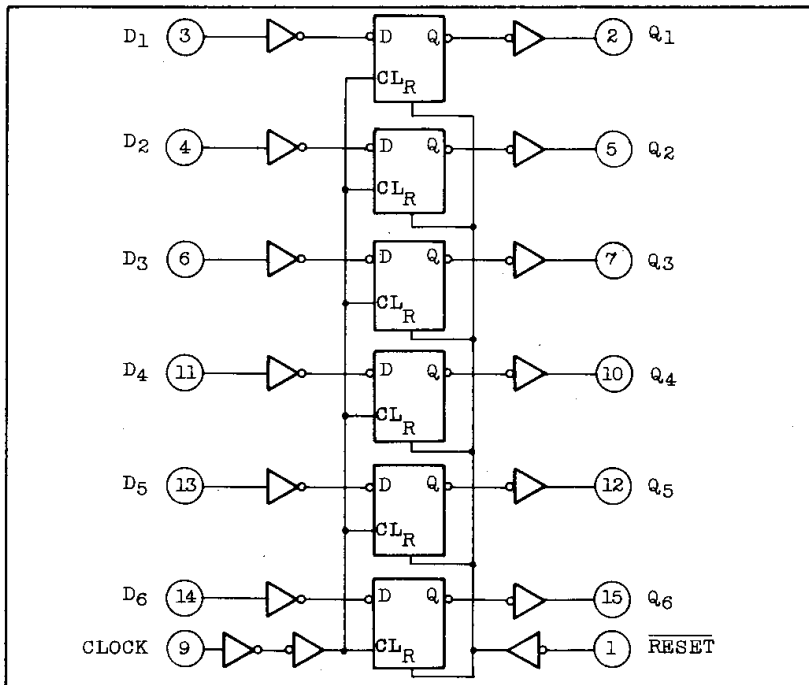
MFP 16 (F16GC-P)

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT
CLOCK [△]	D _n	$\overline{\text{RESET}}$	Q _{n+1}
	H	H	H
	L	H	L
	*	H	Q _n
*	*	L	L

△ : Level change

· : No change

* : Don't care

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RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V _{DD}	3	-	18	V
Input Voltage	V _{IN}	0	-	V _{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V	
			10	9.95	-	9.95	10.00	-	9.95	-		
			15	14.95	-	14.95	15.00	-	14.95	-		
Low-Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.00	0.05	-	0.05	V	
			10	-	0.05	-	0.00	0.05	-	0.05		
			15	-	0.05	-	0.00	0.05	-	0.05		
Output High Current	I _{OH}	V _{OH} =4.6V V _{OH} =2.5V V _{OH} =9.5V V _{OH} =13.5V V _{IN} =V _{SS} , V _{DD}	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA	
			5	-2.5	-	-2.1	-4.0	-	-1.7	-		
			10	-1.5	-	-1.3	-2.2	-	-1.1	-		
			15	-4.0	-	-3.4	-9.0	-	-2.8	-		
Output Low Current	I _{OL}	V _{OL} =0.4V V _{OL} =0.5V V _{OL} =1.5V V _{IN} =V _{SS} , V _{DD}	5	0.61	-	0.51	1.5	-	0.42	-	mA	
			10	1.5	-	1.3	3.8	-	1.1	-		
			15	4.0	-	3.4	15.0	-	2.8	-		
Input High Voltage	V _{IH}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V I _{OUT} < 1μA	5	3.5	-	3.5	2.75	-	3.5	-	V	
			10	7.0	-	7.0	5.5	-	7.0	-		
			15	11.0	-	11.0	8.25	-	11.0	-		
Input Low Voltage	V _{IL}	V _{OUT} =0.5V, 4.5V V _{OUT} =1.0V, 9.0V V _{OUT} =1.5V, 13.5V I _{OUT} < 1μA	5	-	1.5	-	2.25	1.5	-	1.5	V	
			10	-	3.0	-	4.5	3.0	-	3.0		
			15	-	4.0	-	6.75	4.0	-	4.0		
Input Current	"H" Level	I _{IH}	V _{IH} =18V	18	-	0.1	-	10 ⁻⁵	0.1	-	1.0	μA
	"L" Level	I _{IL}	V _{IL} =0V	18	-	-0.1	-	-10 ⁻⁵	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I _{DD}	V _{IN} =V _{SS} , V _{DD} *	5	-	1	-	0.005	1	-	30	μA
			10	-	2	-	0.010	2	-	60	
			15	-	4	-	0.015	4	-	120	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t _{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t _{pLH} t _{pHL}		5	-	150	300	ns
			10	-	65	140	
			15	-	45	100	
Propagation Delay Time ($\overline{\text{RESET}}$ - Q)	t _{pHL}		5	-	170	340	ns
			10	-	70	140	
			15	-	50	100	
Min. Clock Pulse Width	t _w		5	-	55	130	ns
			10	-	20	60	
			15	-	15	40	
Min. Pulse Width ($\overline{\text{RESET}}$)	t _{wL}		5	-	45	100	ns
			10	-	20	50	
			15	-	10	40	
Max. Clock Frequency	f _{CL}		5	3.5	9	-	MHz
			10	6	25	-	
			15	8	34	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t _{rCL} t _{fCL}		5	20	-	-	μs
			10	15	-	-	
			15	15	-	-	

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DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD(V)	MIN.	TYP.	MAX.	UNIT
Min. Set-up Time (DATA - CLOCK)	t _{SU}		5	-	25	50	ns
			10	-	12	25	
			15	-	7	15	
Min. Hold Time (DATA - CLOCK)	t _H		5	-	-8	80	ns
			10	-	0	40	
			15	-	3	30	
Min. Removal Time (RESET - CLOCK)	t _{rem}		5	-	7	40	ns
			10	-	4	20	
			15	-	3	15	
Input Capacitance	C _{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

