

2SJ146

Silicon P-Channel MOS FET

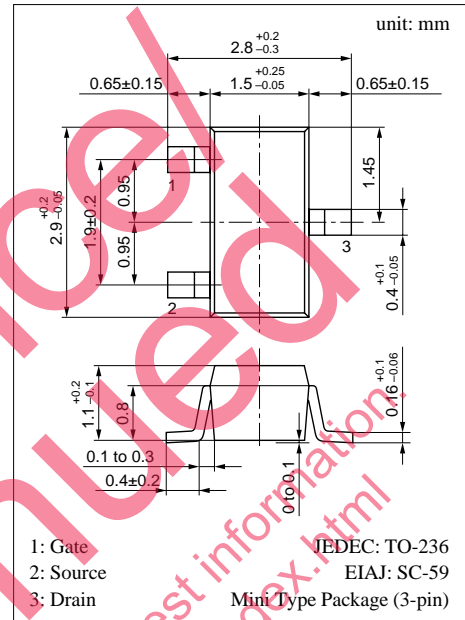
For switching

■ Features

- High-speed switching
- Mini-type package, allowing downsizing of the sets and automatic insertion through the tape/magazine packing.

■ Absolute Maximum Ratings (Ta = 25°C)

| Parameter | Symbol | Ratings | Unit |
|-----------------------------------|-----------|-------------|------|
| Drain to Source breakdown voltage | V_{DSS} | -50 | V |
| Gate to Source voltage | V_{GSO} | -8 | V |
| Drain current | I_D | -100 | mA |
| Max drain current | I_{DP} | -200 | mA |
| Allowable power dissipation | P_D | 150 | mW |
| Channel temperature | T_{ch} | 150 | °C |
| Storage temperature | T_{stg} | -55 to +150 | °C |

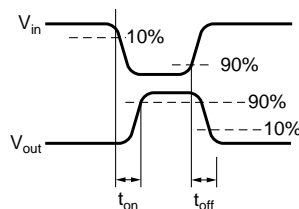
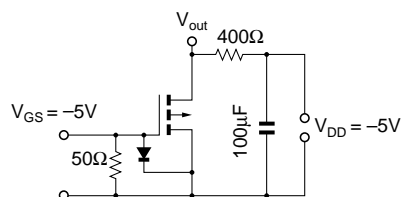


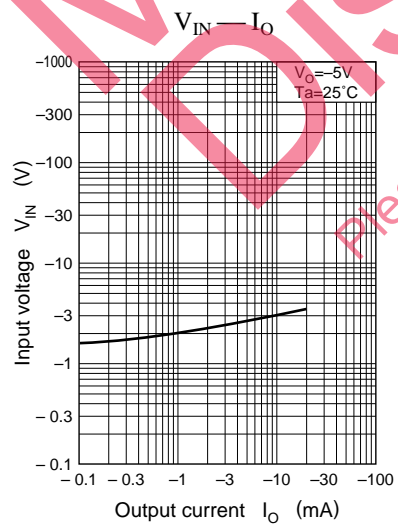
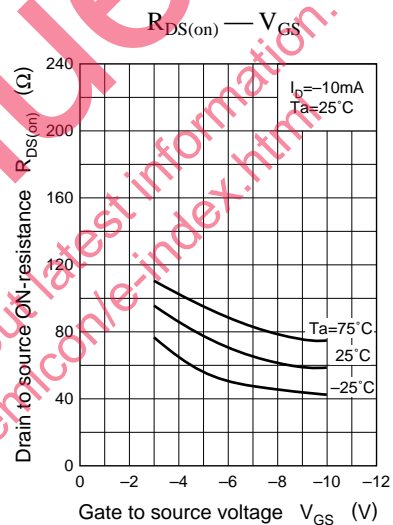
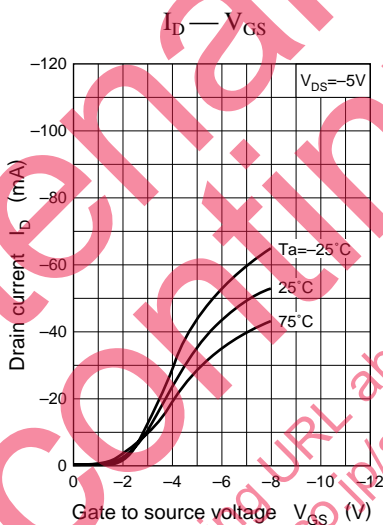
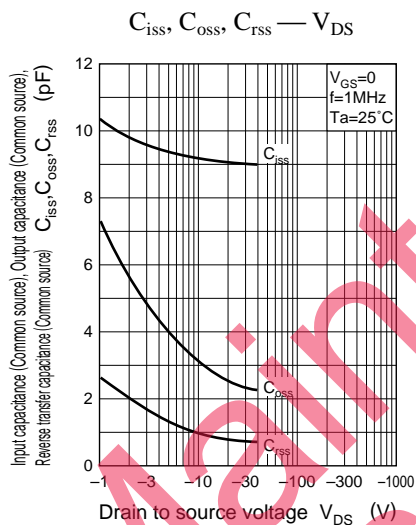
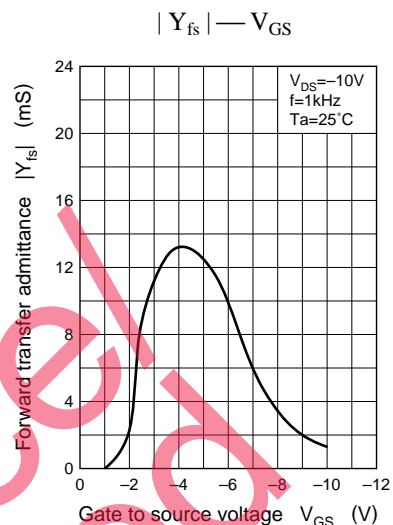
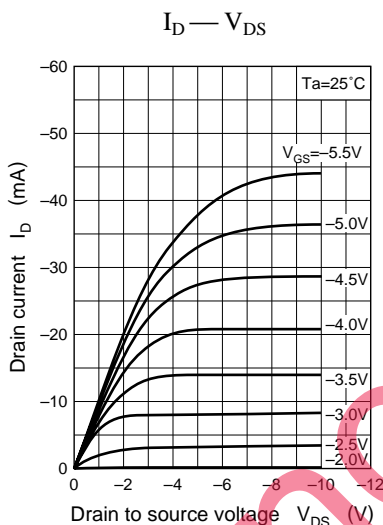
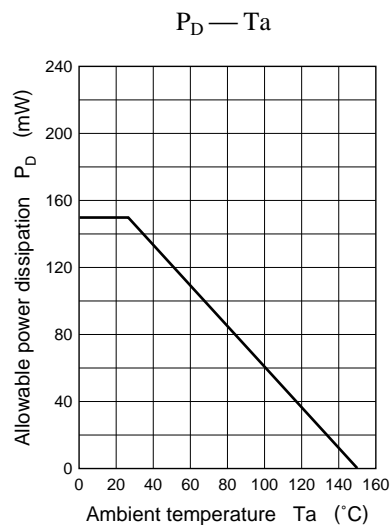
Marking Symbol: 4D

■ Electrical Characteristics (Ta = 25°C)

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--|--------------|---|------|------|------|----------|
| Drain to Source cut-off current | I_{DSS} | $V_{DS} = -30V, V_{GS} = 0$ | | | -10 | μA |
| Gate to Source leakage current | I_{GSS} | $V_{GS} = -8V, V_{DS} = 0$ | | | -1 | μA |
| Drain to Source breakdown voltage | V_{DSS} | $I_D = -100\mu A, V_{GS} = 0$ | -50 | | | V |
| Gate threshold voltage | V_{th} | $V_{DS} = -5V, I_D = -100\mu A$ | -1.5 | | -3.5 | V |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = -10V, I_D = -10mA, f = 1kHz$ | 8 | 13.5 | | mS |
| Drain to Source ON-resistance | $R_{DS(on)}$ | $V_{GS} = -5V, I_D = -10mA$ | | | 150 | Ω |
| Input capacitance (Common Source) | C_{iss} | $V_{DS} = -5V, V_{GS} = 0, f = 1MHz$ | | | 13 | pF |
| Output capacitance (Common Source) | C_{oss} | | | | 7 | pF |
| Reverse transfer capacitance (Common Source) | C_{rss} | | | | 3 | pF |
| Turn-on time | t_{on}^* | $V_{DD} = -5V, V_{GS} = 0 \text{ to } -5V, R_L = 400\Omega$ | | | 40 | ns |
| Turn-off time | t_{off}^* | $V_{DD} = -5V, V_{GS} = -5 \text{ to } 0V, R_L = 400\Omega$ | | | 60 | ns |

* t_{on} , t_{off} measurement circuit





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