



Micro Commercial Components

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SI2302

Features

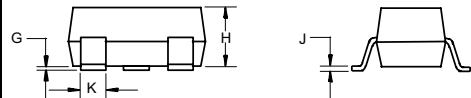
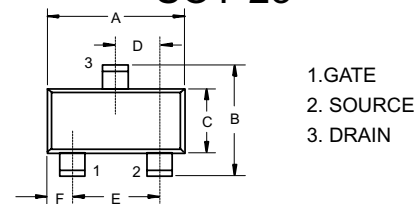
- 20V,3.0A, $R_{DS(ON)}=55m\Omega @ V_{GS}=4.5V$
 $R_{DS(ON)}=82m\Omega @ V_{GS}=2.5V$
- High dense cell design for extremely low $R_{DS(ON)}$
- Rugged and reliable
- Lead free product is acquired
- SOT-23 Package
- Marking Code: S2
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0

Maximum Ratings @ 25°C Unless Otherwise Specified

Symbol	Parameter	Rating	Unit
V_{DS}	Drain-source Voltage	20	V
I_D	Drain Current-Continuous	3	A
I_{DM}	Drain Current-Pulsed ^a	10	A
V_{GS}	Gate-source Voltage	± 8	V
P_D	Total Power Dissipation	1.25	W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^b	100	$^{\circ}C/W$
T_J	Operating Junction Temperature	-55 to +150	$^{\circ}C$
T_{STG}	Storage Temperature	-55 to +150	$^{\circ}C$

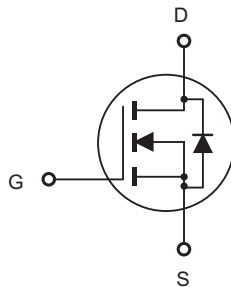
N-Channel Enhancement Mode Field Effect Transistor

SOT-23

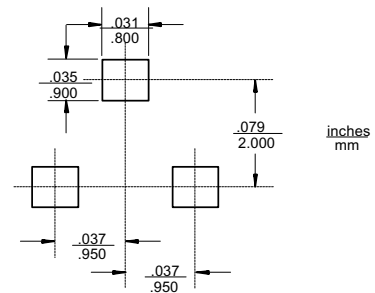


DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.04	
B	.083	.098	2.10	2.64	
C	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
E	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
H	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	.015	.020	.37	.51	

Internal Block Diagram



Suggested Solder Pad Layout





Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 10\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 8V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -8V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 50\mu A$	0.65		1.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3.6A$		55	72	m Ω
		$V_{GS} = 2.5V, I_D = 3.1A$		82	110	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_D = 3.6A$		8.5		S
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0\text{ MHz}$		237		pF
Output Capacitance	C_{oss}			120		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, I_D = 3.6A, V_{GS} = 4.5V, R_{GEN} = 6\Omega$		23	45	ns
Turn-On Rise Time	t_r			11	30	ns
Turn-Off Delay Time	$t_{d(off)}$			34	70	ns
Turn-Off Fall Time	t_f			36	70	ns
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 3.6A, V_{GS} = 4.5V$		6	10	nC
Gate-Source Charge	Q_{gs}			1.4		nC
Gate-Drain Charge	Q_{gd}			1.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				0.94	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 0.94A$			1.2	V
<p>Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.</p>						

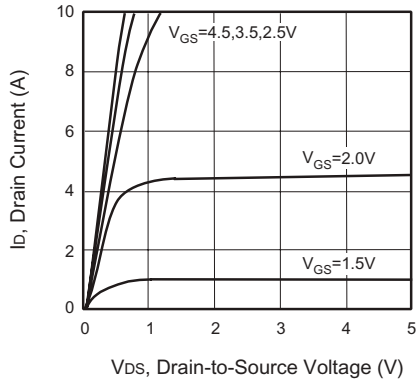


Figure 1. Output Characteristics

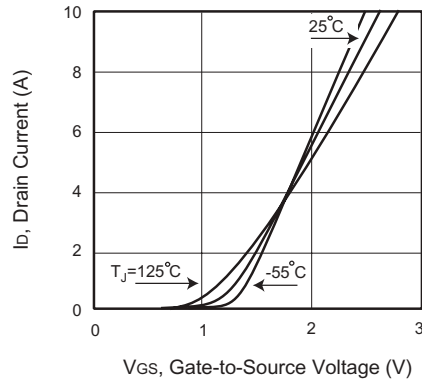


Figure 2. Transfer Characteristics

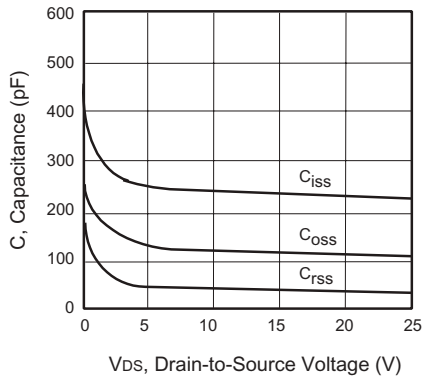


Figure 3. Capacitance

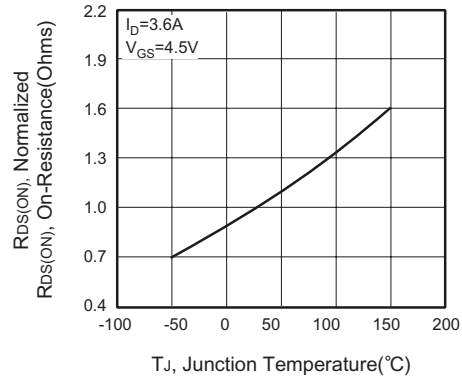


Figure 4. On-Resistance Variation with Temperature

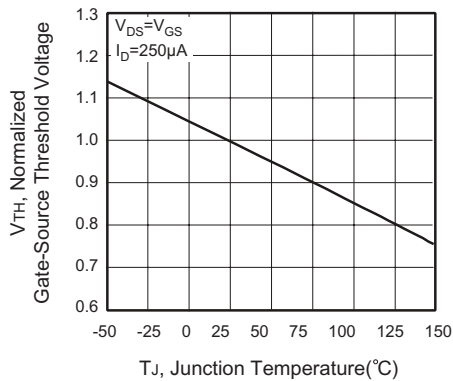


Figure 5. Gate Threshold Variation with Temperature

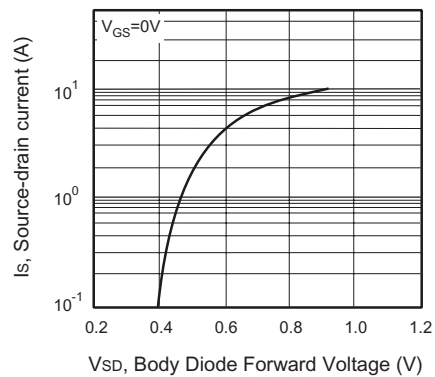


Figure 6. Body Diode Forward Voltage Variation with Source Current

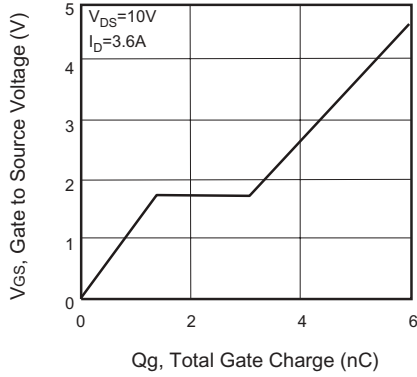


Figure 7. Gate Charge

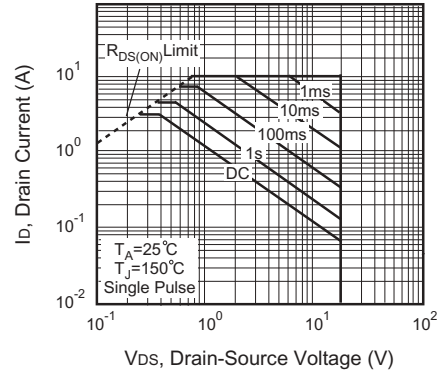


Figure 8. Maximum Safe Operating Area

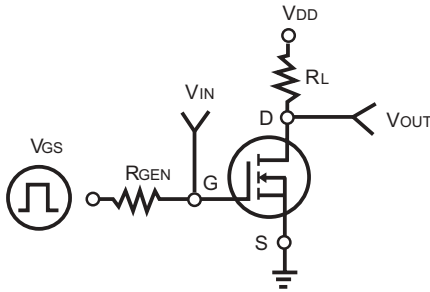


Figure 9. Switching Test Circuit

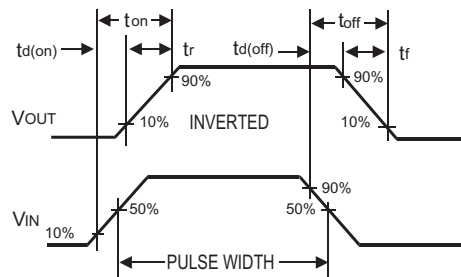


Figure 10. Switching Waveforms

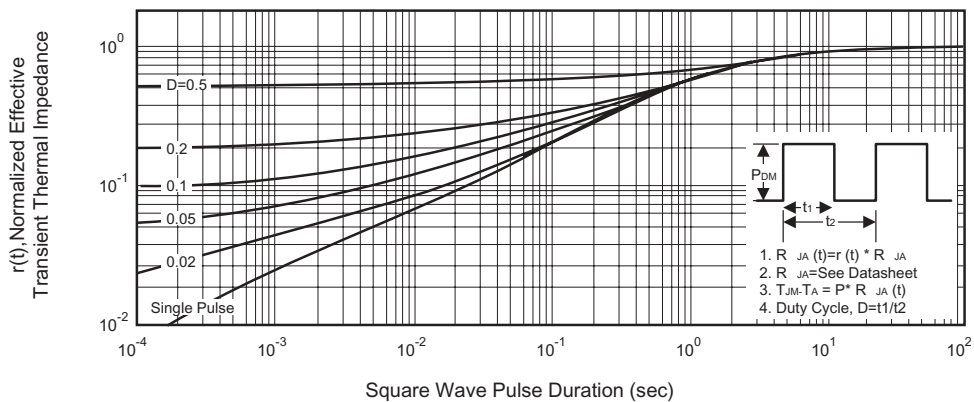


Figure 11. Normalized Thermal Transient Impedance Curve



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Ordering Information

Device (Part Number)-TP	Packing Tape&Reel;3Kpcs/Reel
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