

# MOS FIELD EFFECT POWER TRANSISTOR

## 2SK1282, 1282-Z

### SWITCHING

### N-CHANNEL POWER MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

The 2SK1282/1282-Z is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

- Low On-state Resistance  
 $R_{DS(on)} \leq 0.18 \Omega$  ( $V_{GS} = 10 V, I_D = 2 A$ )  
 $R_{DS(on)} \leq 0.24 \Omega$  ( $V_{GS} = 4 V, I_D = 2 A$ )
- Low  $C_{iss}$   $C_{iss} = 500 pF$  TYP.
- Built-in G-S Gate Protection Diodes

#### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

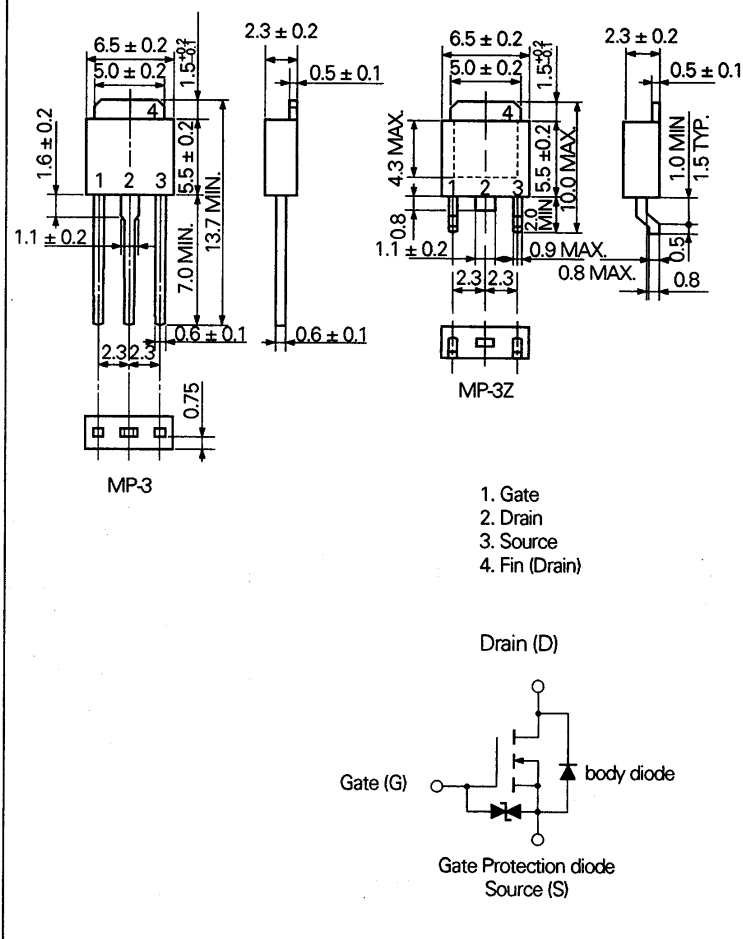
#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 3.0$	A
Drain Current (pulse)	$I_{D(pulse)*}$	$\pm 12$	A
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ ) $P_{T1}$		1.0	W
Total Power Dissipation ( $T_c = 20 \text{ }^\circ\text{C}$ ) $P_{T2}$		20	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$

#### PACKAGE DIMENSIONS

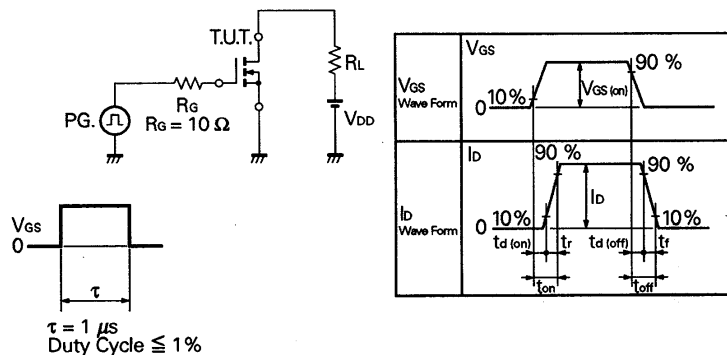
(in millimeters)



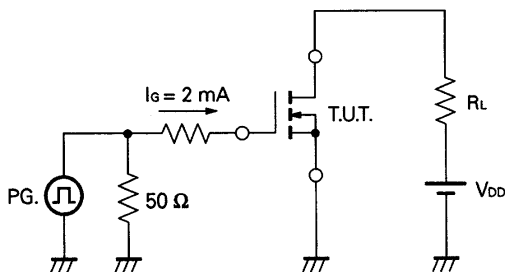
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.15	0.18	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.18	0.24	Ω	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 2 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.4			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		500		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		200		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		40		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		40		ns	V <sub>GS(on)</sub> = 10 V
Rise Time	t <sub>r</sub>		100		ns	V <sub>DD</sub> = 30 V
Turn-Off Delay Time	t <sub>d(off)</sub>		550		ns	I <sub>D</sub> = 2 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		200		ns	R <sub>L</sub> = 15 Ω
Total Gate Charge	Q <sub>G</sub>		13		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		3		nC	I <sub>D</sub> = 3 A
Gate to Drain Charge	Q <sub>GD</sub>		3		nC	V <sub>DD</sub> = 48 V
Diode Forward Voltage	V <sub>SD</sub>		0.9		V	I <sub>SD</sub> = 3 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		140		ns	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		700		nC	di/dt = 50 A/μs

**Test Circuit 1: Switching Time**

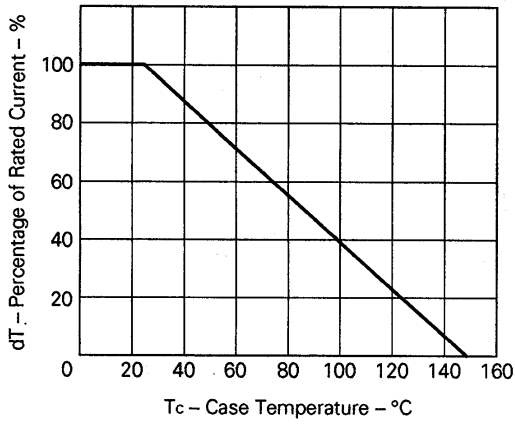


**Test Circuit 2: Gate Charge**

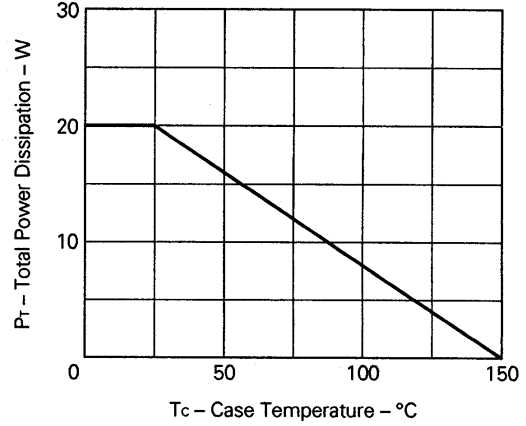


TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )

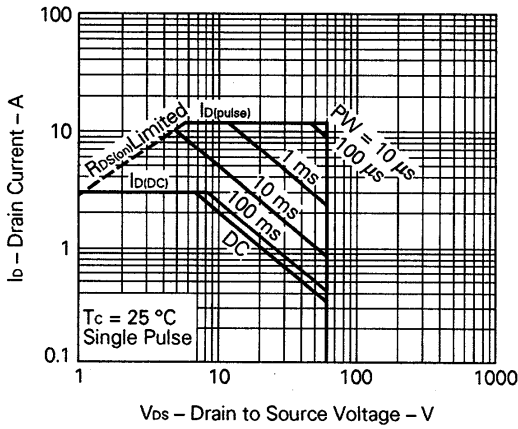
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



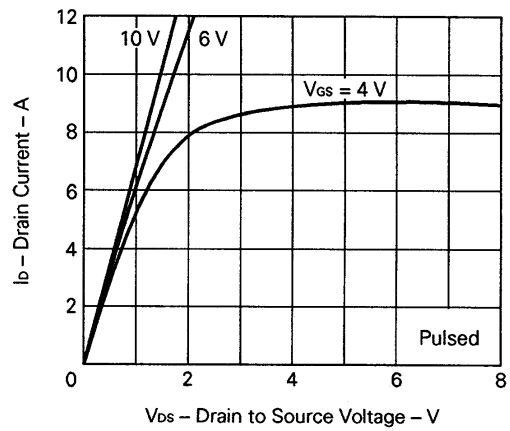
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



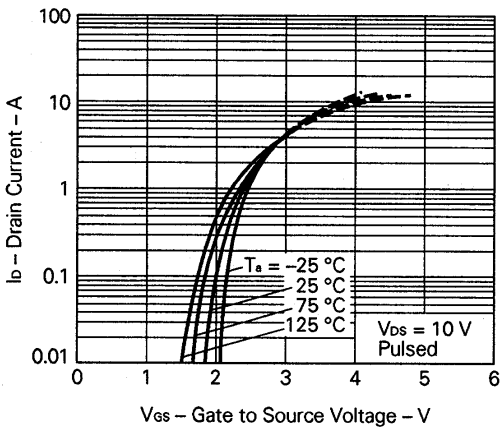
FORWARD BIAS SAFE OPERATING AREA

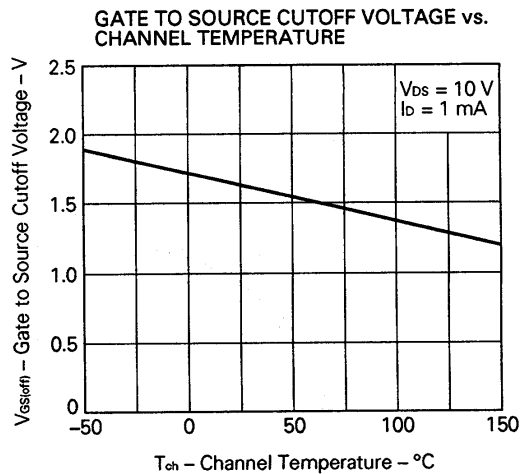
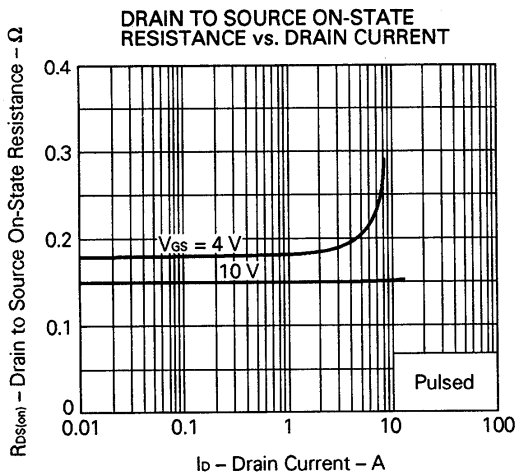
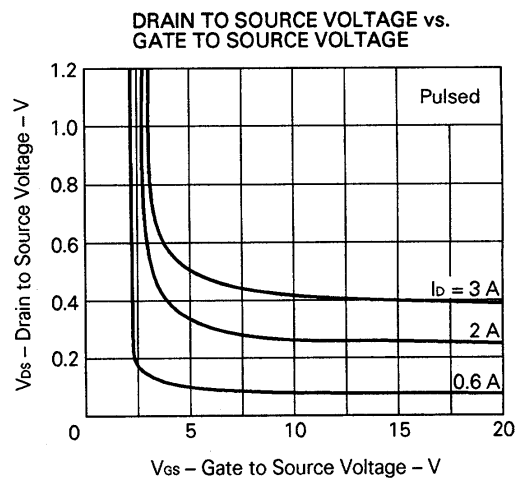
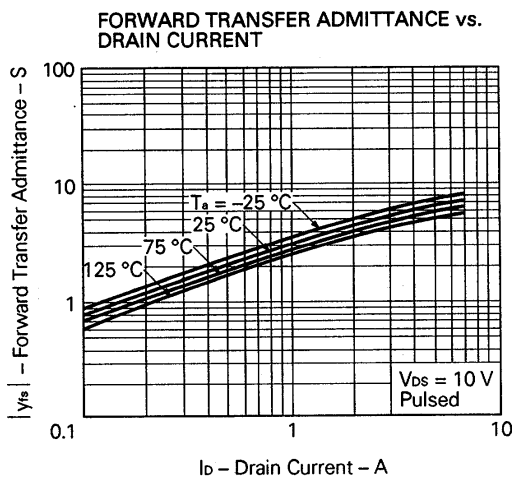
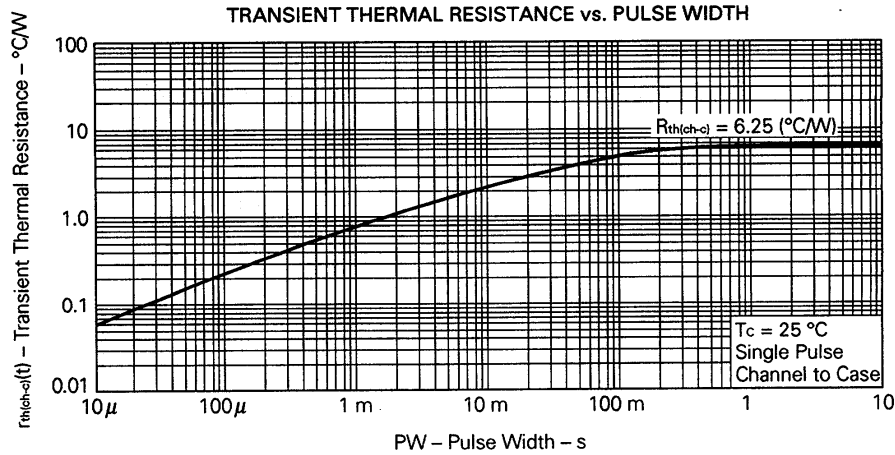


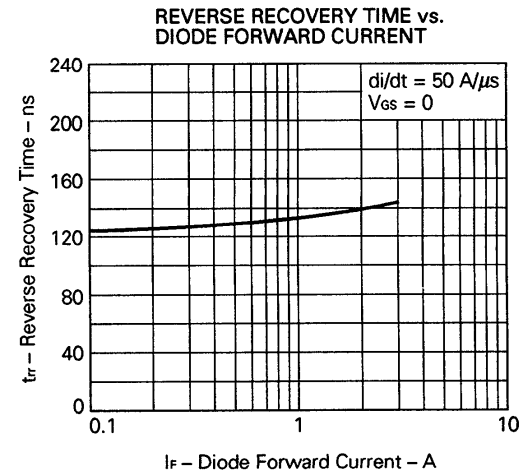
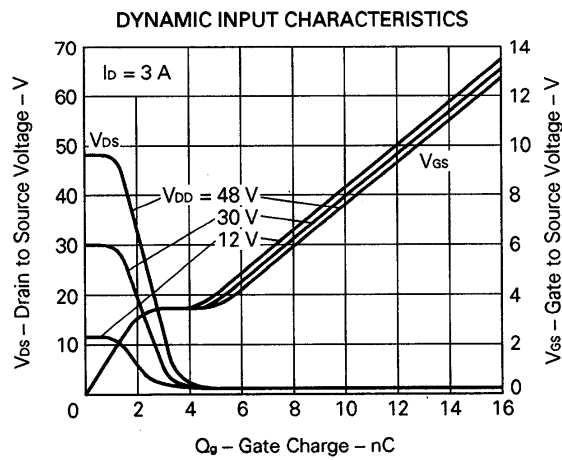
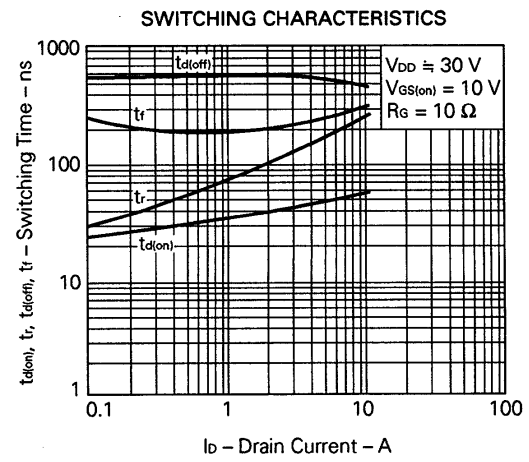
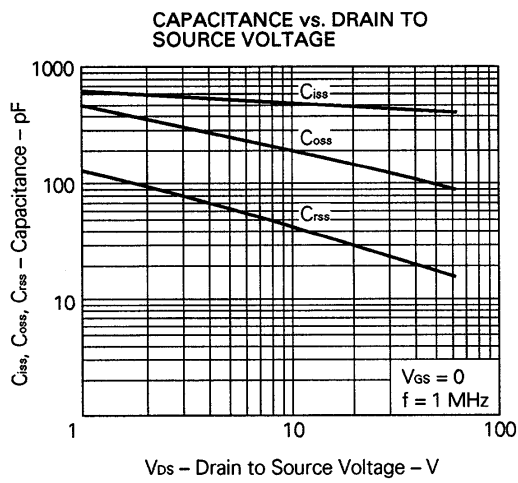
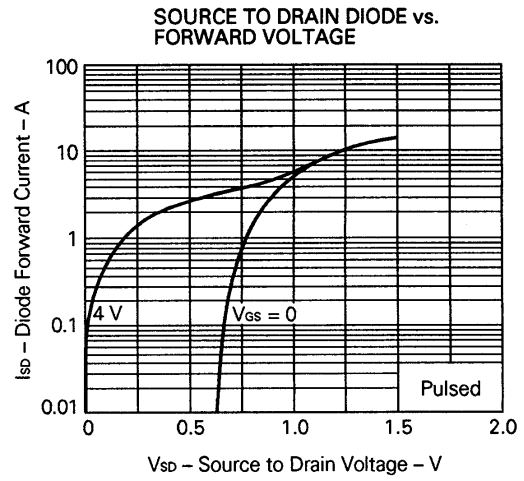
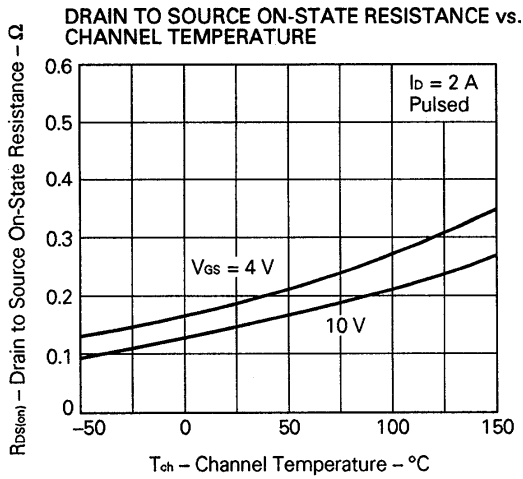
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSFER CHARACTERISTICS







**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

**[MEMO]**

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