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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR 2SK1793, 1793-Z

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK1793 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 7.5 \Omega$ ($V_{GS} = 10 V, I_D = 2 A$)
- Low C_{iss} $C_{iss} = 430 pF$ TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

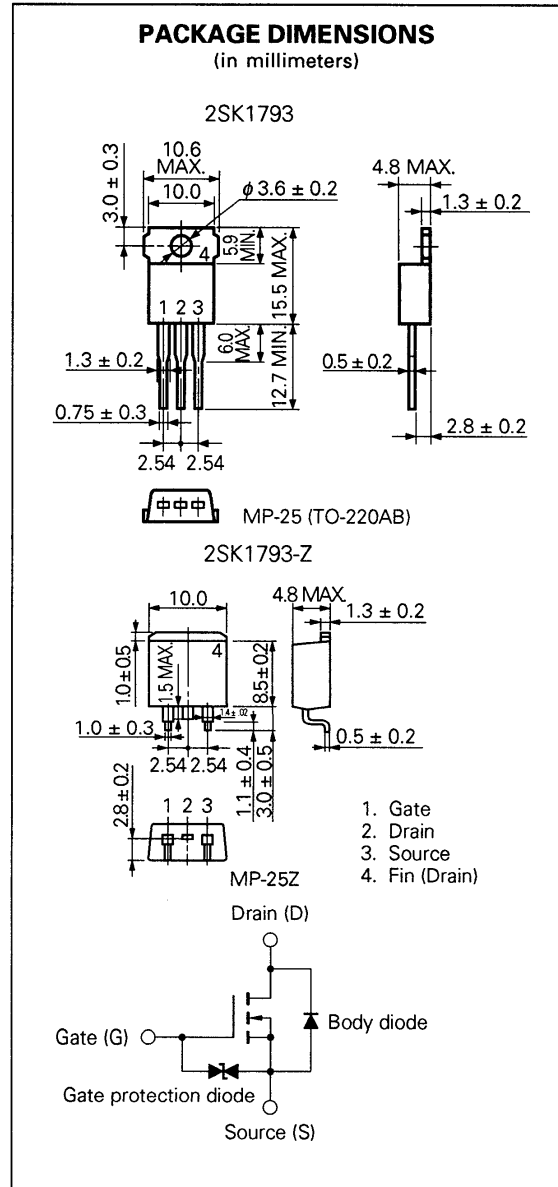
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

| | | | |
|--|------------------|-------------|------------|
| Drain to Source Voltage | V_{DSS} | 900 | V |
| Gate to Source Voltage | V_{GSS} | ± 30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 3 | A |
| Drain Current (pulse) | $I_{D(pulse)^*}$ | ± 6 | A |
| Total Power Dissipation ($T_c = 25^\circ C$) | P_T | 75 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ C$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ C$ |
| Single Avalanche Current | I_{AS}^{**} | 3 | A |
| Single Avalanche Energy | E_{AS}^{**} | 5.4 | mJ |

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

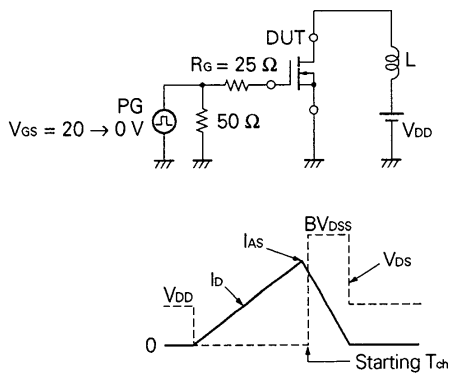
** Starting $T_{ch} = 25^\circ C$, $R_{\theta} = 25 \Omega$, $V_{GS} = 20 V \rightarrow 0$



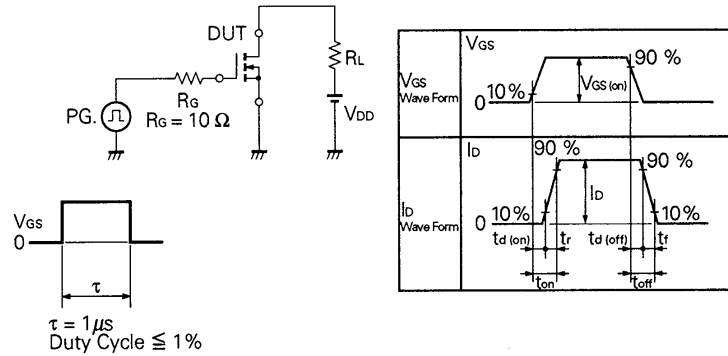
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|------|------|------|---|
| Drain to Source On-state Resistance | R _{Ds(on)} | | 6.2 | 7.5 | Ω | V _{GS} = 10 V, I _D = 2 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 2.5 | | 3.5 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | y _{fs} | 0.8 | 2.0 | | S | V _{DS} = 20 V, I _D = 2 A |
| Drain Leakage Current | I _{DSS} | | | 100 | μA | V _{DS} = 900 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±30 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 430 | | pF | V _{DS} = 10 V |
| Output Capacitance | C _{oss} | | 65 | | pF | V _{GS} = 0 |
| Reverse Transfer Capacitance | C _{rss} | | 21 | | pF | f = 1 MHz |
| Turn-On Delay Time | t _{d(on)} | | 10 | | ns | V _{GS(on)} = 10 V |
| Rise Time | t _r | | 15 | | ns | V _{DD} = 150 V |
| Turn-Off Delay Time | t _{d(off)} | | 40 | | ns | I _D = 2 A, R _G = 10 Ω |
| Fall Time | t _f | | 10 | | ns | R _L = 75 Ω |
| Total Gate Charge | Q _G | | 19 | | nC | V _{GS} = 10 V |
| Gate to Source Charge | Q _{GS} | | 7 | | nC | I _D = 3 A |
| Gate to Drain Charge | Q _{GD} | | 7 | | nC | V _{DD} = 720 V |
| Diode Forward Voltage | V _{F(S-D)} | | 0.9 | | V | I _F = 3 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 470 | | ns | I _F = 3 A |
| Reverse Recovery Charge | Q _{rr} | | 1.9 | | μC | di/dt = 50 A/μs |

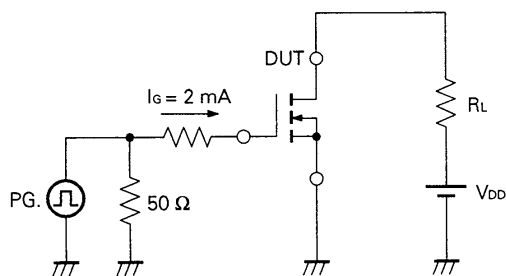
Test Circuit 1: Avalanche Capability



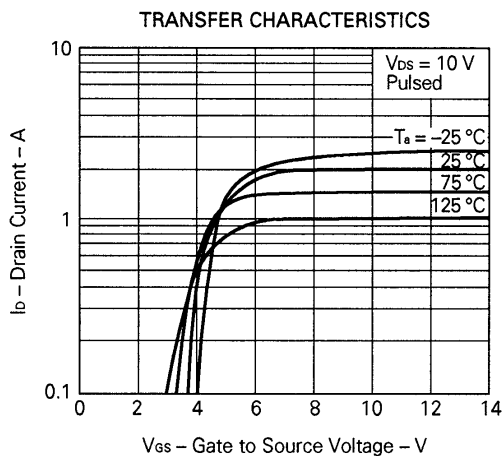
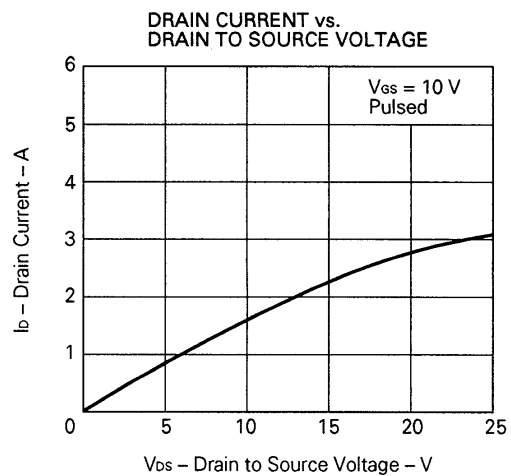
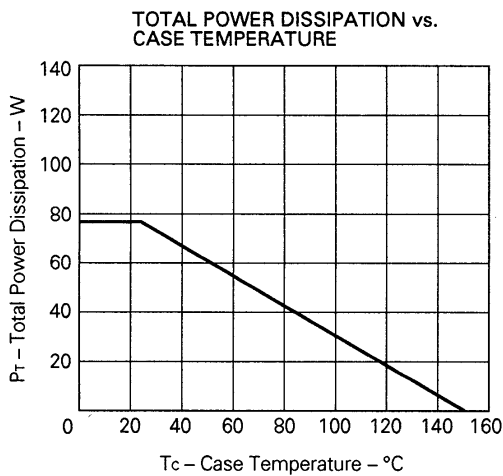
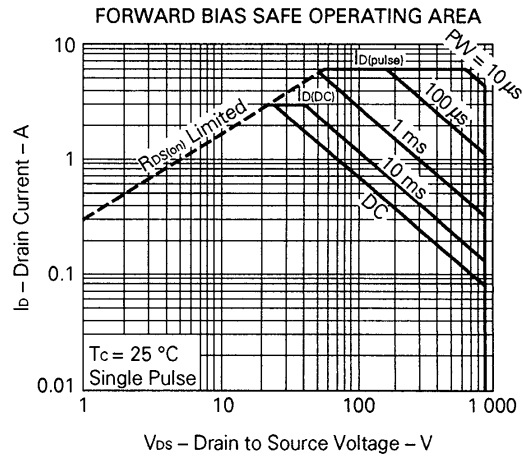
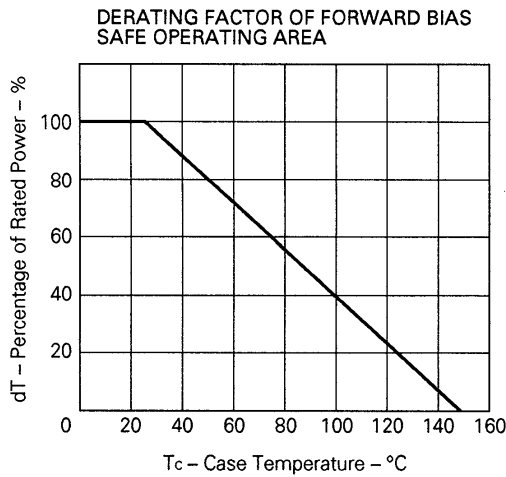
Test Circuit 2: Switching Time

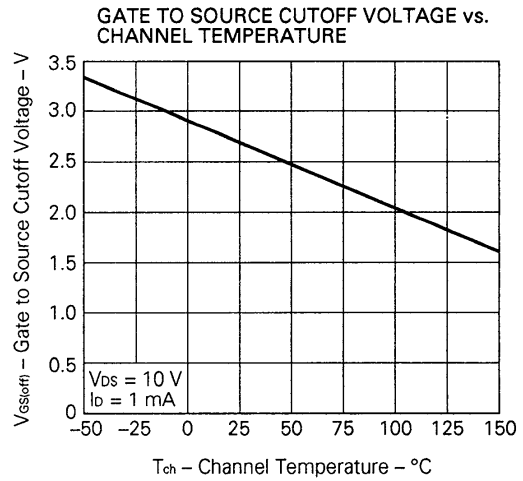
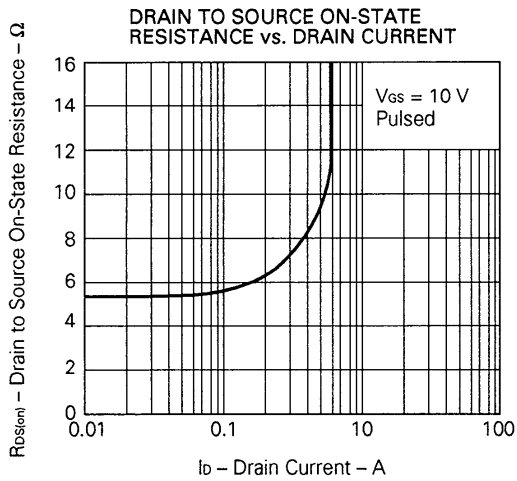
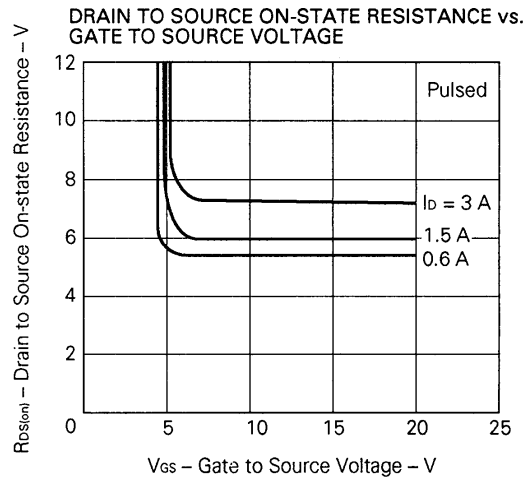
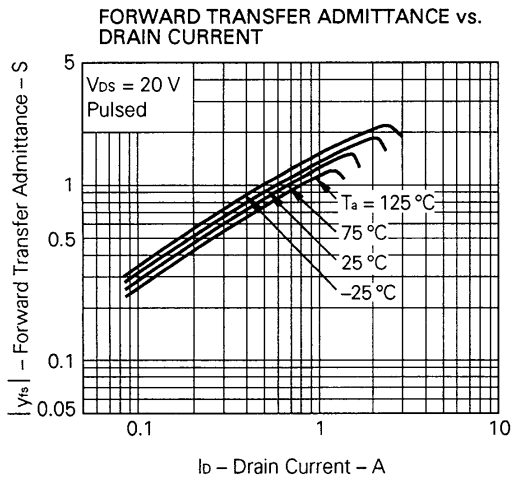
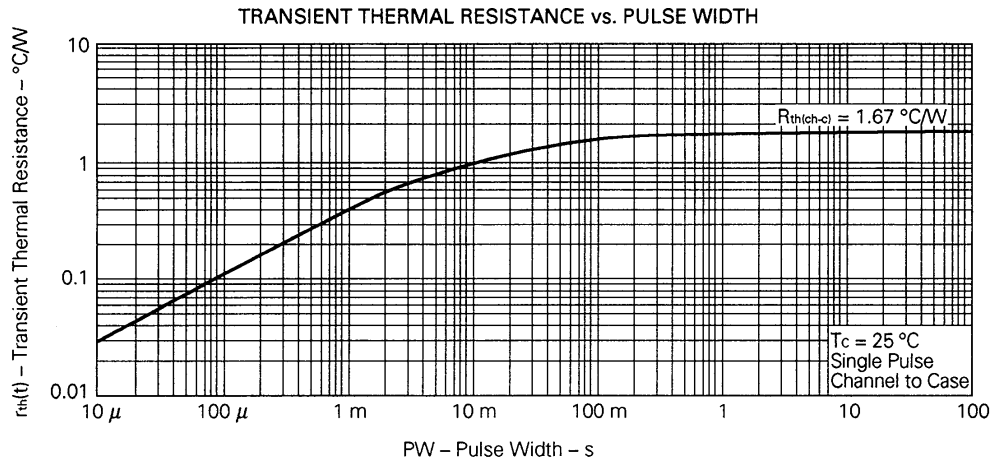


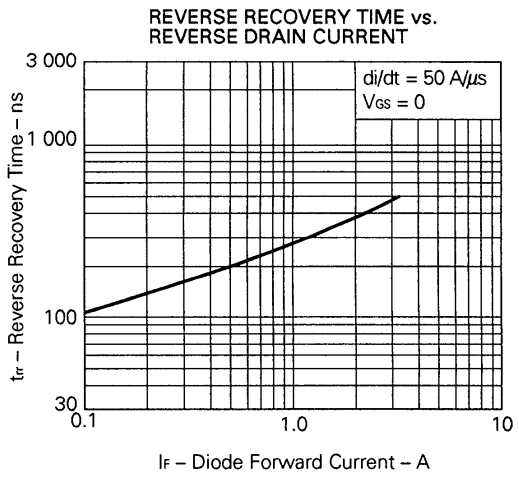
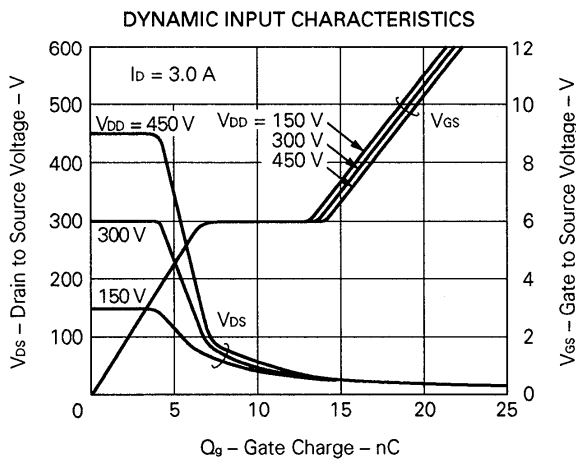
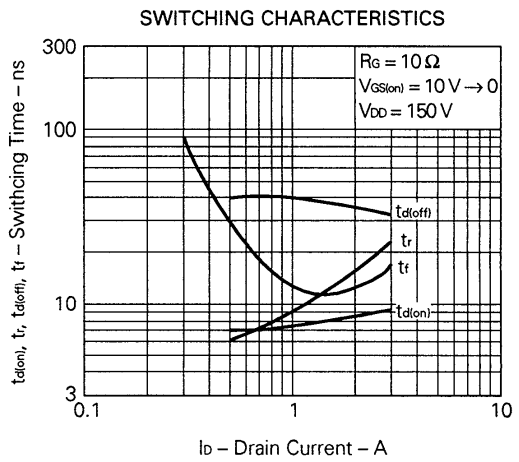
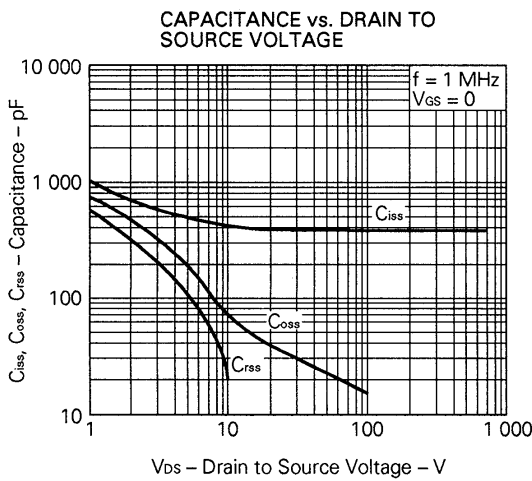
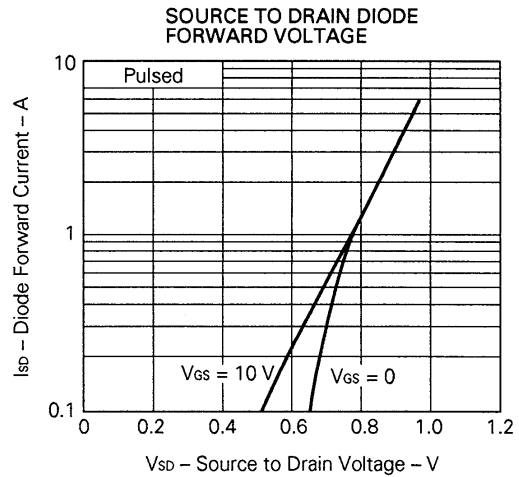
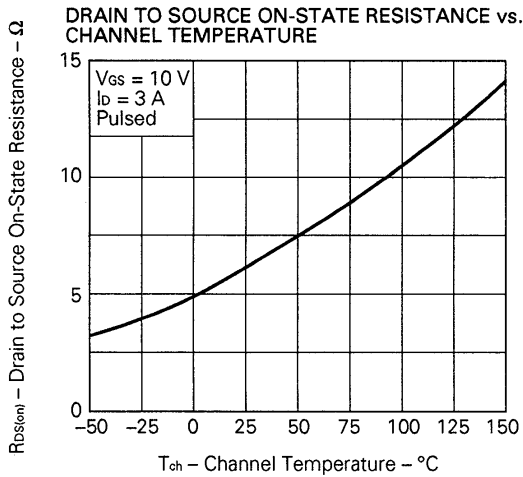
Test Circuit 3: Gate Charge

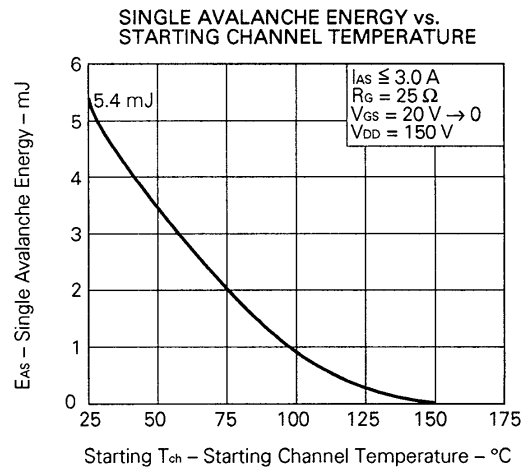
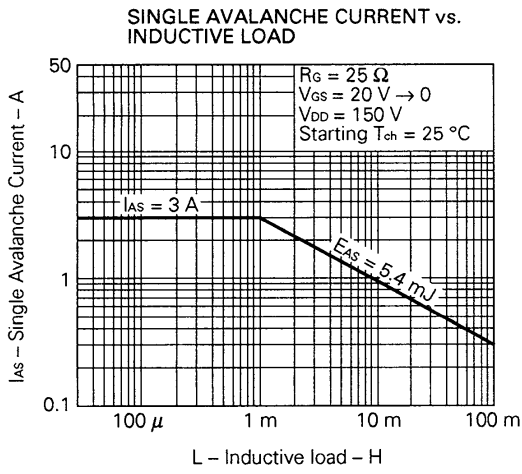


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)









Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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M4 92.6